S700 Datasheet Brief

Version: 1.2

2017-05-23

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Revision History

Date	Revision	Description
2016-07-21	1.1	First release
2017-5-23	1.2	Add USB3 HOST

Introduction

1.1 Overview

S700 is a versatile high-performance, low-power and highly-integrated SoC (System on Chip), it integrates 64-bit Quad-core ARM Cortex-A53SMP4 processor with TrustZone Security system embedded. The powerful Mali-450 MP4 GPU provides a maximized 3D/2D graphic processing effect delivering excellent gaming experience. Compact integrated VPU is qualified for high performance of almost full formats video decoding/encoding capabilities. Advanced Display Engine is designed for display subsystem with low power and low bandwidth.

S700 integrated high efficient DDR Controller which guarantees high data throughput while video/audio playing and 16 million colors LCD and touch panel interfaces are qualified for high quality user interface. Other rich interfaces including LVDS, HDMI transmitter, SDIO and MIPI CSI are qualified for building flexible solutions. USB 3.0 is for Supper Speed of mass data transmission between S700 and slave/hub. Large capacity NAND Flash up to 70-bit ECC is supported for data stability. Other rich interfaces such as UART, SPI and TWI promote the extension ability of the system.

Together with our in-house designed PMU & Audio Codec co-chip ATC260x, S700 provides a true ‘ALL IN ONE’ solution, which makes it the best choice for high-end smart devices with reasonable price.

1.2 Applications

S700 is a highly integrated Application Processor that can perform comprehensive functionalities. It is applicable to a wide variety of smart MID (Multimedia Internet Device) platforms. It is an ideal choice for designing customized solutions as it provides an open and friendly system development kits. S700 is suitable but not limited for the applications below:

- Tablet
- Ultra book
- Smart TV-Box
- POS machine
- ATM machine
- Advertising Machine
- Net book
- Game console
- Smart monitor
- Other smart devices

1.3 Features

1.3.1 CPU (Central Processing Unit)

- 64-bit Multi-core ARM Cortex-A53SMp4 processor
- ARMv8-AArchitecture and AArch64 & AArch32 instruction set supported
- 32KB Instruction cache and 32KB Data cache for CPU0~3
- 512KB L2 cache
- SCU responsible for maintaining coherency among L1 data caches
- Programmable MMU (memory management unit)
- Vector Floating-Point v3 (VFPv3) architecture for floating-point computation that is compliant with the IEEE 754 standard
- Advanced SIMD technology to accelerate the performance of multimedia applications such as 3-D graphics and image processing
- CoreSight debug supported
- Secure Access supported including TrustZone

1.3.2 GPU (Graphic Process Unit)

- Mali-450 MP GPU
- OpenGL ES2.0/1.1, OpenVG 1.1, EGL 1.5
- Four Pixel Processor features
  - each pixel processor used processes a different tile, enabling a faster turnaround
  - programmable fragment shader
  - alpha blending
  - complete non-power-of-2 texture support
  - cube mapping
  - fast dynamic branching
  - fast trigonometric functions, including arctangent
  - full floating-point arithmetic
  - frame buffer blend with destination Alpha
  - indexable texture samplers
  - line, quad, triangle and point sprites
  - no limit on program length
  - perspective correct texturing
  - point sampling, bilinear, and tri-linear filtering
  - programmable mipmap level-of-detail biasing and replacement
  - stencil buffering, 8-bit
  - two-sided stencil
  - unlimited dependent texture reads
  - 4-level hierarchical Z and stencil operations
  - 4-bit per texel compressed texture format
  - Up to 512 times Full Scene Anti-Aliasing (FSAA). 4x multisampling by 128x
  - Super sampling

- Two Geometry Processor features
  - two programmable vertex shaders
  - flexible input and output formats
  - autonomous operation tile list generation
  - indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads.

1.3.3 Video Subsystem

- **Video Decoder**
- Support Real-time video decoder of most popular video formats (some are supported by the 3rd party

applications), such as MPEG-4, H.264, H265, etc.
- Error detection and concealment support for all video formats
- With 2D reference data cache to reduce DDR bandwidth
- Output data format is YUV420 semi-planar
- Average data rate 60Mbps, peak rate up to 120Mbps

- **Video Encoder**
- Support video encoder for baseline H.264
- Only support I and P slices
- Input data format:
  - YUV420SP
  - YVU420SP
  - YUV420P
  - ARGB
  - ABGR
  - ARGBA
  - BGRA
  - RGB565
  - BGR565
- Support VBR and CBR
- Max fps is up to 60fps@1920*1080
- Video size is from 176*144 to 1920*1088
- Support upscale and downscale, from 1/2 to 8
- Low latency data encoder

- **JPEC Decoder**
- Input JPEG file: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:4 ,211H, 211V sampling formats
- Output raw image: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
- For JPEG Baseline Decoder size is from 48x48 to 30000*15000 (450Mpixels)
- For Progressive Decoder size is from 48x48 to 8192x8192
- Support JPEG ROI (region of image) decode
- Maximum data rate is up to 100million pixels per second

- **JPEG Encoder**
- Input data format support:
  - YUV420sp
  - YVU420sp
  - YUV420P
  - ARGB
  - ABGR
  - ARGBA
  - BGRA
  - RGB565
  - BGR565
- Max data rate up to 70million pixels per second
- Image size is from 48*48 to 8176*8176
- Support upscale and downscale, from 1/2 to 8

1.3.4 Secure Subsystem

- ARM® TrustZone® Security Technology
- Special SRAM is included for security service
- Special accelerator for AES-128 Encrypt & Decrypt in ECB/CBC/CBC-CTS mode
- One-time programmed Root key
- Flexible module data path control
- 2048-bit E-fuse equipped

- HDCP Tx
  - Uses AES-128 encryption;
  - Compliant to HDCP revision up to 2.2;
  - Support repeaters;
  - Inside Random Number Generator compliant to NIST-SP 800 90;
  - Inside HMAC-SHA256 block;
  - Inside Input and Output FIFO for raw and Encryption datum;
  - Inside TS packet compliant to blu-ray and MPEG2 format;
  - Support PES portion Encryption mode.

1.3.5 Internal Memory

- **Boot ROM**
- Size: 32KB
- Support boot from the following device:
  - eMMC
  - SPI NOR Flash
  - 8bits Async NAND Flash
  - 8bits Toggle NAND Flash
  - SD/TF card
  - USB driver is inside for upgrading firmware and hardware test

1.3.6 External Memory

- **DRAM**
- 16/32-bit LPDDR2/LPDDR3
- 16/8-bit DDR3/DDR3L
- Up to 4GB supported
- Internal ODT resistance to improve signal integrity
- Programmable input DQS signal calibration option, calibration period is also programmable
- Differential DQS signal to achieve stable data strobe
- Optional ZQ calibration command in programmable period
- Hardware options in DDR state manage to reduce DDR power in some low bandwidth application
- Built-in hardware monitor to improve system debug
- Built-in hardware bandwidth performance counter
- Support more than 4 command processing concurrently in one cycle
- Command reorder in some circumstance to improve bandwidth
- 4GB SDRAM address (2GB per CS)
- Support single or double rank addressing

- **NAND Flash**
- Support both Async (include LBA NAND) and Sync NAND Flash, up to 4 CEs.
- SLC, MLC and TLC NAND Flash supported
- Support Toggle DDR NAND v1.0 and Toggle DDR NAND v2.0.
- Support Open NAND Flash Interface (ONFI) up to v3.0.
- Up to 70bit hardware ECC.
- Ready/Busy signal monitor by hardware automatically.
- Support sync NAND Flash Interface up to 200MHz.
- Support both 3.3v and 1.8v VCCQ.

- **SD/MMC/EMMC**
- 3 on-chip SD Controller integrated
- Support
  - SD/HCSD/SDXC(SRD50mode), miniSD
  - microSD
  - Memory card

  - MMC/RSMMC/MMCPLUS card
  - INAND
  - MOVINAND
  - eMMC
  - SDIO card
- Support SD 3.0, SDIO 3.0 and MMC4.5 protocol，complies with eMMC 5.0 and 5.1
- Support 1 bit, 4bit, 8bit, bus mode.
- Clock max rate up to 170MHz.
- Support IRQ and DMA mode to transmit data
- Contain 512BYTE SRAM*2
- Read /Write CRC Status Hardware auto checked.
- Support Auto multi Block read/write mode.
- Support boot mode.
- Hardware timeout/delay function.
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing.
- Built-in pull up resistance for CMD/DAT lines.
- Support HS200 mode

1.3.7 System Control

- **DMA**
- 10 independent DMA channels in DMA Controller
- Data path is supported with memory to memory, memory to peripheral, peripheral to memory
- Support linklist transfer type
- Support chain transfer type between the different channels
- Support constant fill mode to initial memory
- Support stride mode for frame buffer data transfer
- Support reload mode
- The RW priority of ALL channels can be setting independently
- Support byte align transfer between memory and memory

- **CMU**
- One oscillator with 24MHz clock input and 7 embedded PLLs
- The DDRPLL NANDPLL Display PLL have optional spread-spectrum function to reduce EMS
- Clock gating control for individual components

- **Timer**
- 2 on-chip 2Hz Controller and 2 on-chip Timer Controller inside
- Support IRQ mode
- A global timer, and a watchdog and private timer for each Cortex-A53 processor present in the cluster.

1.3.8 Camera & TVIN Interface

- **MIPI CSI**
- Compliant with MIPI CSI-2 Specification version 1.0 and the D-PHY specification version 0.9
- High-Speed Mode: 80 Mbps to 1 Gbps synchronous
- Support low power mode and ultra low power support
- Support Data Type: YUV422-8bit, RGB565, RGB888
- 1-4 Data Lanes Configurable

- **Sensor interface / TVIN**
- Two sensor input channels
- Support YUYV, RGB565, RGB888 sensor interface
- Windowing function

- 8-bit data parallel with Hsync, Vsync, Pclk
- YUV input sequence selection and storing format selection
- Max support 12M pixel input
- BT656 and BT601 interface support

1.3.9 Display Subsystem

- **Advanced Display Engine**
- Four macro layers (4 sublayer includes in a macro layers)
- Support overlap, scale, crop, blender
- Support xflip, yflip
- Alpha blending, color key, dither and color space conversion, Gamma correction support
- Gamma correction
- Scalar input & output size up to 4096*4096
- Simultaneously output to TV and LCD support
- Support HDMI 3D
- Support source format:
  - ARGB8888, ABGR8888, RGBA8888, BGRA8888
  - RGB 888, BGR 888
  - RGB565, BGR565
  - ARGB1555, ABGR1555, RGBA5551, BGRA5551
  - YUV 4:2:0 planer 8bit/10bit
  - YUV/YVU 420 semi 8bit/10bit
  - IMG FBDC 16*4

- **LCD Controller**
- Support dual channel LVDS interface LCD
- Support active (TFT) LCD panels with digital RGB input interface
- Support MIPI interface
- Programmable timing control for various panels
- Pixel stream input without strict timing requirements
- Maximum 16777216 simultaneous display color
- Fill the empty field when output size < LCD display size
- Support VBI, HBI, AVSI, FEI (Frame end interrupt)

- **MIPI DSI**
- Compliant with MIPI DSI Specification version 1.01 and the D-PHY specification version 0.9
- Display Resolutions up to 1920*1200
- Pixel Format:
- Command Mode: RGB233, RGB444, RGB565, RGB666 (Loosely), and RGB888
- Video Mode: RGB565, RGB666 (Packed), RGB666 (Loosely), and RGB888
- Command and Video mode support(type 1,2,3 and 4 display architecture)
- Low power and ultra low power support
- 75 Mbps to 1Gbps per lane
- Support 1-4 data lanes

- **LVDS**
- Comply with the TIA/EIA-644-A LVDS standard
- Support reference clock frequency range from 10Mhz to 148.5Mhz
- Support LVDS RGB 24/18bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, Odd/even channel Mirror/ swap

- **HDMI**
- Compatible with HDMI 1.4b, HDCP1.4 and DVI 1.0

- Support most video formats from 480i to 1080p and 4k*2k@30Hz, such as:
  - 640*480p@59.94/60Hz
  - 720*480p@59.94/60Hz
  - 720*576p@50Hz
  - 1280*720p@59.94/60Hz
  - 1280*720p@50Hz
  - 720(1440)*480i@59.94/60Hz
  - 720(1440)*576i@50Hz
  - 1440*480p@59.94/60Hz
  - 1440*576p@50Hz
  - 1920*1080i@59.94/60Hz
  - 1920*1080i@50Hz
  - 1920*1080p@24Hz
  - 1920*1080p@59.94/60Hz
  - 1920*1080p@50Hz
  - 3840*2160@24Hz/25Hz/30Hz
  - 4096*2160@24Hz/25Hz/30Hz
- Support 24bit, 30bit, 36bit RGB/YCbCr 4:4:4 format (Deep Color)
- Support xvYCC601, xvYCC709 Enhanced Colorimetry format
- Support IEC60958 audio format up to 24bits
- Support High-bitrate compressed audio formats
- Support up to 8-channel Audio sample, supports 48/96/192/44.2/88.4/176.8kHz audio sample rate
- Support Auto-Lipsync Correction feature
- Support 3D Frame Packing Structure up to 1080p@60Hz
- Support 3D Side-by-Side (Half) Structure with 1080i@59.94/60Hz, 1080i@50Hz, etc.
- Support 3D Top-and-Bottom Structure with 1080p@24Hz, 720p@50Hz, 720p@59.94/60Hz, etc.

- **TVOUT**
- Support NTSC and PAL format for CVBS output
- Four 12-bit video DAC outputs sample rate up to 300MHz

1.3.10 High Speed Interfaces

- **USB3.0 XHCI**
- Host and device mode is supported
- Fully compliant with USB Specification 3.0
- Fully compliant with USB Specification 2.0
- Device mode Supports USB Supper Speed(5Gb/s), High Speed (480Mb/s) and Full Speed (12Mb/s)
- Host mode Supports USB Supper Speed, High Speed, Full Speed and Low Speed
- Supports Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Interface UTMI+(level3)
- Embedded USB Supper Speed Transceiver which complies with Interface PIPE3(32 bits)
- Supports DMA master interface
- Supports 4 out endpoints and 4 In endpoints excluded control endpoints
- Host supports 2 USB ports(1 supper speed port and 1 high speed ports)
- Up to 31 devices are supports by the Host
- Supports USB remote wake-up feature
- Host mode is compliant with XHCI architecture
- Downstearm hub function is supported
-

- **USB2.0**
- Two independent USB2.0 Controllers inside
- UTMI+ level2 Transceiver Macrocell Interface.
- HSIC Interface for an option.

- One OTG function complied with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a and the other working as either Device or Host
- Support Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) with USB20.
- Support point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (one series downstream HUB supported).
- Support full-speed or high-speed in peripheral mode.
- Support high-speed high-bandwidth isochronous transfer and Interrupt transfer.
- Integrated 15KB single port RAM as IN, OUT endpoint buffer. Partially configurable endpoint buffer size, endpoint type with single, double, triple or quad buffering.
- Supports suspend, resume and power managements function.
- Support remote wakeup.
- An optional HSIC interface for USBH1 Controller.
- One OTG function and the other working as either Device or Host

- **UART/IRC**

- 7 on-chip UART Controllers inside
- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 levels Transmit FIFO and 32 levels Receive FIFO
- Capable of speeds up to 3Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data.
- Only UART2/3/4 support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- Only UART0 support IRC(infrared remote control) Inputs
- Support RC6/RC5/9012/NEC(8bit) protocol.
- Need to connect an IR receiver when use.

- **TWI**

- 4 on-chip TWI Controllers inside
- Both master and slave functions support
- Support standard mode (100kbps), fast-speed mode (400kpbs), fast-plus-speed mode (1Mpbs), High-Speed mode (3.4Mbps)
- Multi-master capability
- 10-bit address mode not support
- Internal Pull-Up Resistor (1.5kOhm) optional
- 8bit*128 TX FIFO and 8bit*128 RX FIFO

- **SPI**

- 4 on-chip SPI Controllers inside
- Support master mode and slave mode. The speed of master mode up to 60Mbps, and slaver up to 20Mbps.
- 32bit x32 TX FIFO and 32bit x32 RX FIFO
- Support dual I/O write and read mode while use as master
- Support single data rate mode and double data rate (DDR mode) while use as master
- Support two wire mode, only use SCLK and MOSI signal
- Support IRQ and DMA mode to transmit data
- Support system program boot from SPI nor-Flash

- **I2S**

- 2 channels (1 TX, 1 RX)
- Support 2.0-channel I2S transmitter and receiver
- Support 7.1-channel and 5.1-channel through I2S transmitter with ext.8-channel and 6-channel DAC by TDM (time-division multiplexed) Mode.
- Support 4-channel through I2S receiver, by TDM Mode for 4-channel record.
- Audio data up to 24bits
- Sample rate up to 192KHz

- Provide master work mode

- **SPDIF**
- Support transmitter mode.
- Support sample rate 96k/48k/44.1k/32k
- Support bi-phase format stereo audio data output
- Support 20, 24 bits audio data transfer

- **PCM**
- Include PCM TX and PCM RX, both can work as Master Mode or Slave Mode
- Support Linear PCM (16bit), u-Law (8bit), A-Law (8bit)
- Support clock in Master Mode 2.048MHz, in Slave Mode up to 2.048MHz
- Support Long Frame Sync and Short Frame Sync

- **Ethernet**
- Support 10/100/1000 Mb/s data transfer rate
- Support RGMII/RMII/SMII interface
- Meets the IEEE 802.3 CSMA/CD standard
- Full or half duplex operation
- Flexible address filtering
- Up to 16 physical addresses
- 512 bit hash table for multicast addresses
- Scatter/gather capabilities
- Descriptor "ring" or "chain" structures
- Automatic descriptor list polling
- Clock switching support
- Operates as internal configurable FIFOs
- Programmable transmit threshold levels

- **Key**
- 4*3 Key matrix supported
- Support Parallel Out/Parallel In, Serial Out/Parallel In, Serial Out/Serial In, IO scan Mode
- Support IRQ mode
- Support programmable scan timing

- **PWM**
- 6 independent PWM signal from Hz to MHz
- PWM with 1024-level duty adjustment
- PWM with high level or low level active

1.3.11 Power Management

- Actions' LPD Gen. V (Low Power Design Generation V) architecture integrated
- Actions' ADP(Adaptive Dynamic Power) architecture integrated
- Multiple power domain supported
- Multiple power state supported
- Dynamic internal power adjustment
- Dynamic internal clock adjustment
- High precision temperature sensor is inside
- 3.3V I/O power and 1.0V core power

- **SPS (Smart Power System)**
- 3 separate core voltage domains
- Multiple separate power domains, which can be power up/down by software based on
- Multiple configurable work modes to save power by different frequency or automatically
- clock gating control or power domain on/off control

- Lots of wakeup sources in different mode

1.3.12 Package

- Type: TFBGA 496
- Size: 16mm*16mm
- Ball pitch: 0.65mm
- Ball diameter: 0.35mm

1.4 Application Diagram

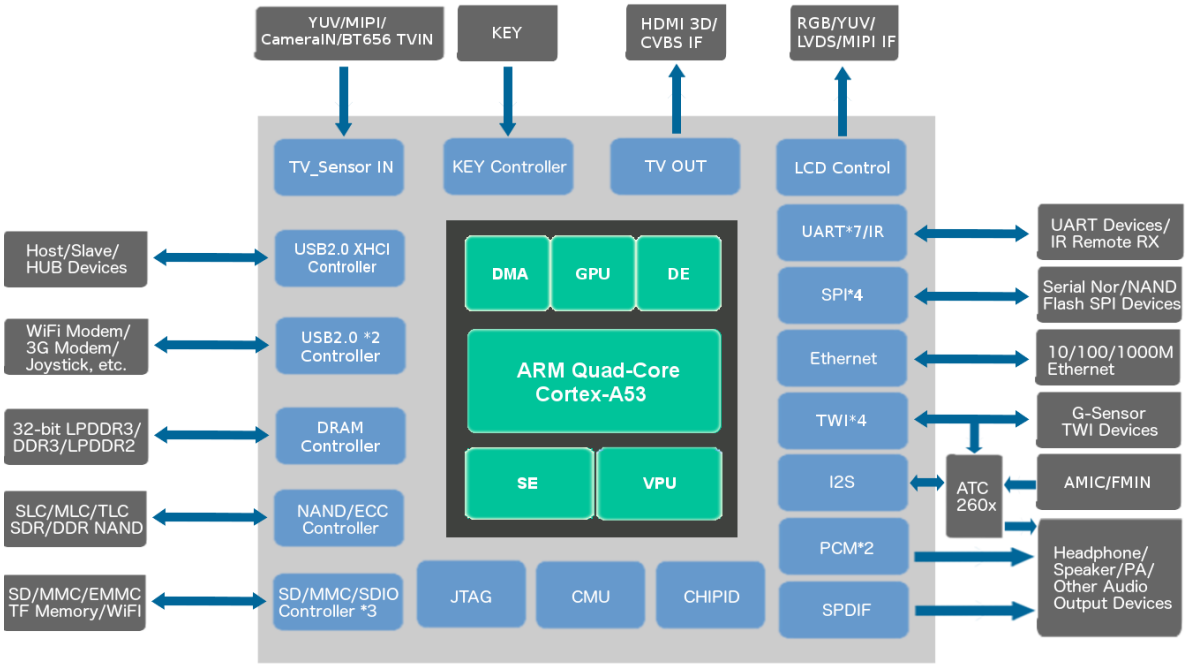
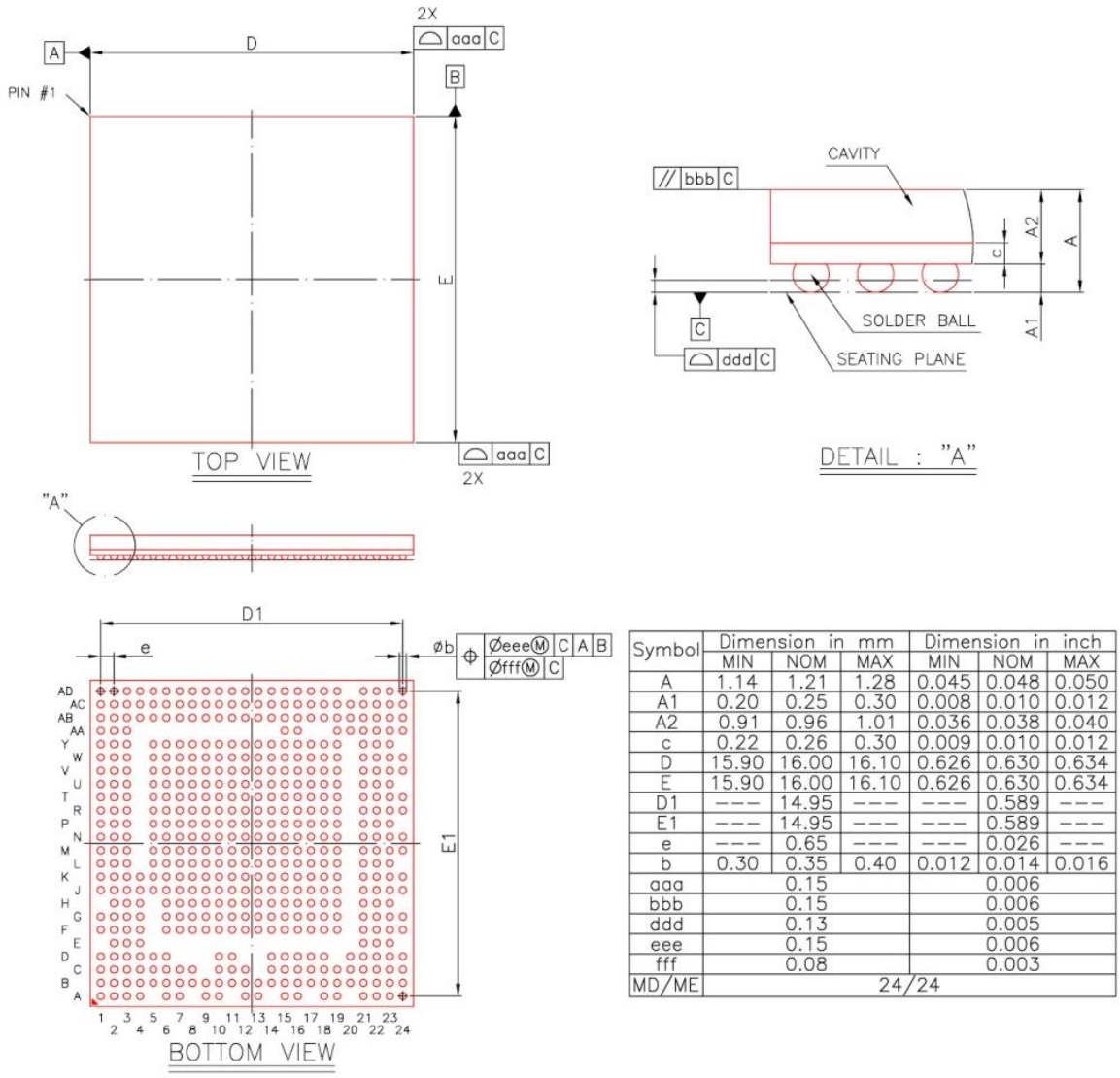


Figure 1-1 Application Diagram

1.5 Package

1.5.1 Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.14	1.21	1.28	0.045	0.048	0.050
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	15.90	16.00	16.10	0.626	0.630	0.634
E	15.90	16.00	16.10	0.626	0.630	0.634
D1	---	14.95	---	---	0.589	---
E1	---	14.95	---	---	0.589	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa		0.15			0.006	
bbb		0.15			0.006	
ddd		0.13			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		24/24				

Figure 1-2 S700 Package Drawing