S500 Datasheet

Version: 1.6

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Revision History

Date	Revision	Description
2015-03-25	1.0	Initial Version
2015-04-21	1.1	Update Sensor Interface
2015-05-28	1.2	Modification on pinlist: Add Table 1-3 and adjust sequence of Table 1-1
2015-07-08	1.3	Correct description mistakes in PWM block
2015-07-17	1.4	Add Example Board Layout figure
2015-11-30	1.5	Add video decoding parameter in feature part
2016-03-07	1.6	Modify POR sequence figure, delete internal signals. Add Ethernet registers.

1 Introduction

1.1 Overview

S500 SoC (System on Chip) is a high performance application processor. It integrates Quad-Core Cortex-A9R4 processor with NEON (advanced SIMD) co-processor and VFPv3 instructions set. PowerVR SGX544 GPU provides the best game experience and Full HD displays. Independent VPU (Video Processing Unit) supports almost full video formats.

S500 provide rich interfaces such as HDMI, USB, SDIO, etc. Bluetooth, WiFi and Displays peripherals are easy and fast to integrate to construct flexible solutions. High performance DDR3/DDR3L/LPDDR2/ LPDDR3 controller and large capacity NAND Flash Controller with 72-bit ECC/Toggle NAND allow engineers to build effective memory system.

Together with Actions' in-house designed companion chip ATC260x which integrated PMU (Power Management Unit) and Audio Codecs together, S500 really makes it the best choice for high performance products with reasonable price.

1.2 Features

1.2.1 Leopard II CPU

- ARM Cortex-A9 R4 CPU
- Low power and efficient multi-core architecture provides effective single-core, dual-core, and quad-core applications
- Fully comply to ARM cortex V7A instruction set 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative integrated
- 512KB L2 Cache, with 16-Way set associative L2 Cache
- Harvard level 1 memory system with MMU (Memory Management Unit)SCU (Snoop Control Unit) interface in charge of memory coherency between the four CPUs
- GIC (General Interrupt Controller) supported
- NEON (advanced SIMD) and VFPv3 D-32 instructions supported, accelerating the performance of multimedia applications such as 3D graphics and image processing
- Supporting VFP (Vector Floating Point) architecture and compliant with the IEEE 754 standard for floating-point calculation
- In-order pipeline with dynamic branch prediction equipped
- Full Coresight debug solution
- ARM TrustZone supported

1.2.2 GPU

- PowerVR SGX544MP
- Industry standard API support – OpenGL-ES 1.1 and 2.0, OpenVG 1.0.1
- Texture support
  - Cube Map
  - Projected Textures
  - Non square Textures
  - Volume Textures
  - Texture Arrays
- Texture Formats
  - RGBA 8888, 565, 1555, 1565
  - Mono chromatic 8, 16, 16f, 32f, 32int
  - Dual channel, 8:8, 16:16, 16f:16f
  - Compressed Textures PVR-TC1, PVR-TC2, ETC1
  - Programmable support for all YUV formats
- Resolution Support
  - Frame buffer max size = 4096*4096
  - Texture max size = 4096*4096
  - Max volume extent = 2048
  - Max texture repeat = 8192

1.2.3 Video Decoder

- Support Real-time video decoder of most popular video formats (some are supported by the 3rd party applications), such as MPEG-4, H.264, etc.
- Support up to 1920*1080p@60fps video decoding
- Error detection and concealment support for all video formats
- With 2D reference data cache to reduce DDR bandwidth
- Output data format is YUV420 semi-planar
- Average data rate 60Mbps, peak rate up to 120Mbps

1.2.4 Video Encoder

- Support video encoder for baseline H.264
- Input data formats:
  - YUV420SP
  - YVU420SP
  - YUV420P
  - ARGB
  - ABGR
  - ARGBA
  - BGRA
  - RGB565
  - BGR565
- Support VBR and CBR
- Max fps is up to 60fps@1920*1080, 5M pixel and 13M pixel
- Video size from 176*144 to 1920*1088
- Support upscale and downscale, from 1/2 to 8
- Low latency data encoder

1.2.5 JPEG Decoder

- Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:4 ,211H, 211V sampling formats
- Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
- JPEG Baseline Decoder size is from 48*48 to 30000*30000 (900Mpixels)
- For Progressive Decoder size is from 48*48 to 8192*8192
- Support JPEG ROI (Region of Image) decode
- Maximum data rate is up to 100 million pixels per second

1.2.6 JPEG Encoder

- Input data format:
  - YUV420sp
  - YVU420sp
  - YUV420P
  - ARGB
  - ABGR
  - ARGBA
  - BGRA
  - RGB565
  - BGR565
- Max data rate up to 70 million pixels per second
- Image size is from 48*48 to 8176*8176
- Support upscale and downscale, from 1⁄2 to 8

1.2.7 System Components

- **DMA**
- There are 12 independent DMA channels in DMA controller
- Data path is supported with memory to memory, memory to peripheral, peripheral to memory
- Support link list transfer type
- Support chain transfer type between different channels
- Support constant fill mode to initial memory
- Support stride mode for frame buffer data transfer
- Support reload mode
- The RW priority of ALL channels can be setting independently
- Support byte align transfer between memory and memory

- **CMU**
- One oscillator with 24MHz clock input and 7 embedded PLLs
- The DDR PLL ,NAND PLL, Display PLL have optional spread-spectrum function to reduce EMS
- clock gating control for individual components

- **Timer**
- 2 on-chip 2Hz controllers and 2 on-chip Timer controllers inside
- Support IRQ mode

- **Interrupt**
- On-chip ARM Generic Interrupt Controller V2.0 support

- Maximum of 5 PPI interrupts for each Cortex-A9 interface and 58 SPI interrupt sources input from different modules
- Maximum of 16 Software Generated Interrupts for each Cortex-A9 processor interface
- Support software-programmable interrupt priority for each interrupt source
- Two separated interrupt outputs (nFIQ and nIRQ) for each processor

- **E-FUSE**
- 256-bit E-FUSE equipped

- **HDCP2 TX**
- Uses industry-standard public-key RSA authentication and AES-128 encryption
- Compliant to HDCP revision 2.1 and 2.0
- Supports repeaters
- Inside Random Number Generator compliant to NIST-SP 800 90
- Inside HMAC-SHA256 block
- Inside Input and Output FIFO for raw and Encryption datum
- Inside TS packet compliant to Blue-Ray and MPEG2 format
- Supports PES portion Encryption mode

1.2.8 Internal Memory

- **BOOT ROM**
- Size : 32KB
- Support boot from the following device:
  - Emmc (SD2 Controller)
  - NAND Flash
  - SD/TF card (SD0 Controller)
  - SPI NOR Flash
  - SPI NAND Flash
- USB driver is inside for firmware upgrade and hardware test

- **SRAM**
- Size : 72KB

1.2.9 External Memory

- **DRAM**
- DDR3 / DDR3L / LPDDR2 / LPDDR3 supported
- up to 2GB supported
- Internal ODT resistance to improve signal integrity
- Programmable input DQS signal calibration option, calibration period is also programmable
- Differential DQS signal to achieve stable data strobe
- Optional ZQ calibration command in programmable period
- Hardware options in DDR state manage to reduce DDR power in some low bandwidth application
- Built-in hardware monitor to improve system debug
- Built-in hardware bandwidth performance counter
- Support more than 4 command processing concurrently in one cycle
- Command reorder in some circumstance to improve bandwidth

- **NAND Flash**

- Support both Async (include LBA NAND) and Sync NAND Flash, up to 4 CEs
- SLC, MLC and TLC NAND Flash support
- Support Toggle DDR NAND V1.0 and Toggle DDR NAND V2.0
- Support Open NAND Flash Interface (ONFI) up to V3.0
- Up to 72bit hardware ECC
- Ready/Busy signal monitor by hardware automatically
- Support sync NAND Flash Interface up to 200MHz
- Support 3.3V and 1.8V VCCQ

- **SD/MMC/EMMC**
- 3 on-chip SD controller inside
- support
  - SD/HCSD/SDXC (SRD50 mode), miniSD
  - microSD
  - memory card
  - MMC/RSMMC/MMCPLUS card
  - INAND
  - MOVINAND
  - eMMC
  - SDIO card
- Support SD 3.0, SDIO 3.0 and MMC 4.5 protocol
- EMMC4.5 supported
- Support 1-bit, 4-bit, 8-bit, bus mode.
- Clock max rate up to 100MHz
- Support IRQ and DMA mode to transmit data
- Contain 512 BYTE SRAM*2
- Read/Write CRC Status Hardware auto checked
- Support Auto multi Block read/write mode
- Support boot mode based on MMC43 SPEC
- Hardware timeout/delay function.
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing
- Built-in pull up resistors for CMD/DAT lines.

1.2.10 Display Subsystem

- **Display Engine:**
- Four video layer
  - ABGR8888, ABGR1555, ARGB8888, RGB565, YUV 4:2:0 planar format, YUV 4:2:0 semi-planar format
  - Video1 Max input 1920*1080
  - Video2~4 Max input 1920*1080
  - 1/4 to 4 scale in horizontal
  - 1/4 to 4 scale in vertical(YUV 4:2:0 planar and YUV 4:2:0 semi-planar)
  - 1/2 to 2 scale in vertical(Other formats)
  - Bicubic or bilinear scaling
  - Brightness, contrast, saturation adjustment
  - Flip in horizontal and vertical
  - 1/2 subsample in horizontal and vertical
- Two cursor Layer
  - ARGB8888
  - Max input 64x64
- Two blender and output path

- Max output 1920*1080
- Alpha blending
- Colorkey
- Dither from 24-bit to 18/16-bit
- Register double buffer
- Gamma correction

- **HDMI**
- Compatible with HDMI 1.4b, HDCP1.1 and DVI 1.0
- Supports most video formats from 480i to 1080p, such as:
  - 640*480p@59.94/60Hz
  - 720*480p@59.94/60Hz
  - 720*576p@50Hz
  - 1280*720p@59.94/60Hz
  - 1280*720p@50Hz
  - 720(1440)*480i@59.94/60Hz
  - 720(1440)*576i@50Hz
  - 1440*480p@59.94/60Hz
  - 1440*576p@50Hz
  - 1920*1080i@59.94/60Hz
  - 1920*1080i@50Hz
  - 1920*1080p@24Hz
  - 1920*1080p@59.94/60Hz
  - 1920*1080p@50Hz
- Supports 24-bit, 30-bit, 36-bit RGB/YCbCr 4:4:4 format (Deep Color)
- Supports xvYCC601, xvYCC709 Enhanced Colorimetry format
- Supports IEC60958 audio format up to 24 bits
- Supports high bit rate compressed audio formats
- Supports up to 8-channel Audio sample, supports 48/96/192/44.2/88.4/176.8kHz audio sample rate
- Supports Auto-Lipsync Correction feature
- Supports 3D Frame Packing Structure up to 1080p@60Hz
- Supports 3D Side-by-Side (Half) Structure with 1080i@59.94/60Hz, 1080i@50Hz, etc.
- Supports 3D Top-and-Bottom Structure with 1080p@24Hz, 720p@50Hz, 720p@59.94/60Hz, etc.

- **LCD Controller**
- Support dual channel LVDS interface LCD
- Support 24-bit RGB interface
- Support MIPI DSI interface
- Programmable timing control for various panels
- Pixel stream input without strict timing requirements
- Resolutions up to 1920*1080
- Maximum 16777216 simultaneous display color
- Fill the empty field when output size is smaller than LCD display size
- Support VBI, HBI, AVSI, FEI (Frame end interrupt)

- **MIPI DSI**
- Compliant with MIPI DSI Specification version 1.01 and the D-PHY specification version 0.9
- Display Resolutions up to 1080p
- Pixel Format:
  - Command Mode: RGB233, RGB444, RGB565, RGB666(Loosely), and RGB888
  - Video Mode: RGB565, RGB666 (Packed), RGB666(Loosely), and RGB888
- Command and Video mode support(type 1,2,3 and 4 display architecture)
- Low power and ultra low power support

- 75 Mbps to 1Gbps per lane
- Support 1-4 data lanes

- **LVDS**
- Comply with the TIA/EIA-644-A LVDS standard
- Support reference clock frequency range from 10MHz to 130MHz
- Support LVDS RGB 24/18 bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, Odd/Even channel Mirror/Swap

1.2.11 CMOS Sensor Interface

- Two CMOS sensor input channels
- Windowing function
- 8-bit data parallel with Hsync, Vsync, Pclk
- DVP/MIPI CSI interface
- YUV input sequence selection and storing format selection
- Max support 5M pixel input

- **MIPI CSI**
- Compliant with MIPI CSI-2 Specification version 1.0 and the D-PHY specification version 0.9
- High-Speed Mode : from 80 Mbps to 1 Gbps synchronous
- Low-Power Mode : spaced one-hot encoding for data
- Ultra low power supported
- Support Data Type : YUV422-8bit
- 1-4 Data Lanes Configurable

1.2.12 Highly-integrated Interfaces

- **USB3**
- Host and Device mode is supported
- Fully compliant with USB Specification 2.0
- Device mode Supports High Speed (480Mb/s) and Full Speed (12Mb/s)
- Host mode Supports USB High Speed, Full Speed and Low Speed
- Supports Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Interface UTMI+(level3)
- Up to 31 devices are supports by the Host
- Supports USB remote wake-up feature
- Host mode is compliant with XHCI architecture
- Downstream hub function is supported

- **USB2*2**
- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- Two independent USB2.0 controllers are inside
- UTMI+ level2 Transceiver Macrocell Interface
- HSIC Interface for an option
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (one series downstream HUB supported)
- Supports full-speed or high-speed in peripheral mode
- Supports 15 IN endpoints and 15 OUT endpoints besides Control endpoint0

- Supports high-speed high-bandwidth isochronous transfer and Interrupt transfer
- Supports suspend, resume and power managements function
- Support remote wakeup
- One OTG function and the other working as either Device or Host

- **UART/IRC**
- 7 on-chip UART controller inside
- 5:8 Data Bits and LSB first in Transmit and Received
- 1:2 Stop Bits
- Even, Odd, or No Parity
- 16 levels Transmit FIFO and 32 levels Receive FIFO
- Capable of speeds up to 3Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Only UART2\3 support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- Only UART0 support IRC(infrared remote control) Inputs
- Support RC6\RC5\9012\NEC(8-bit) protocol
- Need to connect an IR receiver when use
- Support IR Paddle
- The UART3 supports 1.8V/3.3V, configurable

- **TWI**
- 4 on-chip TWI controller inside
- Both master and slave functions support
- Support standard mode (100kbps), fast-speed mode (400kpbs), fast-plus-speed mode (1Mpbs), High-Speed mode (3.4Mbps)
- Multi-master capability
- Internal Pull-Up Resistor (1.5kOhm) optional
- 8-bit*128 TX FIFO and 8-bit*128 RX FIFO

- **SPI**
- 4 on-chip SPI controller inside
- Support master mode and slave mode. The speed of master mode up to 60Mbps, and slaver up to 20Mbps.
- 32-bit*32 TX FIFO and 32-bit*32 RX FIFO
- Support dual I/O write and read mode while use as master
- Support single data rate mode and double data rate (DDR mode) while use as master
- Support two wire mode, only use SCLK and MOSI signal
- Support IRQ and DMA mode to transmit data
- Support system program boot from SPI NOR-Flash

- **Ethernet**
- Supports 10/100 Mb/s data transfer rate
- Supports RMII/SMII interface
- Meets the IEEE 802.3 CSMA/CD standard
- Full or half duplex operation
- Flexible address filtering
- Up to 16 physical addresses
- 512-bit hash table for multicast addresses
- Scatter/gather capabilities
- Descriptor "ring" or "chain" structures
- Automatic descriptor list polling
- Clock switching supported
- Operates as internal configurable FIFOs

- Programmable transmit threshold levels

- **PWM**
- 6 independent PWM signal from 24Hz to 24MHz
- PWM with 1024-level duty adjustment
- PWM with high level or low level active

- **Audio Interface**
- I2S
  - 2 channels (1 TX, 1 RX)
  - Supports 2.0-channel I2S transmitter and receiver
  - Supports 7.1-channel and 5.1-channel through I2S transmitter with ext.8-channel and 6-channel DAC by TDM (Time-Division Multiplexed) Mode
  - Supports 4-channel through I2S receiver, by TDM Mode for 4-channel record
  - Audio data up to 24bits
  - Sample rate up to 192KHz
  - Provides master work mode

- **Key**
- 4*3 Key matrix supported
- Support Parallel Out/Parallel In, Serial Out/Parallel In, Serial Out/Serial In, IO scan Mode;
- Support IRQ mode
- Supports programmable scan timing

1.2.13 OS (Operation System)

- Linux
- Android L

1.2.14 Power

- 3.3V I/O power and 1.0V core power required
- Actions' LPD Gen. IV(Low Power Design Generation IV) architecture integrated
- Actions' ADP(Adaptive Dynamic Power) architecture integrated
- Multiple power domain supported
- Dynamic internal clock adjustment supported
- Multiple standby state supported
- High precision temperature sensor is inside

1.2.15 Package

- Type: TFBGA496
- Size: 16mm*16mm
- Ball pitch: 0.65mm
- Ball diameter: 0.35mm

1.3 Application Diagram

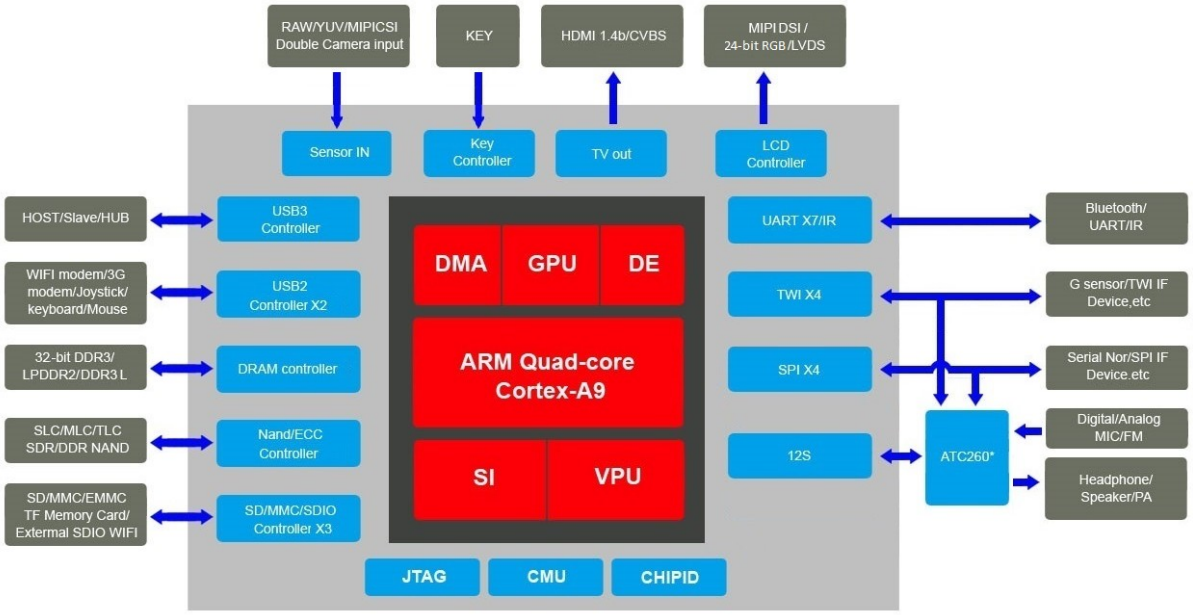


Figure 1-1 S500 Application Diagram

1.4 Pin Description

1.4.1 Pin Order List

Table 1-1 Pin Description

Ball No.	Ball Name	Function Mux	Description
A1	NAND_WRB	NAND_WRB	NAND write enable
A2	NAND_CLE	NAND_CLE	NAND CLE
		SPI2_MOSI	SPI2 MOSI
		GPIOD13	GPIOD13
A3	NAND_CE1B	NAND_CE1B	NAND CE1B
		NAND_CEB1	NAND CEB1
		SPI2_SS	SPI2 SS
		GPIOD15	GPIOD15
A4	NAND_RB	NAND_RB	NAND RB
A6	DSI_DP0	DSI_DP0	MIPI DSI DP0
		SD0_CLKB	SDIO0 CLKB
		SPI0_MISO	SPI0 MISO
		UART2_RX	UART2 RX
		GPIOC6	GPIOC6
A7	DSI_CP	DSI_CP	MIPI DSI CP
		SD1_D1	SDIO1 D1
		GPIOC4	GPIOC4

		LCD0_D1	LCD0 D1
A9	DSI_DP3	DSI_DP3	MIPI DSI DP3
		SD1_CLKB	SDIO1 CLKB
		SD1_CLK	SDIO1 CLK
		GPIOC0	GPIOC0
		LCD0_D16	LCD0 D16
A10	OEN	OEN	LVDS OEN
		GPIOB11	GPIOB11
		LCD0_HSYNC0	LCD HSYNC signal
A12	OBP	OBP	LVDS OBP
		GPIOB16	GPIOB16
		LCD0_D21	LCD D21
A13	OAP	OAP	LVDS OAP
		GPIOB18	GPIOB18
		LCD0_D19	LCD0 D19
A15	EDN	EDN	LVDS EDN
		NOR_D12	NOR Flash D12
		LCD0_D11	LCD D11
		GPIOB23	GPIOB23
A16	ECN	ECN	LVDS ENC
		LCD0_D7	LCD D7
		NOR_A4	NOR Flash A4
		GPIOB25	GPIOB25
A18	TXON2	TXON2	HDMI TXON2
A19	TXON1	TXON1	HDMI TXON1
A21	TPCK	TPCK	HDMI TPCK
A22	HPD	HPD	HDMI HPD
A23	HSIP	HSIP	USB3 HSIP
A24	HSIN	HSIN	USB3 HSIN
B1	NAND_D0	NAND_D0	NAND D0
		SD2_D0	SDIO2 D0
B2	NAND_ALE	NAND_ALE	NAND ALE
		GPIOD12	GPIOD12
		SPI2_MISO	SPI2 MISO
B3	NAND_CE0B	NAND_CE0B	NAND CE0B
		NAND_CEB0	NAND CEB0
		GPIOD14	GPIOD14
		SPI2_SCLK	SPI2 SCLK
B4	NAND_RDB	NAND_RDB	NAND RDB
		SD2_CLK	SDIO2 CLK
B5	DSI_DN2	DSI_DN2	MIPI DSI DN2
		SD1_D1B	SDIO1 D1B
		GPIOC9	GPIOC9
		UART2_CTSB	UART2 CTSB
		SPI0_SS	SPI0 SS
B6	DSI_DN0	DSI_DN0	DSI DN0
		GPIOC7	GPIOC7
		UART2_TX	UART2 TX
		SPI0_MOSI	SPI0 MOSI
B7	DSI_CN	DSI_CN	MIPI DSI CN
		SD1_D0	SDIO D0

		GPIOC5	GPIOC5
		LCD0_D0	LCD0 D0
B8	DSI_DP1	DSI_DP1	MIPI DSI DP1
		SD1_D2	SDIO1 D2
		GPIOC2	GPIOC2
		LCD0_D8	LCD0 D8
B9	DSI_DN3	DSI_DN3	MIPI DSI DN3
		SD1_D3	SDIO1 D3
		GPIOC1	GPIOC1
		LCD0_D9	LCD0 D9
B10	OEP	OEP	LVDS OEP
		LCD0_DCLK0	LCD0 DCLK0
		GPIOB10	GPIOB10
B11	ODN	ODN	LVDS ODN
		LCD0_LDE0	LCD0 LDE0
		GPIOB13	GPIOB13
B12	OCN	OCN	LVDS OCN
		LCD0_D22	LCD0 D22
		GPIOB15	GPIOB15
B13	OAN	OAN	LVDS OAN
		LCD0_D15	LCD0 D15
		GPIOB19	GPIOB19
B14	EEN	EEN	LVDS EEN
		NOR_WR	NOR Flash WR
		LCD0_D13	LCD0 D13
		GPIOB21	GPIOB21
B15	EDP	EDP	LVDS EDP
		NOR_D13	NOR Flash D13
		LCD0_D12	LCD0 D12
		GPIOB22	GPIOB22
B16	EBP	EBP	LVDS EBP
		NOR_D15	NOR Flash D15
		LCD0_D6	LCD0 D6
		GPIOB26	GPIOB26
B17	EAP	EAP	LVDS EAP
		NOR_D9	NOR Flash D9
		LCD0_D4	LCD0 D4
		GPIOB28	GPIOB28
B18	TXOP2	TXOP2	HDMI TXOP1
B19	TXOP1	TXOP1	HDMI TXOP2
B20	TXOP0	TXOP0	HDMI TXOP0
B21	TNCK	TNCK	HDMI TNCK
B22	CEC	CEC	HDMI CEC
B23	HSON	HSON	USB3 HSON
B24	HSOP	HSOP	USB3 HSOP
C1	NAND_D2	NAND_D2	NAND D2
		SD2_D2	SDIO2 D2
C2	NAND_D1	NAND_D1	NAND D1
		SD2_D1	SDIO2 D1
C3	NAND_DQS	NAND_DQS	NAND DQS
		GPIOA12	GPIOA12

C4	NAND_RDBN	NAND_RDBN	NAND RDBN
		SD2_CMD	SDIO2 CMD
C5	NAND_CE3B	NAND_CEB3	NAND CEB3
		GPIOD17	GPIOD17
		PWM4	PWM4
C6	DSI_DP2	DSI_DP2	MIPI DSI DP2
		SD1_CLKB	SDIO1 CLKB
		GPIOC8	GPIOC8
		UART2_RTSB	UART2 RTSB
		SPI0_SCLK	SPI0 SCLK
C7	DVCCIO_DSI	DVCCIO_DSI	MIPI DSI DVCCIO
C8	DSI_DN1	DSI_DN1	MIPI DSI DN1
		LCD0_D2	LCD0 D2
		GPIOC3	GPIOC3
C10	ODP	ODP	LVDS ODP
		LCD0_VSYNC0	LCD0 VSYNC0
		GPIOB12	GPIOB12
C11	OCP	OCP	LVDS OCP
		LCD0_D23	LCD0 D23
		GPIOB14	GPIOB14
C12	OBN	OBN	LVDS OBN
		LCD0_D20	LCD0 D20
		GPIOB17	GPIOB17
C14	EEP	EEP	LVDS EEP
		NOR_RD	NOR Flash RD
		LCD0_D14	LCD0 D14
		GPIOB20	GPIOB20
C15	ECP	ECP	LVDS ECP
		NOR_D11	NOR Flash D11
		LCD0_D10	LCD0 D10
		GPIOB24	GPIOB24
C16	EBN	EBN	LVDS EBN
		NOR_D14	NOR Flash D14
		LCD0_D5	LCD0 D5
		GPIOB27	GPIOB27
C17	EAN	EAN	LVDS EAN
		NOR_D8	NOR Flash D8
		LCD0_D3	LCD0 D3
		GPIOB29	GPIOB29
C18	TMDS_AVCC	TMDS_AVCC	HDMI AVCC
C19	TMDS_AVDD	TMDS_AVDD	HDMI AVDD
C20	TXON0	TXON0	HDMI TXON
C21	USB3_GND	USB3_GND	USB3 Ground
C22	USB3_GND	USB3_GND	USB3 Ground
C23	U3_VBUS0	U3_VBUS0	USB3 VBUS0
C24	U3_IDPIN0	U3_IDPIN0	USB3 IDPIN0
D1	NAND_D3	NAND_D3	NAND D3
		SD2_D3	SDIO2 D3
D2	NAND_DQSN	NAND_DQSN	NAND DQSN
		GPIOA13	GPIOA13
D3	NAND_VSS	NAND_VSS	NAND VSS

D4	NAND_VSS	NAND_VSS	NAND VSS
D5	NAND_VCC	NAND_VCC	NAND VCC
D6	NAND_VCC	NAND_VCC	NAND VCC
D10	AGND_LVDS	AGND_LVDS	LVDS AGND
D11	AVCC_LVDS	AVCC_LVDS	AVCC LVDS
D14	VDD_GPU	VDD_GPU	VDD for GPU
D15	VDD_GPU	VDD_GPU	VDD for GPU
D16	VDD_GPU	VDD_GPU	VDD for GPU
D17	TST_LVDS	TST_LVDS	Test
D18	TMDS_VSS	TMDS_VSS	HDMI TMDS VSS
D20	U2_IDPIN2	U2_IDPIN2	USB2 IDPIN2
D21	PORB	PORB	Power On Reset
D22	USB3_VDDRX	USB3_VDDRX	USB3 VDDRX
D23	U3_DP0	U3_DP0	USB3 DP0
D24	U3_DM0	U3_DM0	USB3 DM0
E2	NAND_D4	NAND_D4	NAND D4
		SD2_D4	SDIO2 D4
E3	NAND_CE2B	NAND_CEB2	NAND CEB2
		PWM5	PWM5
		GPIOD16	GPIOD16
E4	AGND_DAC	AGND_DAC	AGND DAC
E21	VR15	VR15	Vref Voltage
E22	USB3_VDDTX	USB3_VDDTX	USB3 VDDTX
E23	USB3_UVCC	USB3_UVCC	USB3 UVCC
F1	NAND_D7	NAND_D7	NAND D7
		SD2_D7	SDIO2 D7
F2	NAND_D6	NAND_D6	NAND D6
		SD2_D6	SDIO2 D6
F3	NAND_D5	NAND_D5	NAND D5
		SD2_D5	SDIO2 D5
F4	TVCVBS	TVCVBS	TV CVBS
F6	VDD_CORE	VDD_CORE	VDD for Core
F7	VDD_CORE	VDD_CORE	VDD for Core
F8	VDD_CORE	VDD_CORE	VDD for Core
F9	GND	GND	Gound
F10	GND	GND	Gound
F11	GND	GND	Gound
F12	VDD_GPU	VDD_GPU	VDD for GPU
F13	VDD_GPU	VDD_GPU	VDD for GPU
F14	VDD_GPU	VDD_GPU	VDD for GPU
F15	VDD_GPU	VDD_GPU	VDD for GPU
F16	VDD_GPU	VDD_GPU	VDD for GPU
F17	VDD_GPU	VDD_GPU	VDD for GPU
F18	GND	GND	Gound
F19	GND	GND	Gound
F21	HSIC_DQ	HSIC_DQ	USB HSIC DQ
F22	UVCC	UVCC	VCC For USB
F23	U2_DP1	U2_DP1	USB2 DP1
F24	U2_DM1	U2_DM1	USB2 DM1
G1	ETH_TXEN	ETH_TXEN	Ethernet TXEN
		SPI3_SCLK	SPI3 SCLK

		UART2_RX	UART2 RX
		GPIOA16	GPIOA16
		PWM0	PWM0
G2	ETH_REF_CLK	ETH_REF_CLK	Ethernet REF CLK
		SMII_CLK	SMII CLK
		SPI2_MOSI	SPI2 MOSI
		GPIOA21	GPIOA21
		UART4_TX	UART4 TX
G3	ETH_MDIO	ETH_MDIO	Ethernet MDIO
		GPIOA23	GPIOA23
G4	AVCC_DAC	AVCC_DAC	AVCC DAC
G6	VDD_CORE	VDD_CORE	VDD for Core
G7	VDD_CORE	VDD_CORE	VDD for Core
G8	VDD_CORE	VDD_CORE	VDD for Core
G9	GND	GND	Gound
G10	GND	GND	Gound
G11	GND	GND	Gound
G12	VDD_GPU	VDD_GPU	VDD for GPU
G13	VDD_GPU	VDD_GPU	VDD for GPU
G14	VDD_GPU	VDD_GPU	VDD for GPU
G15	VDD_GPU	VDD_GPU	VDD for GPU
G16	VDD_GPU	VDD_GPU	VDD for GPU
G17	VDD_GPU	VDD_GPU	VDD for GPU
G18	GND	GND	Gound
G19	GND	GND	Gound
G21	HSIC_DQS	HSIC_DQS	USB HSIC DQS
G22	USB_GND	USB_GND	USB GND
G23	U2_DP2	U2_DP2	USB2 DP2
G24	U2_DM2	U2_DM2	USB2 DM2
H2	ETH_TXD0	ETH_TXD0	Ethernet TXD0
		SMII_TX	SMII TX
		SPI2_SCLK	SPI2 SCLK
		GPIOA14	GPIOA14
		UART6_RX	UART6 RX
		PWM4	PWM4
H6	VDD_CORE	VDD_CORE	VDD for Core
H7	VDD_CORE	VDD_CORE	VDD for Core
H8	GND	GND	Gound
H9	GND	GND	Gound
H10	GND	GND	Gound
H11	GND	GND	Gound
H12	GND	GND	Gound
H13	GND	GND	Gound
H14	GND	GND	Gound
H15	GND	GND	Gound
H16	GND	GND	Gound
H17	GND	GND	Gound
H18	GND	GND	Gound
H19	GND	GND	Gound
H21	VCCQ_HSIC	VCCQ_HSIC	USB HSIC Power
H22	UAVDD	UAVDD	USB AVDD

H23	U2_VBUS2	U2_VBUS2	USB2 VBUS2
H3	ETH_TXD1	ETH_TXD1	Ethernet TXD1
		SMII_SYNC	SMII SYNC
		SPI2_SS	SPI2 SS
		GPIOA15	GPIOA15
		UART6_TX	UART6 TX
		PWM5	PWM5
H4	ETH_RXER	ETH_RXER	Ethernet RXER
		SPI3_MOSI	SPI3 MOSI
		UART2_TX	UART2 TX
		GPIOA17	GPIOA17
		PWM1	PWM1
J1	ETH_RXD0	ETH_RXD0	Ethernet RXD0
		SPI3_MISO	SPI3 MISO
		UART5_RX	UART5 RX
		UART2_CTSB	UART2 CTSB
		GPIOA20	GPIOA20
		PWM3	PWM3
J2	ETH_RXD1	ETH_RXD1	Ethernet RXD1
		SPI3_SS	SPI3 SS
		UART5_TX	UART5 TX
		UART2_RTSB	UART2 RTSB
		GPIOA19	GPIOA19
		PWM2	PWM2
J3	ETH_MDC	ETH_MDC	Ethernet MDC
		GPIOA22	GPIOA22
J4	ETH_CRS_DV	ETH_CRS_DV	Ethernet CRS DV
		SMII_RX	SMII RX
		SPI2_MISO	SPI2 MISO
		GPIOA18	GPIOA18
		UART4_RX	UART4 RX
		PWM4	PWM4
J5	VDDR	VDDR	VDDR
J6	VDD_CORE	VDD_CORE	VDD for Core
J7	VDD_CORE	VDD_CORE	VDD for Core
J8	GND	GND	Gound
J9	GND	GND	Gound
J10	GND	GND	Gound
J11	GND	GND	Gound
J12	GND	GND	Gound
J13	GND	GND	Gound
J14	GND	GND	Gound
J15	GND	GND	Gound
J16	GND	GND	Gound
J17	GND	GND	Gound
J18	GND	GND	Gound
J19	GND	GND	Gound
J21	KS_OUT0	KS_OUT0	KEY OUT0
		UART5_RX	UART5 RX
		NOR_A9	NOR Flash A9
		PWM2	PWM2

		SD0_CMD	SDIO0 CMD
		GPIOB7	GPIOB7
		SENS1_PCLK	Camera Sensor1 PCLK
J22	AVDD_CMU	AVDD_CMU	AVDD CMU
J23	HOSCI	HOSCI	Crystal input
J24	HOSCO	HOSCO	Crystal output
K1	CS1	CS1	DDR CS1
K2	RET_EN	RET_EN	DDR RET EN
K3	GND	GND	Gound
K4	VDDR	VDDR	VDDR
K5	VDDR	VDDR	VDDR
K6	VDD_CORE	VDD_CORE	VDD for Core
K7	VDD_CORE	VDD_CORE	VDD for Core
K8	GND	GND	Gound
K9	GND	GND	Gound
K10	GND	GND	Gound
K11	GND	GND	Gound
K12	GND	GND	Gound
K13	GND	GND	Gound
K14	GND	GND	Gound
K15	GND	GND	Gound
K16	GND	GND	Gound
K17	GND	GND	Gound
K18	VCC	VCC	VCC
K19	VCC	VCC	VCC
K21	KS_IN3	KS_IN3	KEY IN3
		NOR_A8	NOR Flash A8
		PWM1	PWM1
		GPIOB6	GPIOB6
		SENS1_D7	Camera Sensor1 D7
K22	AVCC_CMU	AVCC_CMU	CMU AVCC
K23	AGND_CMU	AGND_CMU	CMU AGND
K24	CLKO_24M	CLKO_24M	24MHz clock output
		CLKO_25M	25MHz clock output
L1	DQ15	DQ15	DDR DQ15
L2	ZQ	ZQ	DDR ZQ
L3	DQ7	DQ7	DDR DQ7
L5	VDDR	VDDR	VDDR
L6	GND	GND	Gound
L7	GND	GND	Gound
L8	GND	GND	Gound
L9	GND	GND	Gound
L10	GND	GND	Gound
L11	GND	GND	Gound
L12	GND	GND	Gound
L13	GND	GND	Gound
L14	GND	GND	Gound
L15	GND	GND	Gound
L16	GND	GND	Gound
L17	GND	GND	Gound
L18	VCC	VCC	VCC

L19	VCC	VCC	VCC
L21	KS_IN2	KS_IN2	KEY IN2
		NOR_A7	NOR Flash A7
		PWM0	PWM0
		GPIOB5	GPIOB5
		SENS1_D6	Camera Sensor1 D6
L22	KS_OUT1	KS_OUT1	KEY OUT1
		NOR_A10	NOR Flash A10
		PWM3	PWM3
		SD0_CLK	SDIO0 CLK
		GPIOB8	GPIOB8
		SENS1_VSYNC	Camera Sensor1 VSYNC
L23	KS_OUT2	KS_OUT2	KEY OUT2
		UART5_TX	UART5 TX
		SD0_D1B	SDIO0 D1B
		NOR_A11	NOR Flash A11
		PWM2	PWM2
		GPIOB9	GPIOB9
		SENS1_HSYNC	Camera Sensor1 HSYNC
M1	DQ14	DQ14	DDR DQ14
M2	DQ13	DQ13	DDR DQ13
M3	DQ6	DQ6	DDR DQ6
M5	VDDR	VDDR	VDDR
M6	GND	GND	Gound
M7	GND	GND	Gound
M8	GND	GND	Gound
M9	GND	GND	Gound
M10	GND	GND	Gound
M11	GND	GND	Gound
M12	GND	GND	Gound
M13	GND	GND	Gound
M14	GND	GND	Gound
M15	GND	GND	Gound
M16	GND	GND	Gound
M17	GND	GND	Gound
M18	GND	GND	Gound
M19	GND	GND	Gound
M21	KS_IN1	KS_IN1	KEY IN1
		NOR_A6	NOR Flash A6
		PWM1	PWM1
		DRV_VBUS0	DRV VBUS0
		GPIOB4	GPIOB4
		SENS1_D5	Camera Sensor1 D5
		PWM5	PWM5
M22	SR0_DATA6	SR0_DATA6	Camera Sensor0 DATA6
M23	SR0_DATA7	SR0_DATA7	Camera Sensor0 DATA7
M24	SR0_DATA5	SR0_DATA5	Camera Sensor0 DATA5
N1	DQS1	DQS1	DDR DQS1
N2	DQS1#	DQS1#	DDR DQS1#
N3	DQ5	DQ5	DDR DQ5
N5	VDDR	VDDR	VDDR

N6	GND	GND	Gound
N7	GND	GND	Gound
N8	GND	GND	Gound
N9	GND	GND	Gound
N10	GND	GND	Gound
N11	GND	GND	Gound
N12	GND	GND	Gound
N13	GND	GND	Gound
N14	GND	GND	Gound
N15	GND	GND	Gound
N16	GND	GND	Gound
N17	GND	GND	Gound
N19	TST_CMU	TST_CMU	Test
N18	VCCIO	VCCIO	VCCIO
N19	NC	NC	NC
N21	KS_IN0	KS_IN0	KEY IN0
		NOR_A5	NOR Flash A5
		PWM0	PWM0
		GPIOB3	GPIOB3
		SENS1_D4	Camera Sensor1 D4
		PWM4	PWM4
N22	SR0_HSYNC	SR0_HSYNC	Camera Sensor0 HSYNC
N23	SR0_DATA4	SR0_DATA4	Camera Sensor0 DATA4
N24	SR0_VSYNC	SR0_VSYNC	Camera Sensor0 VSYNC
P1	DQ12	DQ12	DDR DQ12
P2	DQ11	DQ11	DDR DQ11
P3	DQS0	DQS0	DDR DQS0
P5	GND	GND	Gound
P6	GND	GND	Gound
P7	GND	GND	Gound
P8	GND	GND	Gound
P9	GND	GND	Gound
P10	GND	GND	Gound
P11	GND	GND	Gound
P12	GND	GND	Gound
P13	GND	GND	Gound
P14	GND	GND	Gound
P15	GND	GND	Gound
P16	GND	GND	Gound
P17	GND	GND	Gound
P18	VDD_CPU	VDD_CPU	VDD for CPU
P19	VDD_CPU_FB	VDD_CPU_FB	VDD CPU Feed back
P21	AVDD_CSI	AVDD_CSI	MIPI CSI AVDD
P22	SR0_DATA3	SR0_DATA3	Camera Sensor0 DATA3
P23	SR0_DATA2	SR0_DATA2	Camera Sensor0 DATA2
R1	DQ10	DQ10	DDR DQ10
R2	DQM1	DQM1	DDR DQM1
R3	DQS0#	DQS0#	DDR DQS0#
R5	GND	GND	Gound
R6	GND	GND	Gound
R7	GND	GND	Gound

R8	GND	GND	Gound
R9	GND	GND	Gound
R10	GND	GND	Gound
R11	GND	GND	Gound
R12	GND	GND	Gound
R13	GND	GND	Gound
R14	GND	GND	Gound
R15	GND	GND	Gound
R16	GND	GND	Gound
R17	GND	GND	Gound
R18	VDD_CPU	VDD_CPU	VDD for CPU
R19	LCD0_D17	LCD0_D17	LCD0 D17
		SD0_CLKB	SDIO0 CLKB
		SD1_CMD	SDIO1 CMD
		GPIOB31	GPIOB31
		NOR_A0	NOR Flash A0
		PWM3	PWM3
R21	AVCC_CSI	AVCC_CSI	MIPI CSI AVCC
R22	SR0_PCLK	SR0_PCLK	Camera Sensor0 PCLK
		NOR_A3	NOR Flash A3
		GPIOC31	GPIOC31
		PWM0	PWM0
R23	SR0_DATA0	SR0_DATA0	Camera Sensor0 DATA0
R24	SR0_DATA1	SR0_DATA1	Camera Sensor0 DATA1
T1	DQ8	DQ8	DDR DQ8
T2	DQ9	DQ9	DDR DQ9
T3	DQ4	DQ4	DDR DQ4
T5	GND	GND	Gound
T6	GND	GND	Gound
T7	GND	GND	Gound
T8	GND	GND	Gound
T9	GND	GND	Gound
T10	GND	GND	Gound
T11	GND	GND	Gound
T12	GND	GND	Gound
T13	GND	GND	Gound
T14	GND	GND	Gound
T15	GND	GND	Gound
T16	GND	GND	Gound
T17	GND	GND	Gound
T18	VDD_CPU	VDD_CPU	VDD for CPU
T19	LCD0_D18	LCD0_D18	LCD0 D18
		GPIOB30	GPIOB30
		NOR_A2	NOR Flash A2
		SENS1_CLKOUT	Camera Sensor1 CLKOUT
		PWM2	PWM2
		PWM4	PWM4
T21	SR0_CKOUT	SR0_CKOUT	Camera Sensor0 CKOUT
		NOR_D10	NOR Flash D10
		GPIOD10	GPIOD10
		SENS1_CLKOUT	Camera Sensor1 CLKOUT

		PWM1	PWM1
T22	SD1_CMD	SD1_CMD	SDIO1 CMD
		NOR_CEB0_7	NOR Flash CEB0 7
		GPIOC20	GPIOC20
T23	SD0_D6	SD0_D6	SDIO0 D6
		NOR_D6	NOR Flash D6
		SD1_D2	SDIO1 D2
		GPIOC16	GPIOC16
T24	SD0_D7	SD0_D7	SDIO0 D7
		NOR_D7	NOR Flash D7
		SD1_D3	SDIO1 D3
		GPIOC17	GPIOC17
U1	A13	A13	DDR A13
U2	A7	A7	DDR A7
U3	DQ3	DQ3	DDR DQ3
U5	VDDR	VDDR	VDDR
U6	VDDR	VDDR	VDDR
U7	GND	GND	Gound
U8	GND	GND	Gound
U9	GND	GND	Gound
U10	GND	GND	Gound
U11	GND	GND	Gound
U12	GND	GND	Gound
U13	GND	GND	Gound
U14	GND	GND	Gound
U15	GND	GND	Gound
U16	GND	GND	Gound
U17	GND	GND	Gound
U18	VDD_CPU	VDD_CPU	VDD for CPU
U19	VDD_CPU	VDD_CPU	VDD for CPU
U21	SIRQ2	SIRQ2	SIRQ2 Interrupt
		GPIOA26	GPIOA26
U22	SD0_D4	SD0_D4	SDIO0 D4
		NOR_D4	NOR Flash D4
		SD1_D0	SDIO1 D0
		GPIOC14	GPIOC14
U23	SD1_CLK	SD1_CLK	SDIO1 CLK
		GPIOC21	GPIOC21
V1	A9	A9	DDR A9
V2	A5	A5	DDR A5
V3	DQ2	DQ2	DDR DQ2
V5	VDDR	VDDR	VDDR
V6	VDDR	VDDR	VDDR
V7	GND	GND	Gound
V8	GND	GND	Gound
V9	GND	GND	Gound
V10	GND	GND	Gound
V11	GND	GND	Gound
V12	GND	GND	Gound
V13	GND	GND	Gound
V14	GND	GND	Gound

V15	GND	GND	Gound
V16	GND	GND	Gound
V17	GND	GND	Gound
V18	VDD_CPU	VDD_CPU	VDD for CPU
V19	VDD_CPU	VDD_CPU	VDD for CPU
V21	SIRQ1	SIRQ1	SIRQ1 Interrupt
		GPIOA25	GPIOA25
V22	SIRQ0	SIRQ0	SIRQ0 Interrupt
		GPIOA24	GPIOA24
V23	SD0_D5	SD0_D5	SDIO0 D5
		NOR_D5	NOR Flash D5
		SD1_D1	SDIO1 D1
		GPIOC15	GPIOC15
V24	SD0_D2	SD0_D2	SDIO0 D2
		NOR_D2	NOR Flash D2
		UART2_RTSB	UART2 RTSB
		UART1_TX	UART1 TX
		GPIOC12	GPIOC12
W1	A4	A4	DDR A4
W2	A0	A0	DDR A0
W3	DQM0	DQM0	DDR DQM0
W5	VDDR	VDDR	VDDR
W6	VDDR	VDDR	VDDR
W7	VDDR	VDDR	VDDR
W8	VDDR	VDDR	VDDR
W9	GND	GND	Gound
W10	GND	GND	Gound
W11	GND	GND	Gound
W12	GND	GND	Gound
W13	GND	GND	Gound
W14	GND	GND	Gound
W15	GND	GND	Gound
W16	VDD_CPU	VDD_CPU	VDD for CPU
W17	VDD_CPU	VDD_CPU	VDD for CPU
W18	VDD_CPU	VDD_CPU	VDD for CPU
W19	VDD_CPU	VDD_CPU	VDD for CPU
W21	PCM1_OUT	PCM1_OUT	PCM1 OUT
		GPIOD31	GPIOD31
		SENS1_D0	Camera Sensor1 D0
		UART6_TX	UART6 TX
		TWI3_SDATA	TWI3 SDATA
W22	SD0_CLK	SD0_CLK	SDIO0 CLK
		GPIOC19	GPIOC19
W23	SD0_D3	SD0_D3	SDIO0 D3
		NOR_D3	NOR Flash D3
		UART2_CTSB	UART2 CTSB
		UART1_RX	UART1 RX
		GPIOC13	GPIOC13
W24	SD0_CMD	SD0_CMD	SDIO0 CMD
		NOR_A1	NOR Flash A1
		GPIOC18	GPIOC18

Y1	BA2	BA2	DDR BA2
Y2	BA0	BA0	DDR BA0
Y3	DQ1	DQ1	DDR DQ1
Y5	VDDR	VDDR	VDDR
Y6	VDDR	VDDR	VDDR
Y7	VDDR	VDDR	VDDR
Y8	VDDR	VDDR	VDDR
Y9	GND	GND	Gound
Y10	GND	GND	Gound
Y11	GND	GND	Gound
Y12	GND	GND	Gound
Y13	GND	GND	Gound
Y14	GND	GND	Gound
Y15	GND	GND	Gound
Y16	VDD_CPU	VDD_CPU	VDD for CPU
Y17	VDD_CPU	VDD_CPU	VDD for CPU
Y18	VDD_CPU	VDD_CPU	VDD for CPU
Y19	VDD_CPU	VDD_CPU	VDD for CPU
Y21	PCM1_CLK	PCM1_CLK	PCM1 CLK
		GPIOD29	GPIOD29
		SENS1_D2	Camera Sensor1 D2
		UART4_TX	UART4 TX
		PWM5	PWM5
Y22	SD0_D1	SD0_D1	SDIO0 D1
		NOR_D1	NOR Flash D1
		UART2_TX	UART2 TX
		UART5_TX	UART5 TX
		GPIOC11	GPIOC11
Y23	SD0_D0	SD0_D0	SDIO0 D0
		NOR_D0	NOR Flash D0
		UART2_RX	UART2 RX
		UART5_RX	UART5 RX
		GPIOC10	GPIOC10
AA1	A15	A15	DDR A15
AA2	CS0	CS0	DDR CS0
AA3	DQ0	DQ0	DDR DQ0
AA15	VDDR	VDDR	VDDR
AA16	VDDR	VDDR	VDDR
AA19	SPI0_MOSI	SPI0_MOSI	SPI0 MOSI
		NOR Flash A15	NOR Flash A15
		GPIOC25	GPIOC25
		TWI3_SDATA	TWI3 SDATA
		PCM0_SYNC	PCM0 SYNC
AA20	VSD_PAD	VSD_PAD	SD3.0 Power
AA21	PCM1_IN	PCM1_IN	PCM1 IN
		GPIOD28	GPIOD28
		SENS1_D3	Camera Sensor1 D3
		UART4_RX	UART4 RX
		PWM4	PWM4
AA22	PCM1_SYNC	PCM1_SYNC	PCM1 SYNC
		GPIOD30	GPIOD30

		SENS1_D1	Camera Sensor1 D1
		UART6_RX	UART6 RX
		TWI3_SCLK	TWI3 SCLK
AA23	TWI0_SCLK	TWI0_SCLK	TWI0 SCLK
		UART2_RTSB	UART2 RTSB
		TWI1_SCLK	TWI1 SCLK
		UART1_TX	UART1 TX
		SPI1_SCLK	SPI1 SCLK
		GPIOC28	GPIOC28
AA24	TWI0_SDATA	TWI0_SDATA	TWI0 SDATA
		UART2_CTSB	UART2 CTSB
		TWI1_SDATA	TWI1 SDATA
		UART1_RX	UART1 RX
		SPI1_MOSI	SPI1 MOSI
		GPIOC29	GPIOC29
AB1	ODT0	ODT0	DDR ODT0
AB2	CAS#	CAS#	DDR CAS#
AB3	GND	GND	Gound
AB4	DDR_VREF	DDR_VREF	DDR VREF
AB5	DQ30	DQ30	DDR DQ30
AB6	DQ29	DQ29	DDR DQ29
AB7	DQ28	DQ28	DDR DQ28
AB8	DQS3	DQS3	DDR DQS3
AB9	DQS3#	DQS3#	DDR DQS3#
AB10	DQ27	DQ27	DDR DQ27
AB11	DQ26	DQ26	DDR DQ26
AB12	DQ31	DQ31	DDR DQ31
AB13	DQM3	DQM3	DDR DQM3
AB14	DQ24	DQ24	DDR DQ24
AB15	VDDR	VDDR	VDDR
AB16	VDDR	VDDR	VDDR
AB17	I2S_D1	I2S_D1	I2S D1
		NOR_A20	NOR Flash A20
		GPIOA31	GPIOA31
AB18	SPI0_SCLK	SPI0_SCLK	SPI0 SCLK
		NOR_A12	NOR Flash A12
		GPIOC22	GPIOC22
		TWI3_SCLK	TWI3 SCLK
		PCM0_CLK	PCM0 CLK
AB19	SPI0_MISO	SPI0_MISO	SPI0 MISO
		NOR_A14	NOR Flash A14
		GPIOC24	GPIOC24
		I2S_MCLK1	I2S MCLK1
		PCM1_IN	PCM1 IN
		PCM0_IN	PCM0 IN
AB20	TWI1_SDATA	TWI1_SDATA	TWI1 SDATA
		GPIOE1	GPIOE1
AB21	UART2_CTSB	UART2_CTSB	UART2 CTSB
		UART0_TX	UART0 TX
		GPIOD21	GPIOD21
AB22	UART2_RTSB	UART2_RTSB	UART2 RTSB

		UART0_RX	UART0 RX
		GPIOD20	GPIOD20
AB23	TWI2_SCLK	TWI2_SCLK	TWI2 SCLK
		GPIOE2	GPIOE2
AB24	TWI2_SDATA	TWI2_SDATA	TWI2 SDATA
		GPIOE3	GPIOE3
AC1	ODT1	ODT1	DDR ODT1
AC2	RAS#	RAS#	DDR RAS#
AC3	CKE1	CKE1	DDR CKE1
AC4	A10	A10	DDR A10
AC5	BA1	BA1	DDR BA1
AC6	A1	A1	DDR A1
AC7	A11	A11	DDR A11
AC8	A6	A6	DDR A6
AC9	DQ22	DQ22	DDR DQ22
AC10	DQ21	DQ21	DDR DQ21
AC11	DQS2#	DQS2#	DDR DQS2#
AC12	DQ19	DQ19	DDR DQ19
AC13	DQM2	DQM2	DDR DQM2
AC14	DQ16	DQ16	DDR DQ16
AC15	GND	GND	Gound
AC16	I2S_BCLK0	I2S_BCLK0	I2S BCLK0
		PCM0_IN	PCM0 IN
		GPIOA28	GPIOA28
		NOR_A17	NOR Flash A17
AC17	I2S_MCLK0	I2S_MCLK0	I2S MCLK0
		GPIOA30	GPIOA30
		PCM1_CLK	PCM1 CLK
		NOR_A19	NOR Flash A19
AC18	I2S_LRCLK1	I2S_LRCLK1	I2S LRCLK1
		PCM0_CLK	PCM0 CLK
		GPIOB1	GPIOB1
		NOR_A22	NOR Flash A22
AC19	SPI0_SS	SPI0_SS	SPI0 SS
		NOR_A13	NOR Flash A13
		GPIOC23	GPIOC23
		I2S_LRCLK1	I2S LRCLK1
		PCM1_OUT	PCM1 OUT
		PCM0_OUT	PCM0 OUT
AC20	TWI1_SCLK	TWI1_SCLK	TWI1 SCLK
		GPIOE0	GPIOE0
AC21	UART2_RX	UART2_RX	UART2 RX
		GPIOD18	GPIOD18
AC22	UART0_RX	UART0_RX	UART0 RX
		UART2_RX	UART2 RX
		SPI1_MISO	SPI1 MISO
		TWI0_SDATA	TWI0 SDATA
		GPIOC26	GPIOC26
		PCM1_IN	PCM1 IN
		I2S_MCLK1	I2S MCLK1
AC23	UART3_RTSB	UART3_RTSB	UART3 RTSB

		UART5_RX	UART5 RX
		GPIOD24	GPIOD24
AC24	UART3_CTSB	UART3_CTSB	UART3 CTSB
		UART5_TX	UART5 TX
		GPIOD25	GPIOD25
AD1	CK	CK	DDR CK
AD2	CK#	CK#	DDR CK#
AD3	CKE0	CKE0	DDR CKE0
AD4	WE#	WE#	DDR WE#
AD5	A12	A12	DDR A12
AD6	A3	A3	DDR A3
AD7	A2	A2	DDR A2
AD8	A14	A14	DDR A14
AD9	A8	A8	DDR A8
AD10	DQ23	DQ23	DDR DQ23
AD11	DQS2	DQS2	DDR DQS2
AD12	DQ20	DQ20	DDR DQ20
AD13	DQ18	DQ18	DDR DQ18
AD14	DQ17	DQ17	DDR DQ17
AD15	DQ25	DQ25	DDR DQ25
AD16	I2S_D0	I2S_D0	I2S D0
		NOR_A16	NOR Flash A16
		GPIOA27	GPIOA27
AD17	I2S_LRCLK0	I2S_LRCLK0	I2S LRCLK0
		GPIOA29	GPIOA29
		PCM1_SYNC	PCM1 SYNC
		NOR_A18	NOR Flash A18
AD18	I2S_BCLK1	I2S_BCLK1	I2S BCLK1
		PCM0_OUT	PCM0 OUT
		GPIOB0	GPIOB0
		NOR_A21	NOR Flash A21
AD19	I2S_MCLK1	I2S_MCLK1	I2S MCLK1
		PCM0_SYNC	PCM0 SYNC
		GPIOB2	GPIOB2
		NOR_A23	NOR Flash A23
AD21	UART2_TX	UART2_TX	UART2 TX
		GPIOD19	GPIOD19
AD22	UART0_TX	UART0_TX	UART0 TX
		UART2_TX	UART2 TX
		SPI1_SS	SPI1 SS
		TWI0_SCLK	TWI0 SCLK
		SPDIF	SPDIF
		GPIOC27	GPIOC27
		PCM1_OUT	PCM1 OUT
		I2S_LRCLK1	I2S LRCLK1
AD23	UART3_RX	UART3_RX	UART3 RX
		GPIOD22	GPIOD22
AD24	UART3_TX	UART3_TX	UART3 TX
		GPIOD23	GPIOD23

1.4.2 Function Block Pin Description

This chapter will give the pin description list in manner of function block, note that some pins are multiplexed, so please pay attention to the multiplexd state before use.

Table 1-2 Function Block Pin Description

Function Block	BGA No.	Pin Name	Function Mux	GPIO Initial State	Description
Clock	K24	CLKO_24M	CLKO_24M		24MHz clock output
	K24	CLKO_24M	CLKO_25M		25MHz clock output
	J23	HOSCI	HOSCI		Crystal input
	J24	HOSCO	HOSCO		Crystal output
System Control	D21	PORB	PORB		Power On Reset
	V22	SIRQ0	SIRQ0		SIRQ0 Interrupt
	V21	SIRQ1	SIRQ1		SIRQ1 Interrupt
	U21	SIRQ2	SIRQ2		SIRQ2 Interrupt
Camera	T21	SR0_CKOUT	SR0_CKOUT		Camera Sensor0 CKOUT
	R23	SR0_DATA0	SR0_DATA0		Camera Sensor0 DATA0
	R24	SR0_DATA1	SR0_DATA1		Camera Sensor0 DATA1
	P23	SR0_DATA2	SR0_DATA2		Camera Sensor0 DATA2
	P22	SR0_DATA3	SR0_DATA3		Camera Sensor0 DATA3
	N23	SR0_DATA4	SR0_DATA4		Camera Sensor0 DATA4
	M24	SR0_DATA5	SR0_DATA5		Camera Sensor0 DATA5
	M22	SR0_DATA6	SR0_DATA6		Camera Sensor0 DATA6
	M23	SR0_DATA7	SR0_DATA7		Camera Sensor0 DATA7
	N22	SR0_HSYNC	SR0_HSYNC		Camera Sensor0 HSYNC
	R22	SR0_PCLK	SR0_PCLK		Camera Sensor0 PCLK
	N24	SR0_VSYNC	SR0_VSYNC		Camera Sensor0 VSYNC
	T19	LCD0_D18	SENS1_CLKOUT		Camera Sensor1 CLKOUT
	T21	SR0_CKOUT	SENS1_CLKOUT		Camera Sensor1 CLKOUT
	W21	PCM1_OUT	SENS1_D0		Camera Sensor1 D0
	AA22	PCM1_SYNC	SENS1_D1		Camera Sensor1 D1
	Y21	PCM1_CLK	SENS1_D2		Camera Sensor1 D2
	AA21	PCM1_IN	SENS1_D3		Camera Sensor1 D3
	N21	KS_IN0	SENS1_D4		Camera Sensor1 D4
	M21	KS_IN1	SENS1_D5		Camera Sensor1 D5
	L21	KS_IN2	SENS1_D6		Camera Sensor1 D6
	K21	KS_IN3	SENS1_D7		Camera Sensor1 D7
	L23	KS_OUT2	SENS1_HSYNC		Camera Sensor1 HSYNC
	J21	KS_OUT0	SENS1_PCLK		Camera Sensor1 PCLK
	L22	KS_OUT1	SENS1_VSYNC		Camera Sensor1 VSYNC
DDR	W2	A0	A0		DDR A0
	AC6	A1	A1		DDR A1
	AC4	A10	A10		DDR A10
	AC7	A11	A11		DDR A11
	AD5	A12	A12		DDR A12
	U1	A13	A13		DDR A13
	AD8	A14	A14		DDR A14
	AA1	A15	A15		DDR A15

	AD7	A2	A2		DDR A2
	AD6	A3	A3		DDR A3
	W1	A4	A4		DDR A4
	V2	A5	A5		DDR A5
	AC8	A6	A6		DDR A6
	U2	A7	A7		DDR A7
	AD9	A8	A8		DDR A8
	V1	A9	A9		DDR A9
	Y2	BA0	BA0		DDR BA0
	AC5	BA1	BA1		DDR BA1
	Y1	BA2	BA2		DDR BA2
	AB2	CAS#	CAS#		DDR CAS#
	AD1	CK	CK		DDR CK
	AD2	CK#	CK#		DDR CK#
	AD3	CKE0	CKE0		DDR CKE0
	AC3	CKE1	CKE1		DDR CKE1
	AA2	CS0	CS0		DDR CS0
	K1	CS1	CS1		DDR CS1
	AA3	DQ0	DQ0		DDR DQ0
	Y3	DQ1	DQ1		DDR DQ1
	R1	DQ10	DQ10		DDR DQ10
	P2	DQ11	DQ11		DDR DQ11
	P1	DQ12	DQ12		DDR DQ12
	M2	DQ13	DQ13		DDR DQ13
	M1	DQ14	DQ14		DDR DQ14
	L1	DQ15	DQ15		DDR DQ15
	AC14	DQ16	DQ16		DDR DQ16
	AD14	DQ17	DQ17		DDR DQ17
	AD13	DQ18	DQ18		DDR DQ18
	AC12	DQ19	DQ19		DDR DQ19
	V3	DQ2	DQ2		DDR DQ2
	AD12	DQ20	DQ20		DDR DQ20
	AC10	DQ21	DQ21		DDR DQ21
	AC9	DQ22	DQ22		DDR DQ22
	AD10	DQ23	DQ23		DDR DQ23
	AB14	DQ24	DQ24		DDR DQ24
	AD15	DQ25	DQ25		DDR DQ25
	AB11	DQ26	DQ26		DDR DQ26
	AB10	DQ27	DQ27		DDR DQ27
	AB7	DQ28	DQ28		DDR DQ28
	AB6	DQ29	DQ29		DDR DQ29
	U3	DQ3	DQ3		DDR DQ3
	AB5	DQ30	DQ30		DDR DQ30
	AB12	DQ31	DQ31		DDR DQ31
	T3	DQ4	DQ4		DDR DQ4
	N3	DQ5	DQ5		DDR DQ5

	M3	DQ6	DQ6		DDR DQ6
	L3	DQ7	DQ7		DDR DQ7
	T1	DQ8	DQ8		DDR DQ8
	T2	DQ9	DQ9		DDR DQ9
	W3	DQM0	DQM0		DDR DQM0
	R2	DQM1	DQM1		DDR DQM1
	AC13	DQM2	DQM2		DDR DQM2
	AB13	DQM3	DQM3		DDR DQM3
	P3	DQS0	DQS0		DDR DQS0
	R3	DQS0#	DQS0#		DDR DQS0#
	N1	DQS1	DQS1		DDR DQS1
	N2	DQS1#	DQS1#		DDR DQS1#
	AD11	DQS2	DQS2		DDR DQS2
	AC11	DQS2#	DQS2#		DDR DQS2#
	AB8	DQS3	DQS3		DDR DQS3
	AB9	DQS3#	DQS3#		DDR DQS3#
	AB1	ODT0	ODT0		DDR ODT0
	AC1	ODT1	ODT1		DDR ODT1
	AC2	RAS#	RAS#		DDR RAS#
	K2	RET_EN	RET_EN		DDR RET EN
	AB4	DDR_VREF	DDR_VREF		DDR VREF
	AD4	WE#	WE#		DDR WE#
	L2	ZQ	ZQ		DDR ZQ
Ethernet	J4	ETH_CRS_DV	ETH_CRS_DV		Ethernet CRS DV
	J3	ETH_MDC	ETH_MDC		Ethernet MDC
	G3	ETH_MDIO	ETH_MDIO		Ethernet MDIO
	G2	ETH_REF_CLK	ETH_REF_CLK		Ethernet REF CLK
	J1	ETH_RXD0	ETH_RXD0		Ethernet RXD0
	J2	ETH_RXD1	ETH_RXD1		Ethernet RXD1
	H4	ETH_RXER	ETH_RXER		Ethernet RXER
	H2	ETH_TXD0	ETH_TXD0		Ethernet TXD0
	H3	ETH_TXD1	ETH_TXD1		Ethernet TXD1
	G1	ETH_TXEN	ETH_TXEN		Ethernet TXEN
HDMI	C18	TMDS_AVCC	TMDS_AVCC		HDMI AVCC
	C19	TMDS_AVDD	TMDS_AVDD		HDMI AVDD
	B22	CEC	CEC		HDMI CEC
	A22	HPD	HPD		HDMI HPD
	D18	TMDS_VSS	TMDS_VSS		HDMI TMDS VSS
	B21	TNCK	TNCK		HDMI TNCK
	A21	TPCK	TPCK		HDMI TPCK
	C20	TXON0	TXON0		HDMI TXON
	A19	TXON1	TXON1		HDMI TXON1
	A18	TXON2	TXON2		HDMI TXON2
	B20	TXOP0	TXOP0		HDMI TXOP0
	B18	TXOP2	TXOP2		HDMI TXOP1
	B19	TXOP1	TXOP1		HDMI TXOP2
I2S	AC16	I2S_BCLK0	I2S_BCLK0		I2S BCLK0
	AD18	I2S_BCLK1	I2S_BCLK1		I2S BCLK1

	AD16	I2S_D0	I2S_D0		I2S D0
	AB17	I2S_D1	I2S_D1		I2S D1
	AD17	I2S_LRCLK0	I2S_LRCLK0		I2S LRCLK0
	AC18	I2S_LRCLK1	I2S_LRCLK1		I2S LRCLK1
	AC19	SPI0_SS	I2S_LRCLK1		I2S LRCLK1
	AD22	UART0_TX	I2S_LRCLK1		I2S LRCLK1
	AC17	I2S_MCLK0	I2S_MCLK0		I2S MCLK0
	AB19	SPI0_MISO	I2S_MCLK1		I2S MCLK1
	AC22	UART0_RX	I2S_MCLK1		I2S MCLK1
	AD19	I2S_MCLK1	I2S_MCLK1		I2S MCLK1
SPDIF	AD22	UART0_TX	SPDIF		SPDIF
KEY	N21	KS_IN0	KS_IN0		KEY IN0
	M21	KS_IN1	KS_IN1		KEY IN1
	L21	KS_IN2	KS_IN2		KEY IN2
	K21	KS_IN3	KS_IN3		KEY IN3
	J21	KS_OUT0	KS_OUT0		KEY OUT0
	L22	KS_OUT1	KS_OUT1		KEY OUT1
	L23	KS_OUT2	KS_OUT2		KEY OUT2
LCD	A15	EDN	LCD0_D11		LCD D11
	A12	OBP	LCD0_D21		LCD D21
	A16	ECN	LCD0_D7		LCD D7
	A10	OEN	LCD0_HSYNC0		LCD HSYNC signal
	B7	DSI_CN	LCD0_D0		LCD0 D0
	A7	DSI_CP	LCD0_D1		LCD0 D1
	C15	ECP	LCD0_D10		LCD0 D10
	B15	EDP	LCD0_D12		LCD0 D12
	B14	EEN	LCD0_D13		LCD0 D13
	C14	EEP	LCD0_D14		LCD0 D14
	B13	OAN	LCD0_D15		LCD0 D15
	A9	DSI_DP3	LCD0_D16		LCD0 D16
	R19	LCD0_D17	LCD0_D17		LCD0 D17
	T19	LCD0_D18	LCD0_D18		LCD0 D18
	A13	OAP	LCD0_D19		LCD0 D19
	C8	DSI_DN1	LCD0_D2		LCD0 D2
	C12	OBN	LCD0_D20		LCD0 D20
	B12	OCN	LCD0_D22		LCD0 D22
	C11	OCP	LCD0_D23		LCD0 D23
	C17	EAN	LCD0_D3		LCD0 D3
	B17	EAP	LCD0_D4		LCD0 D4
	C16	EBN	LCD0_D5		LCD0 D5
	B16	EBP	LCD0_D6		LCD0 D6
	B8	DSI_DP1	LCD0_D8		LCD0 D8
	B9	DSI_DN3	LCD0_D9		LCD0 D9
	B10	OEP	LCD0_DCLK0		LCD0 DCLK0
	B11	ODN	LCD0_LDE0		LCD0 LDE0
	C10	ODP	LCD0_VSYNC0		LCD0 VSYNC0

LVDS	D10	AGND_LVDS	AGND_LVDS		LVDS AGND
	C17	EAN	EAN		LVDS EAN
	B17	EAP	EAP		LVDS EAP
	C16	EBN	EBN		LVDS EBN
	B16	EBP	EBP		LVDS EBP
	C15	ECP	ECP		LVDS ECP
	A15	EDN	EDN		LVDS EDN
	B15	EDP	EDP		LVDS EDP
	B14	EEN	EEN		LVDS EEN
	C14	EEP	EEP		LVDS EEP
	A16	ECN	ECN		LVDS ENC
	B13	OAN	OAN		LVDS OAN
	A13	OAP	OAP		LVDS OAP
	C12	OBN	OBN		LVDS OBN
	A12	OBP	OBP		LVDS OBP
	B12	OCN	OCN		LVDS OCN
	C11	OCP	OCP		LVDS OCP
	B11	ODN	ODN		LVDS ODN
	C10	ODP	ODP		LVDS ODP
	A10	OEN	OEN		LVDS OEN
	B10	OEP	OEP		LVDS OEP
MIPI CSI	R21	AVCC_CSI	AVCC_CSI		MIPI CSI AVCC
	P21	AVDD_CSI	AVDD_CSI		MIPI CSI AVDD
MIPI DSI	B7	DSI_CN	DSI_CN		MIPI DSI CN
	A7	DSI_CP	DSI_CP		MIPI DSI CP
	B6	DSI_DN0	DSI_DN0		MIPI DSI DN0
	C8	DSI_DN1	DSI_DN1		MIPI DSI DN1
	B5	DSI_DN2	DSI_DN2		MIPI DSI DN2
	B9	DSI_DN3	DSI_DN3		MIPI DSI DN3
	A6	DSI_DP0	DSI_DP0		MIPI DSI DP0
	B8	DSI_DP1	DSI_DP1		MIPI DSI DP1
	C6	DSI_DP2	DSI_DP2		MIPI DSI DP2
	A9	DSI_DP3	DSI_DP3		MIPI DSI DP3
NAND Flash	B2	NAND_ALE	NAND_ALE		NAND ALE
	B3	NAND_CE0B	NAND_CE0B		NAND CE0B
	A3	NAND_CE1B	NAND_CE1B		NAND CE1B
	B3	NAND_CE0B	NAND_CEB0		NAND CEB0
	A3	NAND_CE1B	NAND_CEB1		NAND CEB1
	E3	NAND_CE2B	NAND_CEB2		NAND CEB2
	C5	NAND_CE3B	NAND_CEB3		NAND CEB3
	A2	NAND_CLE	NAND_CLE		NAND CLE
	B1	NAND_D0	NAND_D0		NAND D0
	C2	NAND_D1	NAND_D1		NAND D1
	C1	NAND_D2	NAND_D2		NAND D2
	D1	NAND_D3	NAND_D3		NAND D3
	E2	NAND_D4	NAND_D4		NAND D4
	F3	NAND_D5	NAND_D5		NAND D5
	F2	NAND_D6	NAND_D6		NAND D6
	F1	NAND_D7	NAND_D7		NAND D7
	C3	NAND_DQS	NAND_DQS		NAND DQS
	D2	NAND_DQSN	NAND_DQSN		NAND DQSN

	A4	NAND_RB	NAND_RB		NAND RB
	B4	NAND_RDB	NAND_RDB		NAND RDB
	C4	NAND_RDBN	NAND_RDBN		NAND RDBN
	A1	NAND_WRB	NAND_WRB		NAND write enable
NOR Flash	R19	LCD0_D17	NOR_A0		NOR Flash A0
	W24	SD0_CMD	NOR_A1		NOR Flash A1
	L22	KS_OUT1	NOR_A10		NOR Flash A10
	L23	KS_OUT2	NOR_A11		NOR Flash A11
	AB18	SPI0_SCLK	NOR_A12		NOR Flash A12
	AC19	SPI0_SS	NOR_A13		NOR Flash A13
	AB19	SPI0_MISO	NOR_A14		NOR Flash A14
	AA19	SPI0_MOSI	NOR Flash A15		NOR Flash A15
	AD16	I2S_D0	NOR_A16		NOR Flash A16
	AC16	I2S_BCLK0	NOR_A17		NOR Flash A17
	AD17	I2S_LRCLK0	NOR_A18		NOR Flash A18
	AC17	I2S_MCLK0	NOR_A19		NOR Flash A19
	T19	LCD0_D18	NOR_A2		NOR Flash A2
	AB17	I2S_D1	NOR_A20		NOR Flash A20
	AD18	I2S_BCLK1	NOR_A21		NOR Flash A21
	AC18	I2S_LRCLK1	NOR_A22		NOR Flash A22
	AD19	I2S_MCLK1	NOR_A23		NOR Flash A23
	R22	SR0_PCLK	NOR_A3		NOR Flash A3
	A16	ECN	NOR_A4		NOR Flash A4
	N21	KS_IN0	NOR_A5		NOR Flash A5
	M21	KS_IN1	NOR_A6		NOR Flash A6
	L21	KS_IN2	NOR_A7		NOR Flash A7
	K21	KS_IN3	NOR_A8		NOR Flash A8
	J21	KS_OUT0	NOR_A9		NOR Flash A9
	T22	SD1_CMD	NOR_CEB0_7		NOR Flash CEB0 7
	Y23	SD0_D0	NOR_D0		NOR Flash D0
	Y22	SD0_D1	NOR_D1		NOR Flash D1
	T21	SR0_CKOUT	NOR_D10		NOR Flash D10
	C15	ECP	NOR_D11		NOR Flash D11
	A15	EDN	NOR_D12		NOR Flash D12
	B15	EDP	NOR_D13		NOR Flash D13
	C16	EBN	NOR_D14		NOR Flash D14
	B16	EBP	NOR_D15		NOR Flash D15
	V24	SD0_D2	NOR_D2		NOR Flash D2
	W23	SD0_D3	NOR_D3		NOR Flash D3
	U22	SD0_D4	NOR_D4		NOR Flash D4
	V23	SD0_D5	NOR_D5		NOR Flash D5
	T23	SD0_D6	NOR_D6		NOR Flash D6
	T24	SD0_D7	NOR_D7		NOR Flash D7
	C17	EAN	NOR_D8		NOR Flash D8
	B17	EAP	NOR_D9		NOR Flash D9
	C14	EEP	NOR_RD		NOR Flash RD
	B14	EEN	NOR_WR		NOR Flash WR

	AB18	SPI0_SCLK	PCM0_CLK		PCM0 CLK
PCM	AC18	I2S_LRCLK1	PCM0_CLK		PCM0 CLK
	AB19	SPI0_MISO	PCM0_IN		PCM0 IN
	AC16	I2S_BCLK0	PCM0_IN		PCM0 IN
	AC19	SPI0_SS	PCM0_OUT		PCM0 OUT
	AD18	I2S_BCLK1	PCM0_OUT		PCM0 OUT
	AA19	SPI0_MOSI	PCM0_SYNC		PCM0 SYNC
	AD19	I2S_MCLK1	PCM0_SYNC		PCM0 SYNC
	AC17	I2S_MCLK0	PCM1_CLK		PCM1 CLK
	Y21	PCM1_CLK	PCM1_CLK		PCM1 CLK
	AA21	PCM1_IN	PCM1_IN		PCM1 IN
	AB19	SPI0_MISO	PCM1_IN		PCM1 IN
	AC22	UART0_RX	PCM1_IN		PCM1 IN
	AC19	SPI0_SS	PCM1_OUT		PCM1 OUT
	AD22	UART0_TX	PCM1_OUT		PCM1 OUT
	W21	PCM1_OUT	PCM1_OUT		PCM1 OUT
	AA22	PCM1_SYNC	PCM1_SYNC		PCM1 SYNC
	AD17	I2S_LRCLK0	PCM1_SYNC		PCM1 SYNC
PWM	G1	ETH_TXEN	PWM0		PWM0
	L21	KS_IN2	PWM0		PWM0
	N21	KS_IN0	PWM0		PWM0
	R22	SR0_PCLK	PWM0		PWM0
	H4	ETH_RXER	PWM1		PWM1
	K21	KS_IN3	PWM1		PWM1
	M21	KS_IN1	PWM1		PWM1
	T21	SR0_CKOUT	PWM1		PWM1
	J2	ETH_RXD1	PWM2		PWM2
	J21	KS_OUT0	PWM2		PWM2
	L23	KS_OUT2	PWM2		PWM2
	T19	LCD0_D18	PWM2		PWM2
	J1	ETH_RXD0	PWM3		PWM3
	L22	KS_OUT1	PWM3		PWM3
	R19	LCD0_D17	PWM3		PWM3
	AA21	PCM1_IN	PWM4		PWM4
	C5	NAND_CE3B	PWM4		PWM4
	H2	ETH_TXD0	PWM4		PWM4
	J4	ETH_CRS_DV	PWM4		PWM4
	N21	KS_IN0	PWM4		PWM4
	T19	LCD0_D18	PWM4		PWM4
	E3	NAND_CE2B	PWM5		PWM5
	H3	ETH_TXD1	PWM5		PWM5
	M21	KS_IN1	PWM5		PWM5
	Y21	PCM1_CLK	PWM5		PWM5
SDIO	B7	DSI_CN	SD1_D0		SDIO D0
	L22	KS_OUT1	SD0_CLK		SDIO0 CLK
	W22	SD0_CLK	SD0_CLK		SDIO0 CLK
	A6	DSI_DP0	SD0_CLKB		SDIO0 CLKB

	R19	LCD0_D17	SD0_CLKB		SDIO0 CLKB
	J21	KS_OUT0	SD0_CMD		SDIO0 CMD
	W24	SD0_CMD	SD0_CMD		SDIO0 CMD
	Y23	SD0_D0	SD0_D0		SDIO0 D0
	Y22	SD0_D1	SD0_D1		SDIO0 D1
	L23	KS_OUT2	SD0_D1B		SDIO0 D1B
	V24	SD0_D2	SD0_D2		SDIO0 D2
	W23	SD0_D3	SD0_D3		SDIO0 D3
	U22	SD0_D4	SD0_D4		SDIO0 D4
	V23	SD0_D5	SD0_D5		SDIO0 D5
	T23	SD0_D6	SD0_D6		SDIO0 D6
	T24	SD0_D7	SD0_D7		SDIO0 D7
	A9	DSI_DP3	SD1_CLK		SDIO1 CLK
	U23	SD1_CLK	SD1_CLK		SDIO1 CLK
	A9	DSI_DP3	SD1_CLKB		SDIO1 CLKB
	C6	DSI_DP2	SD1_CLKB		SDIO1 CLKB
	R19	LCD0_D17	SD1_CMD		SDIO1 CMD
	T22	SD1_CMD	SD1_CMD		SDIO1 CMD
	U22	SD0_D4	SD1_D0		SDIO1 D0
	A7	DSI_CP	SD1_D1		SDIO1 D1
	V23	SD0_D5	SD1_D1		SDIO1 D1
	B5	DSI_DN2	SD1_D1B		SDIO1 D1B
	B8	DSI_DP1	SD1_D2		SDIO1 D2
	T23	SD0_D6	SD1_D2		SDIO1 D2
	B9	DSI_DN3	SD1_D3		SDIO1 D3
	T24	SD0_D7	SD1_D3		SDIO1 D3
	B4	NAND_RDB	SD2_CLK		SDIO2 CLK
	C4	NAND_RDBN	SD2_CMD		SDIO2 CMD
	B1	NAND_D0	SD2_D0		SDIO2 D0
	C2	NAND_D1	SD2_D1		SDIO2 D1
	C1	NAND_D2	SD2_D2		SDIO2 D2
	D1	NAND_D3	SD2_D3		SDIO2 D3
	E2	NAND_D4	SD2_D4		SDIO2 D4
	F3	NAND_D5	SD2_D5		SDIO2 D5
	F2	NAND_D6	SD2_D6		SDIO2 D6
	F1	NAND_D7	SD2_D7		SDIO2 D7
SMII	G2	ETH_REF_CLK	SMII_CLK		SMII CLK
	J4	ETH_CRS_DV	SMII_RX		SMII RX
	H3	ETH_TXD1	SMII_SYNC		SMII SYNC
	H2	ETH_TXD0	SMII_TX		SMII TX
SPIO	A6	DSI_DP0	SPI0_MISO		SPI0 MISO
	AB19	SPI0_MISO	SPI0_MISO		SPI0 MISO
	AA19	SPI0_MOSI	SPI0_MOSI		SPI0 MOSI
	B6	DSI_DN0	SPI0_MOSI		SPI0 MOSI
	AB18	SPI0_SCLK	SPI0_SCLK		SPI0 SCLK
	C6	DSI_DP2	SPI0_SCLK		SPI0 SCLK
	AC19	SPI0_SS	SPI0_SS		SPI0 SS
	B5	DSI_DN2	SPI0_SS		SPI0 SS
	AC22	UART0_RX	SPI1_MISO		SPI1 MISO
	AA24	TWI0_SDATA	SPI1_MOSI		SPI1 MOSI

	AA23	TWI0_SCLK	SPI1_SCLK		SPI1 SCLK
	AD22	UART0_TX	SPI1_SS		SPI1 SS
	B2	NAND_ALE	SPI2_MISO		SPI2 MISO
	J4	ETH_CRS_DV	SPI2_MISO		SPI2 MISO
	A2	NAND_CLE	SPI2_MOSI		SPI2 MOSI
	G2	ETH_REF_CLK	SPI2_MOSI		SPI2 MOSI
	B3	NAND_CE0B	SPI2_SCLK		SPI2 SCLK
	H2	ETH_TXD0	SPI2_SCLK		SPI2 SCLK
	A3	NAND_CE1B	SPI2_SS		SPI2 SS
	H3	ETH_TXD1	SPI2_SS		SPI2 SS
	J1	ETH_RXD0	SPI3_MISO		SPI3 MISO
	H4	ETH_RXER	SPI3_MOSI		SPI3 MOSI
	G1	ETH_TXEN	SPI3_SCLK		SPI3 SCLK
	J2	ETH_RXD1	SPI3_SS		SPI3 SS
TV	F4	TVCVBS	TVCVBS		TV CVBS
TWI	AA23	TWI0_SCLK	TWI0_SCLK		TWI0 SCLK
	AD22	UART0_TX	TWI0_SCLK		TWI0 SCLK
	AA24	TWI0_SDATA	TWI0_SDATA		TWI0 SDATA
	AC22	UART0_RX	TWI0_SDATA		TWI0 SDATA
	AA23	TWI0_SCLK	TWI1_SCLK		TWI1 SCLK
	AC20	TWI1_SCLK	TWI1_SCLK		TWI1 SCLK
	AA24	TWI0_SDATA	TWI1_SDATA		TWI1 SDATA
	AB20	TWI1_SDATA	TWI1_SDATA		TWI1 SDATA
	AB23	TWI2_SCLK	TWI2_SCLK		TWI2 SCLK
	AB24	TWI2_SDATA	TWI2_SDATA		TWI2 SDATA
	AA22	PCM1_SYNC	TWI3_SCLK		TWI3 SCLK
	AB18	SPI0_SCLK	TWI3_SCLK		TWI3 SCLK
	AA19	SPI0_MOSI	TWI3_SDATA		TWI3 SDATA
	W21	PCM1_OUT	TWI3_SDATA		TWI3 SDATA
UART	AB22	UART2_RTSB	UART0_RX		UART0 RX
	AC22	UART0_RX	UART0_RX		UART0 RX
	AB21	UART2_CTSB	UART0_TX		UART0 TX
	AD22	UART0_TX	UART0_TX		UART0 TX
	AA24	TWI0_SDATA	UART1_RX		UART1 RX
	W23	SD0_D3	UART1_RX		UART1 RX
	AA23	TWI0_SCLK	UART1_TX		UART1 TX
	V24	SD0_D2	UART1_TX		UART1 TX
	AA24	TWI0_SDATA	UART2_CTSB		UART2 CTSB
	AB21	UART2_CTSB	UART2_CTSB		UART2 CTSB
	B5	DSI_DN2	UART2_CTSB		UART2 CTSB
	J1	ETH_RXD0	UART2_CTSB		UART2 CTSB
	W23	SD0_D3	UART2_CTSB		UART2 CTSB
	AA23	TWI0_SCLK	UART2_RTSB		UART2 RTSB
	AB22	UART2_RTSB	UART2_RTSB		UART2 RTSB
	C6	DSI_DP2	UART2_RTSB		UART2 RTSB
	J2	ETH_RXD1	UART2_RTSB		UART2 RTSB
	V24	SD0_D2	UART2_RTSB		UART2 RTSB

	A6	DSI_DP0	UART2_RX		UART2 RX
	AC21	UART2_RX	UART2_RX		UART2 RX
	AC22	UART0_RX	UART2_RX		UART2 RX
	G1	ETH_TXEN	UART2_RX		UART2 RX
	Y23	SD0_D0	UART2_RX		UART2 RX
	AD21	UART2_TX	UART2_TX		UART2 TX
	AD22	UART0_TX	UART2_TX		UART2 TX
	B6	DSI_DN0	UART2_TX		UART2 TX
	H4	ETH_RXER	UART2_TX		UART2 TX
	Y22	SD0_D1	UART2_TX		UART2 TX
	AC24	UART3_CTSB	UART3_CTSB		UART3 CTSB
	AC23	UART3_RTSB	UART3_RTSB		UART3 RTSB
	AD23	UART3_RX	UART3_RX		UART3 RX
	AD24	UART3_TX	UART3_TX		UART3 TX
	AA21	PCM1_IN	UART4_RX		UART4 RX
	J4	ETH_CRS_DV	UART4_RX		UART4 RX
	G2	ETH_REF_CLK	UART4_TX		UART4 TX
	Y21	PCM1_CLK	UART4_TX		UART4 TX
	AC23	UART3_RTSB	UART5_RX		UART5 RX
	J1	ETH_RXD0	UART5_RX		UART5 RX
	J21	KS_OUT0	UART5_RX		UART5 RX
	Y23	SD0_D0	UART5_RX		UART5 RX
	AC24	UART3_CTSB	UART5_TX		UART5 TX
	J2	ETH_RXD1	UART5_TX		UART5 TX
	L23	KS_OUT2	UART5_TX		UART5 TX
	Y22	SD0_D1	UART5_TX		UART5 TX
	AA22	PCM1_SYNC	UART6_RX		UART6 RX
	H2	ETH_TXD0	UART6_RX		UART6 RX
	H3	ETH_TXD1	UART6_TX		UART6 TX
	W21	PCM1_OUT	UART6_TX		UART6 TX
USB	F21	HSIC_DQ	HSIC_DQ		USB HSIC DQ
	G21	HSIC_DQS	HSIC_DQS		USB HSIC DQS
	F24	U2_DM1	U2_DM1		USB2 DM1
	G24	U2_DM2	U2_DM2		USB2 DM2
	F23	U2_DP1	U2_DP1		USB2 DP1
	G23	U2_DP2	U2_DP2		USB2 DP2
	D20	U2_IDPIN2	U2_IDPIN2		USB2 IDPIN2
	D24	U3_DM0	U3_DM0		USB3 DM0
	D23	U3_DP0	U3_DP0		USB3 DP0
	A24	HSIN	HSIN		USB3 HSIN
	A23	HSIP	HSIP		USB3 HSIP
	B23	HSON	HSON		USB3 HSON
	B24	HSOP	HSOP		USB3 HSOP
	C24	U3_IDPIN0	U3_IDPIN0		USB3 IDPIN0
GPIO	C3	NAND_DQS	GPIOA12	0	GPIOA12
	D2	NAND_DQSN	GPIOA13	1*	GPIOA13

	H2	ETH_TXD0	GPIOA14	x	GPIOA14
	H3	ETH_TXD1	GPIOA15	x	GPIOA15
	G1	ETH_TXEN	GPIOA16	0**	GPIOA16
	H4	ETH_RXER	GPIOA17	z	GPIOA17
	J4	ETH_CRS_DV	GPIOA18	x	GPIOA18
	J2	ETH_RXD1	GPIOA19	z	GPIOA19
	J1	ETH_RXD0	GPIOA20	z	GPIOA20
	G2	ETH_REF_CLK	GPIOA21	x	GPIOA21
	J3	ETH_MDC	GPIOA22	x	GPIOA22
	G3	ETH_MDIO	GPIOA23	x	GPIOA23
	V22	SIRQ0	GPIOA24	z	GPIOA24
	V21	SIRQ1	GPIOA25	z	GPIOA25
	U21	SIRQ2	GPIOA26	z	GPIOA26
	AD16	I2S_D0	GPIOA27	z	GPIOA27
	AC16	I2S_BCLK0	GPIOA28	z	GPIOA28
	AD17	I2S_LRCLK0	GPIOA29	z	GPIOA29
	AC17	I2S_MCLK0	GPIOA30	z	GPIOA30
	AB17	I2S_D1	GPIOA31	z	GPIOA31
	AD18	I2S_BCLK1	GPIOB0	z	GPIOB0
	AC18	I2S_LRCLK1	GPIOB1	z	GPIOB1
	B10	OEP	GPIOB10	z	GPIOB10
	A10	OEN	GPIOB11	z	GPIOB11
	C10	ODP	GPIOB12	z	GPIOB12
	B11	ODN	GPIOB13	z	GPIOB13
	C11	OCP	GPIOB14	z	GPIOB14
	B12	OCN	GPIOB15	z	GPIOB15
	A12	OBP	GPIOB16	z	GPIOB16
	C12	OBN	GPIOB17	z	GPIOB17
	A13	OAP	GPIOB18	z	GPIOB18
	B13	OAN	GPIOB19	z	GPIOB19
	AD19	I2S_MCLK1	GPIOB2	z	GPIOB2
	C14	EEP	GPIOB20	z	GPIOB20
	B14	EEN	GPIOB21	z	GPIOB21
	B15	EDP	GPIOB22	z	GPIOB22
	A15	EDN	GPIOB23	z	GPIOB23
	C15	ECP	GPIOB24	z	GPIOB24
	A16	ECN	GPIOB25	z	GPIOB25
	B16	EBP	GPIOB26	z	GPIOB26
	C16	EBN	GPIOB27	z	GPIOB27
	B17	EAP	GPIOB28	z	GPIOB28
	C17	EAN	GPIOB29	z	GPIOB29
	N21	KS_IN0	GPIOB3	1*	GPIOB3
	T19	LCD0_D18	GPIOB30	0**	GPIOB30
	R19	LCD0_D17	GPIOB31	0**	GPIOB31
	M21	KS_IN1	GPIOB4	1*	GPIOB4
	L21	KS_IN2	GPIOB5	1*	GPIOB5

	K21	KS_IN3	GPIOB6	z	GPIOB6
	J21	KS_OUT0	GPIOB7	z	GPIOB7
	L22	KS_OUT1	GPIOB8	1*	GPIOB8
	L23	KS_OUT2	GPIOB9	1**	GPIOB9
	A9	DSI_DP3	GPIOC0	z	GPIOC0
	B9	DSI_DN3	GPIOC1	z	GPIOC1
	Y23	SD0_D0	GPIOC10	x	GPIOC10
	Y22	SD0_D1	GPIOC11	x	GPIOC11
	V24	SD0_D2	GPIOC12	x	GPIOC12
	W23	SD0_D3	GPIOC13	x	GPIOC13
	U22	SD0_D4	GPIOC14	x	GPIOC14
	V23	SD0_D5	GPIOC15	x	GPIOC15
	T23	SD0_D6	GPIOC16	x	GPIOC16
	T24	SD0_D7	GPIOC17	x	GPIOC17
	W24	SD0_CMD	GPIOC18	x	GPIOC18
	W22	SD0_CLK	GPIOC19	x	GPIOC19
	B8	DSI_DP1	GPIOC2	z	GPIOC2
	T22	SD1_CMD	GPIOC20	x	GPIOC20
	U23	SD1_CLK	GPIOC21	x	GPIOC21
	AB18	SPI0_SCLK	GPIOC22	1	GPIOC22
	AC19	SPI0_SS	GPIOC23	1	GPIOC23
	AB19	SPI0_MISO	GPIOC24	1	GPIOC24
	AA19	SPI0_MOSI	GPIOC25	1	GPIOC25
	AC22	UART0_RX	GPIOC26	z	GPIOC26
	AD22	UART0_TX	GPIOC27	1**	GPIOC27
	AA23	TWI0_SCLK	GPIOC28	z	GPIOC28
	AA24	TWI0_SDATA	GPIOC29	z	GPIOC29
	C8	DSI_DN1	GPIOC3	z	GPIOC3
	R22	SR0_PCLK	GPIOC31	z	GPIOC31
	A7	DSI_CP	GPIOC4	z	GPIOC4
	B7	DSI_CN	GPIOC5	z	GPIOC5
	A6	DSI_DP0	GPIOC6	z	GPIOC6
	B6	DSI_DN0	GPIOC7	z	GPIOC7
	C6	DSI_DP2	GPIOC8	z	GPIOC8
	B5	DSI_DN2	GPIOC9	z	GPIOC9
	T21	SR0_CKOUT	GPIOD10	0**	GPIOD10
	B2	NAND_ALE	GPIOD12	x	GPIOD12
	A2	NAND_CLE	GPIOD13	x	GPIOD13
	B3	NAND_CE0B	GPIOD14	x	GPIOD14
	A3	NAND_CE1B	GPIOD15	x	GPIOD15
	E3	NAND_CE2B	GPIOD16	x	GPIOD16
	C5	NAND_CE3B	GPIOD17	x	GPIOD17
	AC21	UART2_RX	GPIOD18	z	GPIOD18
	AD21	UART2_TX	GPIOD19	1**	GPIOD19
	AB22	UART2_RTSB	GPIOD20	0**	GPIOD20
	AB21	UART2_CTSB	GPIOD21	z	GPIOD21
	AD23	UART3_RX	GPIOD22	z	GPIOD22
	AD2	UART3_TX	GPIOD23	1**	GPIOD23

	4				
	AC23	UART3_RTSB	GPIOD24	0**	GPIOD24
	AC24	UART3_CTSB	GPIOD25	z	GPIOD25
	AA21	PCM1_IN	GPIOD28	z	GPIOD28
	Y21	PCM1_CLK	GPIOD29	z	GPIOD29
	AA22	PCM1_SYNC	GPIOD30	z	GPIOD30
	W21	PCM1_OUT	GPIOD31	z	GPIOD31
	AC20	TWI1_SCLK	GPIOE0	z	GPIOE0
	AB20	TWI1_SDATA	GPIOE1	z	GPIOE1
	AB23	TWI2_SCLK	GPIOE2	z	GPIOE2
	AB24	TWI2_SDATA	GPIOE3	z	GPIOE3
Power and GND	K23	AGND_CMU	AGND_CMU		CMU AGND
	E4	AGND_DAC	AGND_DAC		AGND DAC
	K22	AVCC_CMU	AVCC_CMU		CMU AVCC
	G4	AVCC_DAC	AVCC_DAC		AVCC DAC
	D11	AVCC_LVDS	AVCC_LVDS		AVCC LVDS
	J22	AVDD_CMU	AVDD_CMU		AVDD CMU
	C7	DVCCIO_DSI	DVCCIO_DSI		MIPI DSI DVCCIO
	M21	KS_IN1	DRV_VBUS0		DRV VBUS0
	D5	NAND_VCC	NAND_VCC		NAND VCC
	D6	NAND_VCC	NAND_VCC		NAND VCC
	D3	NAND_VSS	NAND_VSS		NAND VSS
	D4	NAND_VSS	NAND_VSS		NAND VSS
	N19	TST_CMU	TST_CMU		Test
	D17	TST_LVDS	TST_LVDS		Test
	H23	U2_VBUS2	U2_VBUS2		USB2 VBUS2
	C23	U3_VBUS0	U3_VBUS0		USB3 VBUS0
	H22	UAVDD	UAVDD		USB AVDD
	G22	USB_GND	USB_GND		USB GND
	C21	USB3_GND	USB3_GND		USB3 Ground
	C22	USB3_GND	USB3_GND		USB3 Ground
	E23	USB3_UVCC	USB3_UVCC		USB3 UVCC
	D22	USB3_VDDRX	USB3_VDDRX		USB3 VDDRX
	E22	USB3_VDDTX	USB3_VDDTX		USB3 VDDTX
	F22	UVCC	UVCC		VCC For USB
	K18	VCC	VCC		VCC
	K19	VCC	VCC		VCC
	L18	VCC	VCC		VCC
	L19	VCC	VCC		VCC
	N18	VCCIO	VCCIO		VCC For IO
	H21	VCCQ_HSIC	VCCQ_HSIC		USB HSIC Power
	F6	VDD_CORE	VDD_CORE		VDD for Core
	F7	VDD_CORE	VDD_CORE		VDD for Core
	F8	VDD_CORE	VDD_CORE		VDD for Core
	G6	VDD_CORE	VDD_CORE		VDD for Core
	G7	VDD_CORE	VDD_CORE		VDD for Core
	G8	VDD_CORE	VDD_CORE		VDD for Core
	H6	VDD_CORE	VDD_CORE		VDD for Core
	H7	VDD_CORE	VDD_CORE		VDD for Core
	J6	VDD_CORE	VDD_CORE		VDD for Core
	J7	VDD_CORE	VDD_CORE		VDD for Core

	K6	VDD_CORE	VDD_CORE		VDD for Core
	K7	VDD_CORE	VDD_CORE		VDD for Core
	P18	VDD_CPU	VDD_CPU		VDD for CPU
	R18	VDD_CPU	VDD_CPU		VDD for CPU
	T18	VDD_CPU	VDD_CPU		VDD for CPU
	U18	VDD_CPU	VDD_CPU		VDD for CPU
	U19	VDD_CPU	VDD_CPU		VDD for CPU
	V18	VDD_CPU	VDD_CPU		VDD for CPU
	V19	VDD_CPU	VDD_CPU		VDD for CPU
	W16	VDD_CPU	VDD_CPU		VDD for CPU
	W17	VDD_CPU	VDD_CPU		VDD for CPU
	W18	VDD_CPU	VDD_CPU		VDD for CPU
	W19	VDD_CPU	VDD_CPU		VDD for CPU
	Y16	VDD_CPU	VDD_CPU		VDD for CPU
	Y17	VDD_CPU	VDD_CPU		VDD for CPU
	Y18	VDD_CPU	VDD_CPU		VDD for CPU
	Y19	VDD_CPU	VDD_CPU		VDD for CPU
	P19	VDD_CPU_FB	VDD_CPU_FB		VDD CPU Feed back
	D14	VDD_GPU	VDD_GPU		VDD for GPU
	D15	VDD_GPU	VDD_GPU		VDD for GPU
	D16	VDD_GPU	VDD_GPU		VDD for GPU
	F12	VDD_GPU	VDD_GPU		VDD for GPU
	F13	VDD_GPU	VDD_GPU		VDD for GPU
	F14	VDD_GPU	VDD_GPU		VDD for GPU
	F15	VDD_GPU	VDD_GPU		VDD for GPU
	F16	VDD_GPU	VDD_GPU		VDD for GPU
	F17	VDD_GPU	VDD_GPU		VDD for GPU
	G12	VDD_GPU	VDD_GPU		VDD for GPU
	G13	VDD_GPU	VDD_GPU		VDD for GPU
	G14	VDD_GPU	VDD_GPU		VDD for GPU
	G15	VDD_GPU	VDD_GPU		VDD for GPU
	G16	VDD_GPU	VDD_GPU		VDD for GPU
	G17	VDD_GPU	VDD_GPU		VDD for GPU
	AA15	VDDR	VDDR		VDDR
	AA16	VDDR	VDDR		VDDR
	AB15	VDDR	VDDR		VDDR
	AB16	VDDR	VDDR		VDDR
	J5	VDDR	VDDR		VDDR
	K4	VDDR	VDDR		VDDR
	K5	VDDR	VDDR		VDDR
	L5	VDDR	VDDR		VDDR
	M5	VDDR	VDDR		VDDR
	N5	VDDR	VDDR		VDDR
	U5	VDDR	VDDR		VDDR
	U6	VDDR	VDDR		VDDR
	V5	VDDR	VDDR		VDDR
	V6	VDDR	VDDR		VDDR
	W5	VDDR	VDDR		VDDR
	W6	VDDR	VDDR		VDDR
	W7	VDDR	VDDR		VDDR
	W8	VDDR	VDDR		VDDR

	Y5	VDDR	VDDR		VDDR
	Y6	VDDR	VDDR		VDDR
	Y7	VDDR	VDDR		VDDR
	Y8	VDDR	VDDR		VDDR
	E21	VR15	VR15		Vref Voltage
	AA20	VSD_PAD	VSD_PAD		SD3.0 Power
	AB3	GND	GND		Gound
	AC15	GND	GND		Gound
	F10	GND	GND		Gound
	F11	GND	GND		Gound
	F18	GND	GND		Gound
	F19	GND	GND		Gound
	F9	GND	GND		Gound
	G10	GND	GND		Gound
	G11	GND	GND		Gound
	G18	GND	GND		Gound
	G19	GND	GND		Gound
	G9	GND	GND		Gound
	H10	GND	GND		Gound
	H11	GND	GND		Gound
	H12	GND	GND		Gound
	H13	GND	GND		Gound
	H14	GND	GND		Gound
	H15	GND	GND		Gound
	H16	GND	GND		Gound
	H17	GND	GND		Gound
	H18	GND	GND		Gound
	H19	GND	GND		Gound
	H8	GND	GND		Gound
	H9	GND	GND		Gound
	J10	GND	GND		Gound
	J11	GND	GND		Gound
	J12	GND	GND		Gound
	J13	GND	GND		Gound
	J14	GND	GND		Gound
	J15	GND	GND		Gound
	J16	GND	GND		Gound
	J17	GND	GND		Gound
	J18	GND	GND		Gound
	J19	GND	GND		Gound
	J8	GND	GND		Gound
	J9	GND	GND		Gound
	K10	GND	GND		Gound
	K11	GND	GND		Gound
	K12	GND	GND		Gound
	K13	GND	GND		Gound
	K14	GND	GND		Gound
	K15	GND	GND		Gound
	K16	GND	GND		Gound
	K17	GND	GND		Gound
	K3	GND	GND		Gound

	K8	GND	GND		Gound
	K9	GND	GND		Gound
	L10	GND	GND		Gound
	L11	GND	GND		Gound
	L12	GND	GND		Gound
	L13	GND	GND		Gound
	L14	GND	GND		Gound
	L15	GND	GND		Gound
	L16	GND	GND		Gound
	L17	GND	GND		Gound
	L6	GND	GND		Gound
	L7	GND	GND		Gound
	L8	GND	GND		Gound
	L9	GND	GND		Gound
	M10	GND	GND		Gound
	M11	GND	GND		Gound
	M12	GND	GND		Gound
	M13	GND	GND		Gound
	M14	GND	GND		Gound
	M15	GND	GND		Gound
	M16	GND	GND		Gound
	M17	GND	GND		Gound
	M18	GND	GND		Gound
	M19	GND	GND		Gound
	M6	GND	GND		Gound
	M7	GND	GND		Gound
	M8	GND	GND		Gound
	M9	GND	GND		Gound
	N10	GND	GND		Gound
	N11	GND	GND		Gound
	N12	GND	GND		Gound
	N13	GND	GND		Gound
	N14	GND	GND		Gound
	N15	GND	GND		Gound
	N16	GND	GND		Gound
	N17	GND	GND		Gound
	N6	GND	GND		Gound
	N7	GND	GND		Gound
	N8	GND	GND		Gound
	N9	GND	GND		Gound
	P10	GND	GND		Gound
	P11	GND	GND		Gound
	P12	GND	GND		Gound
	P13	GND	GND		Gound
	P14	GND	GND		Gound
	P15	GND	GND		Gound
	P16	GND	GND		Gound
	P17	GND	GND		Gound
	P5	GND	GND		Gound
	P6	GND	GND		Gound
	P7	GND	GND		Gound

	P8	GND	GND		Gound
	P9	GND	GND		Gound
	R10	GND	GND		Gound
	R11	GND	GND		Gound
	R12	GND	GND		Gound
	R13	GND	GND		Gound
	R14	GND	GND		Gound
	R15	GND	GND		Gound
	R16	GND	GND		Gound
	R17	GND	GND		Gound
	R5	GND	GND		Gound
	R6	GND	GND		Gound
	R7	GND	GND		Gound
	R8	GND	GND		Gound
	R9	GND	GND		Gound
	T10	GND	GND		Gound
	T11	GND	GND		Gound
	T12	GND	GND		Gound
	T13	GND	GND		Gound
	T14	GND	GND		Gound
	T15	GND	GND		Gound
	T16	GND	GND		Gound
	T17	GND	GND		Gound
	T5	GND	GND		Gound
	T6	GND	GND		Gound
	T7	GND	GND		Gound
	T8	GND	GND		Gound
	T9	GND	GND		Gound
	U10	GND	GND		Gound
	U11	GND	GND		Gound
	U12	GND	GND		Gound
	U13	GND	GND		Gound
	U14	GND	GND		Gound
	U15	GND	GND		Gound
	U16	GND	GND		Gound
	U17	GND	GND		Gound
	U7	GND	GND		Gound
	U8	GND	GND		Gound
	U9	GND	GND		Gound
	V10	GND	GND		Gound
	V11	GND	GND		Gound
	V12	GND	GND		Gound
	V13	GND	GND		Gound
	V14	GND	GND		Gound
	V15	GND	GND		Gound
	V16	GND	GND		Gound
	V17	GND	GND		Gound
	V7	GND	GND		Gound
	V8	GND	GND		Gound
	V9	GND	GND		Gound
	W10	GND	GND		Gound

	W11	GND	GND		Gound
	W12	GND	GND		Gound
	W13	GND	GND		Gound
	W14	GND	GND		Gound
	W15	GND	GND		Gound
	W9	GND	GND		Gound
	Y10	GND	GND		Gound
	Y11	GND	GND		Gound
	Y12	GND	GND		Gound
	Y13	GND	GND		Gound
	Y14	GND	GND		Gound
	Y15	GND	GND		Gound
	Y9	GND	GND		Gound

Notes on GPIO Initial State:
GPIO Initial state is listed for reference, please take the actual application as final state.
1 represent that this pin is weak pull-up with resistors in range of 10KOhm to 100KOhm.*
*1** represent that this pin is z at first time and pull-up later.*
*0** represent that this pin is z at first time and pull-down later.*
X represent that this pin value varies during the System Initial process.

1.4.3 Pin Multiplex List

Table 1-3 Pin Multiplex List

Note that the functions in Func1~Func6 do not contain all the functions used, it's a table for pin multiplexing illustration.

BGA	Function Mux	Func1 (GPIO/ PWR)	Func2 (PWM/ SIRQ/ LVDS/ TWI)	Func3 (DSI/ CSI/ DDR/ I2S/ PCM/ KEY)	Func4 (UART/ LCD/ NAND)	Func5 (NAND/ Cam/ SPI)	Func6 (Ethernet/ SDIO/ HDMI/ USB)
C03	NAND_DQS/ GPIOA12	GPIOA12			NAND DQS		
D02	NAND_DQSN/ GPIOA13	GPIOA13			NAND DQSN		
H02	ETH_TXD0/ SMII_TX/ SPI2_SCLK/ UART6_RX/ PWM4/ GPIOA14	GPIOA14	PWM4		UART6 RX	SPI2 SCLK	Ethernet TXD0/ SMII TX
H03	ETH_TXD1/ SMII_SYNC/ SPI2_SS/ UART6_TX/ PWM5/ GPIOA15	GPIOA15	PWM5		UART6 TX	SPI2 SS	Ethernet TXD1/ SMII SYNC
G01	ETH_TXEN/ SPI3_SCLK/ UART2_RX/ PWM0/ GPIOA16	GPIOA16	PWM0		UART2 RX	SPI3 SCLK	Ethernet TXEN
H04	ETH_RXER/ SPI3_MOSI/ UART2_TX/ PWM1/ GPIOA17	GPIOA17	PWM1		UART2 TX	SPI3 MOSI	Ethernet RXER
J04	ETH_CRS_DV/ SMII_RX/ SPI2_MISO/ UART4_RX/ PWM4/ GPIOA18	GPIOA18	PWM4		UART4 RX	SPI2 MISO	Ethernet CRS DV/ SMII RX
J02	ETH_RXD1/ SPI3_SS/ UART5_TX/ UART2_RTSB/ PWM2/ GPIOA19	GPIOA19	PWM2		UART5 TX/ UART2 RTSB	SPI3 SS	Ethernet RXD1
J01	ETH_RXD0/ SPI3_MISO/ UART5_RX/ UART2_CTSB/ PWM3/ GPIOA20	GPIOA20	PWM3		UART5 RX/ UART2 CTSB	SPI3 MISO	Ethernet RXD0
G02	ETH_REF_CLK/ SMII_CLK/ SPI2_MOSI/ UART4_TX/ GPIOA21	GPIOA21			UART4 TX	SPI2 MOSI	Ethernet REF CLK/ SMII CLK
J03	ETH_MDC/ GPIOA22	GPIOA22					Ethernet MDC

G03	ETH_MDIO/ GPIOA23	GPIOA23					Ethernet MDIO
V22	SIRQ0/ GPIOA24	GPIOA24	SIRQ0 Interrupt				
V21	SIRQ1/ GPIOA25	GPIOA25	SIRQ1 Interrupt				
U21	SIRQ2/ GPIOA26	GPIOA26	SIRQ2 Interrupt				
AD16	I2S_D0/ NOR_A16/ GPIOA27	GPIOA27		I2S D0			
AC16	I2S_BCLK0/ PCM0_IN/ NOR_A17/ GPIOA28	GPIOA28		PCM0 IN/ I2S BCLK0			
AD17	I2S_LRCLK0/ PCM1_SYNC/ NOR_A18/ GPIOA29	GPIOA29		PCM1 SYNC/ I2S LRCLK0			
AC17	I2S_MCLK0/ PCM1_CLK/ NOR_A19/ GPIOA30	GPIOA30		PCM1 CLK/ I2S MCLK0			
AB17	I2S_D1/ NOR_A20/ GPIOA31	GPIOA31		I2S D1			
AD18	I2S_BCLK1/ PCM0_OUT/ NOR_A21/ GPIOB0	GPIOB00		PCM0 OUT/ I2S BCLK1			
AC18	I2S_LRCLK1/ PCM0_CLK/ NOR_A22/ GPIOB1	GPIOB01		PCM0 CLK/ I2S LRCLK1			
AD19	I2S_MCLK1/ PCM0_SYNC/ NOR_A23/ GPIOB2	GPIOB02		PCM0 SYNC/ I2S MCLK1			
N21	KS_IN0/ NOR_A5/ PWM0/ PWM4/ SENS1_D4/ GPIOB3	GPIOB03	PWM0/ PWM4	KEY IN0		Camera Sensor1 D4	
M21	KS_IN1/ NOR_A6/ PWM1/ PWM5/ SENS1_D5/ DRV_VBUS0/ GPIOB4	GPIOB04	PWM1/ PWM5	KEY IN1		Camera Sensor1 D5	DRV VBUS0
L21	KS_IN2/ NOR_A7/ PWM0/ GPIOB5/ SENS1_D6	GPIOB05	PWM0	KEY IN2		Camera Sensor1 D6	
K21	KS_IN3/ NOR_A8/ PWM1/ SENS1_D7/ GPIOB6	GPIOB06	PWM1	KEY IN3		Camera Sensor1 D7	

J21	KS_OUT0/ UART5_RX/ NOR_A9/ PWM2/ SD0_CMD/ SENS1_PCLK/ GPIOB7	GPIOB07	PWM2	KEY OUT0	UART5 RX	Camera Sensor1 PCLK	SDIO0 CMD
L22	KS_OUT1/ NOR_A10/ PWM3/ SD0_CLK/ SENS1_VSYNC/ GPIOB8	GPIOB08	PWM3	KEY OUT1		Camera Sensor1 VSYNC	SDIO0 CLK
L23	KS_OUT2/ UART5_TX/ SD0_D1B/ NOR_A11/ PWM2/ SENS1_HSYNC/ GPIOB9	GPIOB09	PWM2	KEY OUT2	UART5 TX	Camera Sensor1 HSYNC	SDIO0 D1B
B10	OEP/ LCD0_DCLK0/ GPIOB10	GPIOB10	LVDS OEP		LCD0 DCLK0		
A10	OEN/ LCD0_HSYNC0/ GPIOB11	GPIOB11	LVDS OEN		LCD HSYNC0 signal		
C10	ODP/ LCD0_VSYNC0/ GPIOB12	GPIOB12	LVDS ODP		LCD0 VSYNC0		
B11	ODN/ LCD0_LDE0/ GPIOB13	GPIOB13	LVDS ODN		LCD0 LDE0		
C11	OCP/ LCD0_D23/ GPIOB14	GPIOB14	LVDS OCP		LCD0 D23		
B12	OCN/ LCD0_D22/ GPIOB15	GPIOB15	LVDS OCN		LCD0 D22		
A12	OBP/ LCD0_D21/ GPIOB16	GPIOB16	LVDS OBP		LCD D21		
C12	OBN/ LCD0_D20/ GPIOB17	GPIOB17	LVDS OBN		LCD0 D20		
A13	OAP/ LCD0_D19/ GPIOB18	GPIOB18	LVDS OAP		LCD0 D19		
B13	OAN/ LCD0_D15/ GPIOB19	GPIOB19	LVDS OAN		LCD0 D15		
C14	EEP/ NOR_RD/ LCD0_D14/ GPIOB20	GPIOB20	LVDS EEP		LCD0 D14		
B14	EEN/ NOR_WR/ LCD0_D13/ GPIOB21	GPIOB21	LVDS EEN		LCD0 D13		
B15	EDP/ NOR_D13/ LCD0_D12/ GPIOB22	GPIOB22	LVDS EDP		LCD0 D12		
A15	EDN/ NOR_D12/ LCD0_D11/ GPIOB23	GPIOB23	LVDS EDN		LCD D11		
C15	ECP/ NOR_D11/ LCD0_D10/ GPIOB24	GPIOB24	LVDS ECP		LCD0 D10		

A16	ECN/ LCD0_D7/ NOR_A4/	GPIOB25	LVDS ENC		LCD D7		
B16	EBP/ NOR_D15/ LCD0_D6/ GPIOB26	GPIOB26	LVDS EBP		LCD0 D6		
C16	EBN/ NOR_D14/ LCD0_D5/ GPIOB27	GPIOB27	LVDS EBN		LCD0 D5		
B17	EAP/ NOR_D9/ LCD0_D4/ GPIOB28	GPIOB28	LVDS EAP		LCD0 D4		
C17	EAN/ NOR_D8/ LCD0_D3/ GPIOB29	GPIOB29	LVDS EAN		LCD0 D3		
T19	LCD0_D18/ NOR_A2/ SENS1_CLKOUT/ PWM2/ PWM4/ GPIOB30	GPIOB30	PWM2/ PWM4		LCD0 D18	Camera Sensor1 CLKOUT	
R19	LCD0_D17/ SD0_CLKB/ SD1_CMD/ NOR_A0/ PWM3/ GPIOB31	GPIOB31	PWM3		LCD0 D17		SDIO0 CLKB/ SDIO1 CMD
A09	DSI_DP3/ SDIO1 CLKB/ SDIO1 CLK/ LCD0 D16/ GPIOC0	GPIOC00		MIPI DSI DP3	LCD0 D16		SDIO1 CLKB/ SDIO1 CLK
B09	DSI_DN3/ SD1_D3/ LCD0_D9/ GPIOC1	GPIOC01		MIPI DSI DN3	LCD0 D9		SDIO1 D3
B08	DSI_DP1/ SD1_D2/ LCD0_D8/ GPIOC2	GPIOC02		MIPI DSI DP1	LCD0 D8		SDIO1 D2
C08	DSI_DN1/ LCD0_D2/ GPIOC3	GPIOC03		MIPI DSI DN1	LCD0 D2		
A07	DSI_CP/ SD1_D1/ LCD0_D1/ GPIOC4	GPIOC04		MIPI DSI CP	LCD0 D1		SDIO1 D1
B07	DSI_CN/ SD1_D0/ LCD0_D0/ GPIOC5	GPIOC05		MIPI DSI CN	LCD0 D0		SDIO D0
A06	DSI_DP0/ SD0_CLKB/ SPI0_MISO/ UART2_RX/ GPIOC6	GPIOC06		MIPI DSI DP0	UART2 RX	SPI0 MISO	SDIO0 CLKB
B06	DSI_DN0/ UART2_TX/ SPI0_MOSI/ GPIOC7	GPIOC07		MIPI DSI DN0	UART2 TX	SPI0 MOSI	
C06	DSI_DP2/ SD1_CLKB/ UART2_RTSB/ SPI0_SCLK/ GPIOC8	GPIOC08		MIPI DSI DP2	UART2 RTSB	SPI0 SCLK	SDIO1 CLKB
B05	DSI_DN2/ SD1_D1B/ UART2_CTSB/ SPI0_SS/ GPIOC9	GPIOC09		MIPI DSI DN2	UART2 CTSB	SPI0 SS	SDIO1 D1B
Y23	SD0_D0/ NOR_D0/ UART2_RX/ UART5_RX/ GPIOC10	GPIOC10			UART2 RX/ UART5 RX		SDIO0 D0

Y22	SD0_D1/ NOR_D1/ UART2_TX/ UART5_TX/ GPIOC11	GPIOC11			UART2 TX/ UART5 TX		SDIO0 D1
V24	SD0_D2/ NOR_D2/ UART2_RTSB/ UART1_TX/ GPIOC12	GPIOC12			UART2 RTSB/ UART1 TX		SDIO0 D2
W23	SD0_D3/ NOR_D3/ UART2_CTSB/ UART1_RX/ GPIOC13	GPIOC13			UART2 CTSB/ UART1 RX		SDIO0 D3
U22	SD0_D4/ NOR_D4/ SD1_D0/ GPIOC14	GPIOC14					SDIO0 D4/ SDIO1 D0
V23	SD0_D5/ NOR_D5/ SD1_D1/ GPIOC15	GPIOC15					SDIO0 D5/ SDIO1 D1
T23	SD0_D6/ NOR_D6/ SD1_D2/ GPIOC16	GPIOC16					SDIO0 D6/ SDIO1 D2
T24	SD0_D7/ NOR_D7/ SD1_D3/ GPIOC17	GPIOC17					SDIO1 D3/ SDIO0 D7
W24	SD0_CMD/ NOR_A1/ GPIOC18	GPIOC18					SDIO0 CMD
W22	SD0_CLK/ GPIOC19	GPIOC19					SDIO0 CLK
T22	SD1_CMD/ NOR_CEB0_7/ GPIOC20	GPIOC20					SDIO1 CMD
U23	SD1_CLK/ GPIOC21	GPIOC21					SDIO1 CLK
AB18	SPI0_SCLK/ NOR_A12/ TWI3_SCLK/ PCM0_CLK/ GPIOC22	GPIOC22	TWI3 SCLK	PCM0 CLK		SPI0 SCLK	
AC19	SPI0_SS/ NOR_A13/ I2S_LRCLK1/ PCM1_OUT/ PCM0_OUT/ GPIOC23	GPIOC23		PCM1 OUT/ PCM0 OUT/ I2S LRCLK1		SPI0 SS	
AB19	SPI0_MISO/ NOR_A14/ I2S_MCLK1/ PCM1_IN/ PCM0_IN/ GPIOC24	GPIOC24		PCM1 IN/ PCM0 IN/ I2S MCLK1		SPI0 MISO	
AA19	SPI0_MOSI/ NOR Flash A15/ TWI3_SDATA/ PCM0_SYNC/ GPIOC25	GPIOC25	TWI3 SDATA			SPI0 MOSI	SD3.0 Power

AC22	UART0_RX/ UART2_RX/ SPI1_MISO/ TWI0_SDATA/ PCM1_IN/ I2S_MCLK1/ GPIOC26	GPIOC26	TWI0 SDATA	PCM1 IN/ I2S MCLK1	UART0 RX/ UART2 RX	SPI1 MISO	
AD22	UART0_TX/ UART2_TX/ SPI1_SS/ TWI0_SCLK/ SPDIF/ PCM1_OUT/ I2S_LRCLK1/ GPIOC27	GPIOC27	TWI0 SCLK	PCM1 OUT/ I2S LRCLK1/ SPDIF	UART0 TX/ UART2 TX	SPI1 SS	
AA23	TWI0_SCLK/ UART2_RTSB/ TWI1_SCLK/ UART1_TX/ SPI1_SCLK/ GPIOC28	GPIOC28	TWI0 SCLK/ TWI1 SCLK		UART2 RTSB/ UART1 TX	SPI1 SCLK	
AA24	TWI0_SDATA/ UART2_CTSB/ TWI1_SDATA/ UART1_RX/ SPI1_MOSI/ GPIOC29	GPIOC29	TWI0 SDATA/ TWI1 SDATA		UART2 CTSB/ UART1 RX	SPI1 MOSI	
R22	SR0_PCLK/ NOR_A3/ PWM0/ GPIOC31	GPIOC31	PWM0			Camera Sensor0 PCLK	
T21	SR0_CKOUT/ NOR_D10/ SENS1_CLKOUT/ PWM1/ GPIOD10	GPIOD10	PWM1			Camera Sensor0/ Camera Sensor1 CKOUT	
B02	NAND_ALE/ SPI2_MISO/ GPIOD12	GPIOD12			NAND ALE	SPI2 MISO	
A02	NAND_CLE/ GPIOD13/ SPI2_MOSI	GPIOD13			NAND CLE	SPI2 MOSI	
B03	NAND_CE0B/ NAND_CEB0/ SPI2_SCLK/ GPIOD14	GPIOD14			NAND CE0B/ NAND CEB0	SPI2 SCLK	
A03	NAND_CE1B/ NAND_CEB1/ SPI2_SS/ GPIOD15	GPIOD15			NAND CE1B/ NAND CEB1	SPI2 SS	
E03	NAND_CE2B/ PWM5/ GPIOD16	GPIOD16	PWM5		NAND CEB2		
C05	NAND_CE3B/ PWM4/ GPIOD17	GPIOD17	PWM4		NAND CEB3		
AC21	UART2_RX/ GPIOD18	GPIOD18			UART2 RX		
AD21	UART2_TX/ GPIOD19	GPIOD19			UART2 TX		

AB22	UART2_RTSB/ UART0_RX/ GPIOD20	GPIOD20			UART2 RTSB/ UART0 RX		
AB21	UART2_CTSB/ UART0_TX/ GPIOD21	GPIOD21			UART2 CTSB/ UART0 TX		
AD23	UART3_RX/ GPIOD22	GPIOD22			UART3 RX		
AD24	UART3_TX/ GPIOD23	GPIOD23			UART3 TX		
AC23	UART3_RTSB/ UART5_RX/ GPIOD24	GPIOD24			UART3 RTSB/ UART5 RX		
AC24	UART3_CTSB/ UART5_TX/ GPIOD25	GPIOD25			UART3 CTSB/ UART5 TX		
AA21	PCM1_IN/ SENS1_D3/ UART4_RX/ PWM4/ GPIOD28	GPIOD28	PWM4	PCM1 IN	UART4 RX	Camera Sensor1 D3	
Y21	PCM1_CLK/ SENS1_D2/ UART4_TX/ PWM5/ GPIOD29	GPIOD29	PWM5	PCM1 CLK	UART4 TX	Camera Sensor1 D2	
AA22	PCM1_SYNC/ SENS1_D1/ UART6_RX/ TWI3_SCLK/ GPIOD30	GPIOD30	TWI3 SCLK	PCM1 SYNC	UART6 RX	Camera Sensor1 D1	
W21	PCM1_OUT/ SENS1_D0/ UART6_TX/ TWI3_SDATA/ GPIOD31	GPIOD31	TWI3 SDATA	PCM1 OUT	UART6 TX	Camera Sensor1 D0	
AC20	TWI1_SCLK/ GPIOE0	GPIOE00	TWI1 SCLK				
AB20	TWI1_SDATA/ GPIOE1	GPIOE01	TWI1 SDATA				
AB23	TWI2_SCLK/ GPIOE2	GPIOE02	TWI2 SCLK				
AB24	TWI2_SDATA/ GPIOE3	GPIOE03	TWI2 SDATA				
D21	PORB	Power On Reset					
F04	TVCVBS	TV CVBS					
N18	VCCIO	VCC For IO					
F22	UVCC	VCC For USB					
P19	VDD_CPU_FB	VDD CPU Feed back					

E21	VR15	Vref Voltage					
D10	AGND_LVDS		LVDS AGND				
D17	NA		-				
W02	A0			DDR A0			
AC06	A1			DDR A1			
AC04	A10			DDR A10			
AC07	A11			DDR A11			
AD05	A12			DDR A12			
U01	A13			DDR A13			
AD08	A14			DDR A14			
AA01	A15			DDR A15			
AD07	A2			DDR A2			
AD06	A3			DDR A3			
W01	A4			DDR A4			
V02	A5			DDR A5			
AC08	A6			DDR A6			
U02	A7			DDR A7			
AD09	A8			DDR A8			
V01	A9			DDR A9			
Y02	BA0			DDR BA0			
AC05	BA1			DDR BA1			
Y01	BA2			DDR BA2			
AB02	CAS#			DDR CAS#			
AD01	CK			DDR CK			
AD02	CK#			DDR CK#			
AD03	CKE0			DDR CKE0			
AC03	CKE1			DDR CKE1			
AA02	CS0			DDR CS0			

K01	CS1			DDR CS1			
AA03	DQ0			DDR DQ0			
Y03	DQ1			DDR DQ1			
R01	DQ10			DDR DQ10			
P02	DQ11			DDR DQ11			
P01	DQ12			DDR DQ12			
M02	DQ13			DDR DQ13			
M01	DQ14			DDR DQ14			
L01	DQ15			DDR DQ15			
AC14	DQ16			DDR DQ16			
AD14	DQ17			DDR DQ17			
AD13	DQ18			DDR DQ18			
AC12	DQ19			DDR DQ19			
V03	DQ2			DDR DQ2			
AD12	DQ20			DDR DQ20			
AC10	DQ21			DDR DQ21			
AC09	DQ22			DDR DQ22			
AD10	DQ23			DDR DQ23			
AB14	DQ24			DDR DQ24			
AD15	DQ25			DDR DQ25			
AB11	DQ26			DDR DQ26			
AB10	DQ27			DDR DQ27			
AB07	DQ28			DDR DQ28			
AB06	DQ29			DDR DQ29			
U03	DQ3			DDR DQ3			
AB05	DQ30			DDR DQ30			
AB12	DQ31			DDR DQ31			
T03	DQ4			DDR DQ4			

N03	DQ5			DDR DQ5			
M03	DQ6			DDR DQ6			
L03	DQ7			DDR DQ7			
T01	DQ8			DDR DQ8			
T02	DQ9			DDR DQ9			
W03	DQM0			DDR DQM0			
R02	DQM1			DDR DQM1			
AC13	DQM2			DDR DQM2			
AB13	DQM3			DDR DQM3			
P03	DQS0			DDR DQS0			
R03	DQS0#			DDR DQS0#			
N01	DQS1			DDR DQS1			
N02	DQS1#			DDR DQS1#			
AD11	DQS2			DDR DQS2			
AC11	DQS2#			DDR DQS2#			
AB08	DQS3			DDR DQS3			
AB09	DQS3#			DDR DQS3#			
AB01	ODT0			DDR ODT0			
AC01	ODT1			DDR ODT1			
AC02	RAS#			DDR RAS#			
K02	RET_EN			DDR RET EN			
AB04	DDR_VREF			DDR VREF			
AD04	WE#			DDR WE#			
L02	ZQ			DDR ZQ			
R21	AVCC_CSI			MIPI CSI AVCC			
P21	AVDD_CSI			MIPI CSI AVDD			

C07	DVCCIO_DSI			MIPI DSI DVCCIO			
H22	UAVDD						USB AVDD
G22	USB_GND						USB GND
F21	HSIC_DQ						USB HSIC DQ
G21	HSIC_DQS						USB HSIC DQS
H21	VCCQ_HSIC						USB HSIC Power
F24	U2_DM1						USB2 DM1
G24	U2_DM2						USB2 DM2
F23	U2_DP1						USB2 DP1
G23	U2_DP2						USB2 DP2
D20	U2_IDPIN2						USB2 IDPIN2
H23	U2_VBUS2						USB2 VBUS2
D24	U3_DM0						USB3.0 DM0
D23	U3_DP0						USB3.0 DP0
A24	HSIN						USB3.0 HSIN
A23	HSIP						USB3.0 HSIP
B23	HSON						USB3.0 HSON
B24	HSOP						USB3.0 HSOP
C24	U3_IDPIN0						USB3.0 IDPIN0
E23	USB3_UVCC						USB3.0 UVCC
C23	U3_VBUS0						USB3.0 VBUS0
D22	USB3_VDDRX						USB3.0 VDDRX
E22	USB3_VDDTX						USB3.0 VDDTX
B01	NAND_D0/ SD2_D0				NAND D0		SDIO2 D0
C02	NAND_D1/ SD2_D1				NAND D1		SDIO2 D1
C01	NAND_D2/ SD2_D2				NAND D2		SDIO2 D2
D01	NAND_D3/ SD2_D3				NAND D3		SDIO2 D3

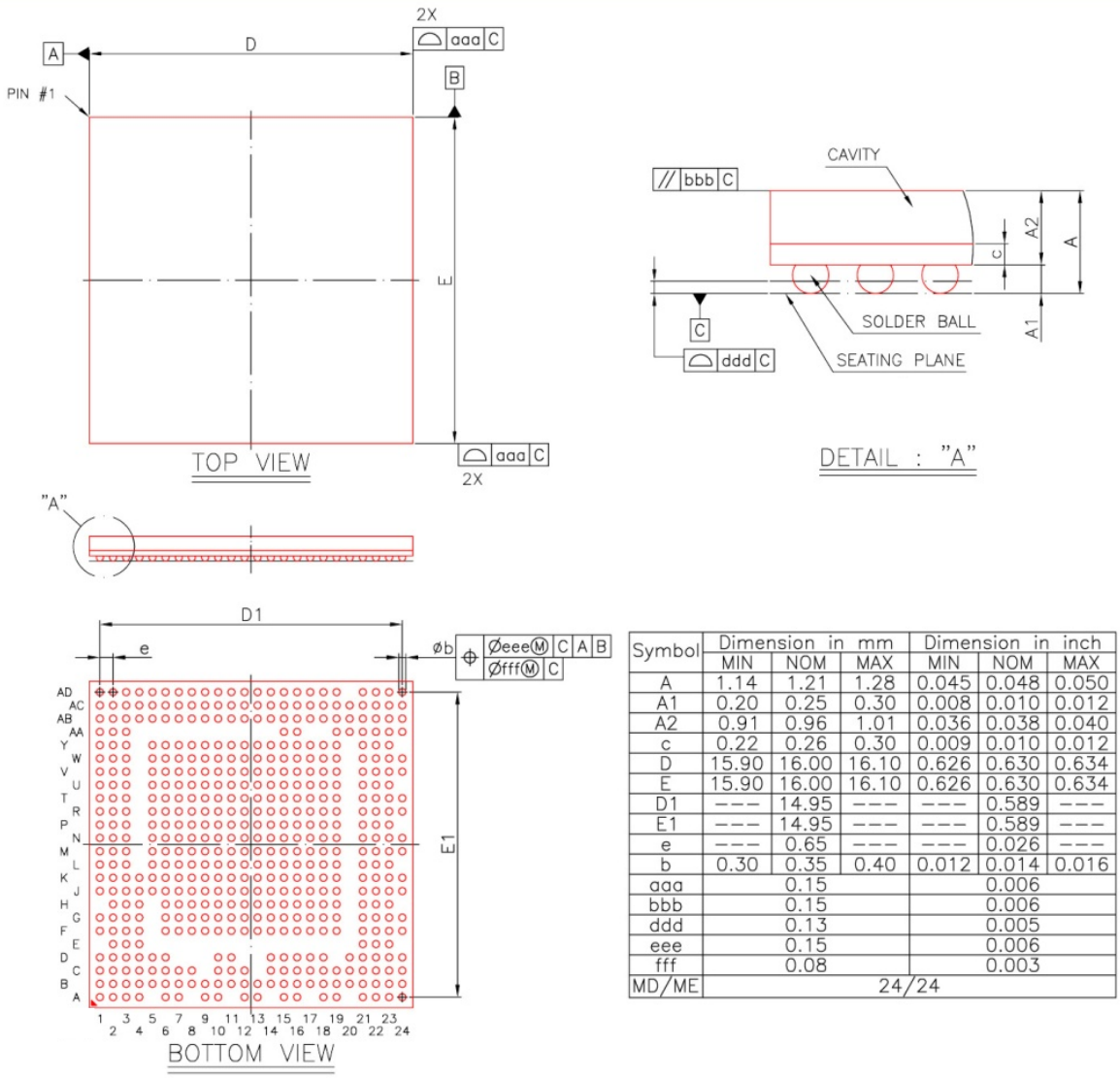
E02	NAND_D4/ SD2_D4				NAND D4		SDIO2 D4
F03	NAND_D5/ SD2_D5				NAND D5		SDIO2 D5
F02	NAND_D6/ SD2_D6				NAND D6		SDIO2 D6
F01	NAND_D7/ SD2_D7				NAND D7		SDIO2 D7
A04	NAND_RB				NAND RB		
B04	NAND_RDB/ SD2_CLK				NAND RDB		SDIO2 CLK
C04	NAND_RDBN/ SD2_CMD				NAND RDBN		SDIO2 CMD
A01	NAND_WRB				NAND write enable		
R23	SR0_DATA0					Camera Sensor0 DATA0	
R24	SR0_DATA1					Camera Sensor0 DATA1	
P23	SR0_DATA2					Camera Sensor0 DATA2	
P22	SR0_DATA3					Camera Sensor0 DATA3	
N23	SR0_DATA4					Camera Sensor0 DATA4	
M24	SR0_DATA5					Camera Sensor0 DATA5	
M22	SR0_DATA6					Camera Sensor0	

						DATA6	
M23	SR0_DATA7					Camera Sensor0 DATA7	
N22	SR0_HSYNC					Camera Sensor0 HSYNC	
N24	SR0_VSYNC					Camera Sensor0 VSYNC	
C18	TMDS_AVCC						HDMI AVCC
C19	TMDS_AVDD						HDMI AVDD
B22	CEC						HDMI CEC
A22	HPD						HDMI HPD
D18	TMDS_VSS						HDMI TMDS VSS
B21	TNCK						HDMI TNCK
A21	TPCK						HDMI TPCK
C20	TXON0						HDMI TXON
A19	TXON1						HDMI TXON1
A18	TXON2						HDMI TXON2
B20	TXOP0						HDMI TXOP0
B18	TXOP2						HDMI TXOP1
B19	TXOP1						HDMI TXOP2
K24	CLKO_24M/ CLKO_25M						
E04	AGND_DAC						
G04	AVCC_DAC						
J22	AVDD_CMU						
K23	AGND_CMU						
K22	AVCC_CMU						

J23	HOSCI						
J24	HOSCO						
AA20	VSD_PAD						

1.5 Package

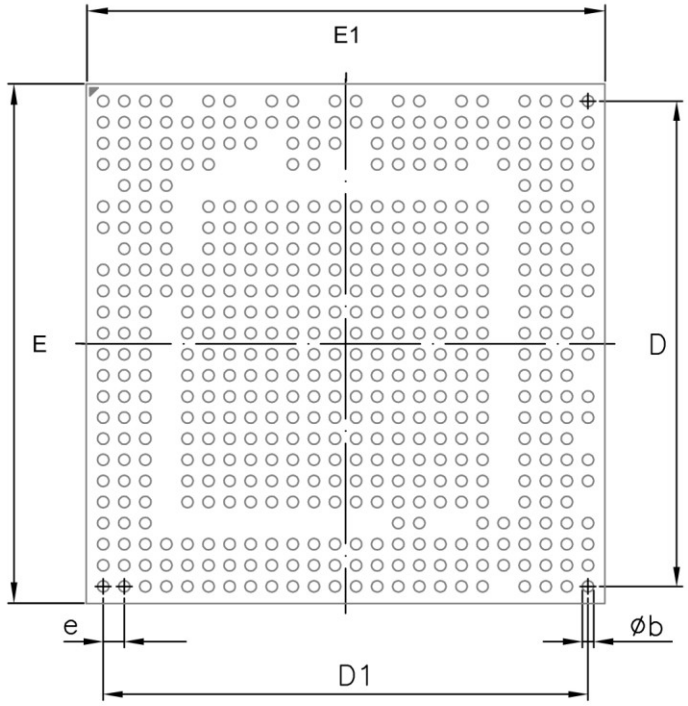
1.5.1 Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.14	1.21	1.28	0.045	0.048	0.050
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	15.90	16.00	16.10	0.626	0.630	0.634
E	15.90	16.00	16.10	0.626	0.630	0.634
D1	---	14.95	---	---	0.589	---
E1	---	14.95	---	---	0.589	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa		0.15			0.006	
bbb		0.15			0.006	
ddd		0.13			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		24/24				

Figure 1-2 S500 Package Drawing

1.5.2 Landing Pattern Recommendation



Symbol	Dimension in mm	Dimension in inch
e	0.65	0.026
b	0.3	0.012
D	14.95	0.589
D1	14.95	0.589
E	16	0.63
E1	16	0.63

Figure 1-3 Example Board Layout

1.6 Electrical Characteristics

1.6.1 Absolute Maximum Ratings

These absolute maximum ratings are stress ratings, operating at or beyond these ratings for extended periods of time (above 1ms) may result in permanent damage to the S500. All voltages ratings are relative to VSS.

Table 1-4 Absolte Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	°C
Storage Temperature	Tstg	-55	+150	°C
Supply Voltage	VDD/AVDD_CMU/USB_AVDD AVDD_MIPI/AVDD_LVDS/HDMI_LVD	-0.3	1.5	V
	VDDR	-0.3	2.5	V
	VCC/UVCC/AVCC_CMU/ AVCC_LVDS/HDMI_AVCC/NAND_VCC	-0.3	3.6	V
Input Voltage	Digital IO	-0.3	3.6	V
	Analog IO	-0.3	3.6	V
	HOSCI/HOSCO	-0.3	1.5	V
	VBUS	-0.3	5.5	V
Human Body Model (HBM)	V_{ESD} (HBM)	2000	-	V

1.6.2 DC Characteristics

Table 1-5 DC Characteristics

VCC = 3.1V Tamb = 0 to 70 °C 3.1V I/O

Parameter	Symbol	Min.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}	-	-	0.8	V
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level output voltage	V_{OL}	-	-	0.4	V
High-level output voltage	V_{OH}	2.4	-	-	V

NAND_VCC= 1.8V Tamb = 0 to 70 °C 1.8V I/O

Parameter	Symbol	Min.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}	-	-	0.4	V
High-level input voltage	V_{IH}	1.2	-	-	V
Low-level output voltage	V_{OL}	-	-	0.2	V
High-level output voltage	V_{OH}	1.5	-	-	V

VDDR = 1.5V Tamb = 0 to 70 °C 1.5V I/O

Parameter	Symbol	Min.	TYP.	MAX.	Unit
Low-level output voltage	V_{OL}	-	-	DDR_VREF-0.4	V
High-level output voltage	V_{OH}	DDR_VREF+0.4	-	-	V
Low-level input voltage	V_{IL}	-	-	DDR_VREF-0.2	V
High-level input voltage	V_{IH}	DDR_VREF+0.2	-	-	V

2 System Control

2.1 System Boot

S500 supports booting from external storage drivers, including SPI NAND, SPI NOR, and SD/MMC/eMMC. The BRECLauncher block will conduct loading boot code from external storage drivers, it will check the storage drivers' ID and if it's the right driver. If no storage diver is found right, S500 will load boot code from ADFULauncher. The right boot code will be loaded into internal SRAM and run, then the operating system will be boot up or uploaded.

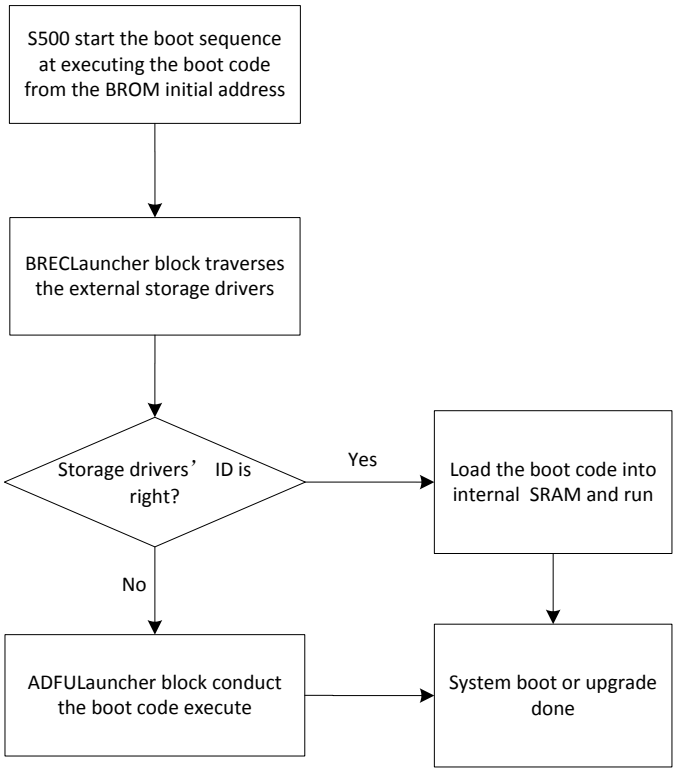


Figure 2-1 Boot sequence diagram

2.2 Address Mapping

Table 2-1 Adress Mapping

Physical Address		Size (Byte)	Function
Start	End		
0x00000000	0x7FFFFFFF	2G	DDR Memory
0x80000000	0x9FFFFFFF	512M	Reserved
0xA0000000	0xAFFFFFFF	256M	Reserved
0xB0000000	0xB7FFFFFF	128M	IO device
0xB8000000	0xBFFFFFFF	128M	Reserved
0xC0000000	0xEFFFFFFF	768M	Reserved
0xF0000000	0xFCFFFFFF	208M	Reserved
0xFD000000	0xFFFFFFFF	48M	BROM/NOR

			Note: [0xFD000000, 0xFEFFFFFF] for NOR address space [0xFFFF0000, 0xFFFF7FFF] for BROM address space NOR and BROM uses the same HSEL
IO device			
0xB0000000	0xB0007FFF	32K	Coresight base address
0xB0008000	0xB000EFFF	28K	Reserved
0xB000F000	0xB000FFFF	4K	Reserved
0xB0010000	0xB001FFFF	64K	Reserved
0xB0020000	0xB0021FFF	8K	PERIPHBASE(Timer/WD/INTC/SCU) 0x0000-0x00FF:SCU control and configuration 0x0100-0x01FF:Interrupt interface registers 0x0200-0x02FF:Global timer 0x0600-0x06FF:Timer and watchdog 0x1000-0x1FFF:Interrupt distributor
0xB0022000	0xB0022FFF	4K	REGFILEBASE(L2 control)
0xB0023000	0xB002FFFF	52K	Reserved
0xB0030000	0xB003FFFF	64K	Reserved
0xB0040000	0xB0040FFF	4K	Integration ROM table
0xB0041000	0xB004FFFF	60K	Reserved
0xB0050000	0xB0050FFF	4K	Reserved
0xB0051000	0xB0051FFF	4K	Reserved
0xB0052000	0xB0052FFF	4K	Reserved
0xB0053000	0xB0053FFF	4K	Reserved
0xB0054000	0xB0054FFF	4K	Reserved
0xB0055000	0xB0055FFF	4K	Reserved
0xB0056000	0xB0056FFF	8K	Reserved
0xB0057000	0xB0057FFF	8K	Reserved
0xB0058000	0xB0058FFF	4K	CTI0
0xB0059000	0xB0059FFF	4K	CTI1
0xB005A000	0xB005AFFF	4K	CTI2
0xB005B000	0xB005BFFF	4K	CTI3
0xB005C000	0xB005FFFF	16K	Reserved
0xB0060000	0xB00FFFFF	832K	Reserved
0xB0100000	0xB010FFFF	64K	AUDIO(I2S/SPDIF)
0xB0110000	0xB0117FFF	32K	PCM0 Controller
0xB0118000	0xB011FFFF	32K	PCM1 Controller
0xB0120000	0xB0121FFF	8K	UART0/IRC Controller
0xB0122000	0xB0123FFF	8K	UART1 Controller
0xB0124000	0xB0125FFF	8K	UART2 Controller
0xB0126000	0xB0127FFF	8K	UART3 Controller
0xB0128000	0xB0129FFF	8K	UART4 Controller
0xB012A000	0xB012BFFF	8K	UART5 Controller
0xB012C000	0xB012DFFF	8K	UART6 Controller
0xB012E000	0xB012FFFF	8K	Reserved
0xB0130000	0xB013FFFF	64K	Reserved
0xB0140000	0xB014FFFF	64K	Reserved
0xB0150000	0xB015FFFF	64K	Reserved
0xB0160000	0xB0167FFF	32K	CMU
0xB0168000	0xB016FFFF	32K	2Hz/Timer
0xB0170000	0xB0173FFF	16K	TWI0 Controller

0xB0174000	0xB0177FFF	16K	TWI1 Controller
0xB0178000	0xB017BFFF	16K	TWI2 Controller
0xB017C000	0xB017FFFF	16K	TWI3 Controller
0xB0180000	0xB018FFFF	64K	Reserved
0xB0190000	0xB019FFFF	64K	Reserved
0xB01A0000	0xB01AFFFF	64K	Key Scan Controller
0xB01B0000	0xB01BFFFF	64K	GPIO/MFP Controller (include PWM, SPS, RMU, AVS)
0xB01C0000	0xB01CFFFF	64K	DDR_UPCTL&PUB
0xB01D0000	0xB01DFFFF	64K	Reserved
0xB01E0000	0xB01FFFFF	128K	Reserved
0xB0200000	0xB0203FFF	16K	SPI0 Controller
0xB0204000	0xB0207FFF	16K	SPI1 Controller
0xB0208000	0xB020BFFF	16K	SPI2 Controller
0xB020C000	0xB020FFFF	16K	SPI3 Controller
0xB0210000	0xB021FFFF	64K	Nand Flash Controller
0xB0220000	0xB0227FFF	32K	MIPI DSI
0xB0228000	0xB022FFFF	32K	Reserved
0xB0230000	0xB0233FFF	16K	SD0 Controller
0xB0234000	0xB0237FFF	16K	SD1 Controller
0xB0238000	0xB023BFFF	16K	SD2 Controller
0xB023C000	0xB023FFFF	16K	Reserved
0xB0240000	0xB024FFFF	64K	SRAMI(Nor/SRAM/BROM Controller/ShareSRAMCTL)
0xB0250000	0xB0257FFF	32K	HDCP2Tx
0xB0258000	0xB025FFFF	32K	Reserved
0xB0260000	0xB026FFFF	64K	DMA Controller
0xB0270000	0xB0277FFF	32K	SI Controller
0xB0278000	0xB027FFFF	32K	Reserved
0xB0280000	0xB0287FFF	32K	VDE
0xB0288000	0xB028FFFF	32K	VCE
0xB0290000	0xB029FFFF	64K	DCU_DMM Controller
0xB02A0000	0xB02AFFFF	64K	LCD Controller
0xB02B0000	0xB02B7FFF	32K	Reserved
0xB02B8000	0xB02BFFFF	32K	Reserved
0xB02C0000	0xB02CFFFF	64K	HDMI Controller
0xB02D0000	0xB02D7FFF	32K	MIPI CSI
0xB02D8000	0xB02DFFFF	32K	Reserved
0xB02E0000	0xB02EFFFF	64K	DE(Display Engine)
0xB02F0000	0xB02F3FFF	16K	Reserved
0xB02F4000	0xB02FFFFF	48K	Reserved
0xB0300000	0xB030FFFF	64K	G3D
0xB0310000	0xB031FFFF	64K	Ethernet MAC
0xB0320000	0xB03FFFFF	896K	Reserved
0xB0400000	0xB04FFFFF	1M	USB3 Controller
0xB0500000	0xB05FFFFF	1M	NOC service
0xB0600000	0xB07FFFFF	2M	USB2H Controller
0xB0800000	0xB3FFFFFF	56M	Reserved
SRAMOC:			
0xB4000000	0xB405FFFF	384K	Reserved
0xB4060000	0xB40BFFFF	384K	ShareSRAM (72K SRAM space: 0xB4060000~0xB4071FFF)
0xB40E0000	0xB40FFFFF	128K	Reserved

0xB4100000	0xB7FFFFFF	63M	Reserved
SRAMI Memory:			
0xFD000000	0xFEFFFFFF	32MB	Nor flash
0xFFFE0000	0xFFFE7FFF	32K	Reserved
0xFFFF0000	0xFFFF7FFF	32K	Reserved
0xFFFF8000	0xFFFF8FFF	4K	Reserved
0xFFFF0000	0xFFFF0FFF	4K	BROM(remap =0)
0xFFFF1000	0xFFFF7FFF	28K	BROM
0xFFFF8000	0xFFFF8FFF	4K	Boot_RAM(4KB,remap=0)
0xFFFF0000	0xFFFF0FFF	4K	Boot_RAM(4KB,remap=1)
0xFFFF1000	0xFFFF7FFF	28K	BROM
0xFFFF8000	0xFFFF8FFF	4K	BROM(remap=1)

2.3 System Secure

System Secure of S500 is ensured by implementing ARM based TrustZone technology, eFUSE, and secure algorithm, protecting the system from hack attacks and shack attacks.

3 Clock and Reset Management Unit

3.1 Overview

The Clock and Reset management Unit is responsible for providing appropriate clocks for system and subsystems, and manages reset of the system.

3.2 RMU (Reset Management Unit)

The reset management unit is in control of the reset of VDD power domain, and support reset triggers from software and hardware, including power on reset, watchdog timer reset, JTAG reset and other software reset source.

Table 3-1 Reset status

	JTAG	CPU 0	CPU 1	CPU 2	CPU 3	WD0_flag	WD1_2_3_flag	WD_Controller	CMU	CHIPID	Others
Power On/Wake Up:											
POWEROK	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Working Mode:											
Whole_WD0RST_n	No	No	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
CPU2_pwron_rst_n	No	No	No	Yes	No	No	No	No	No	No	No
CPU3_pwron_rst_n	No	No	No	No	Yes	No	No	No	No	No	No
Software Reset:											
SW_RST	No	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes

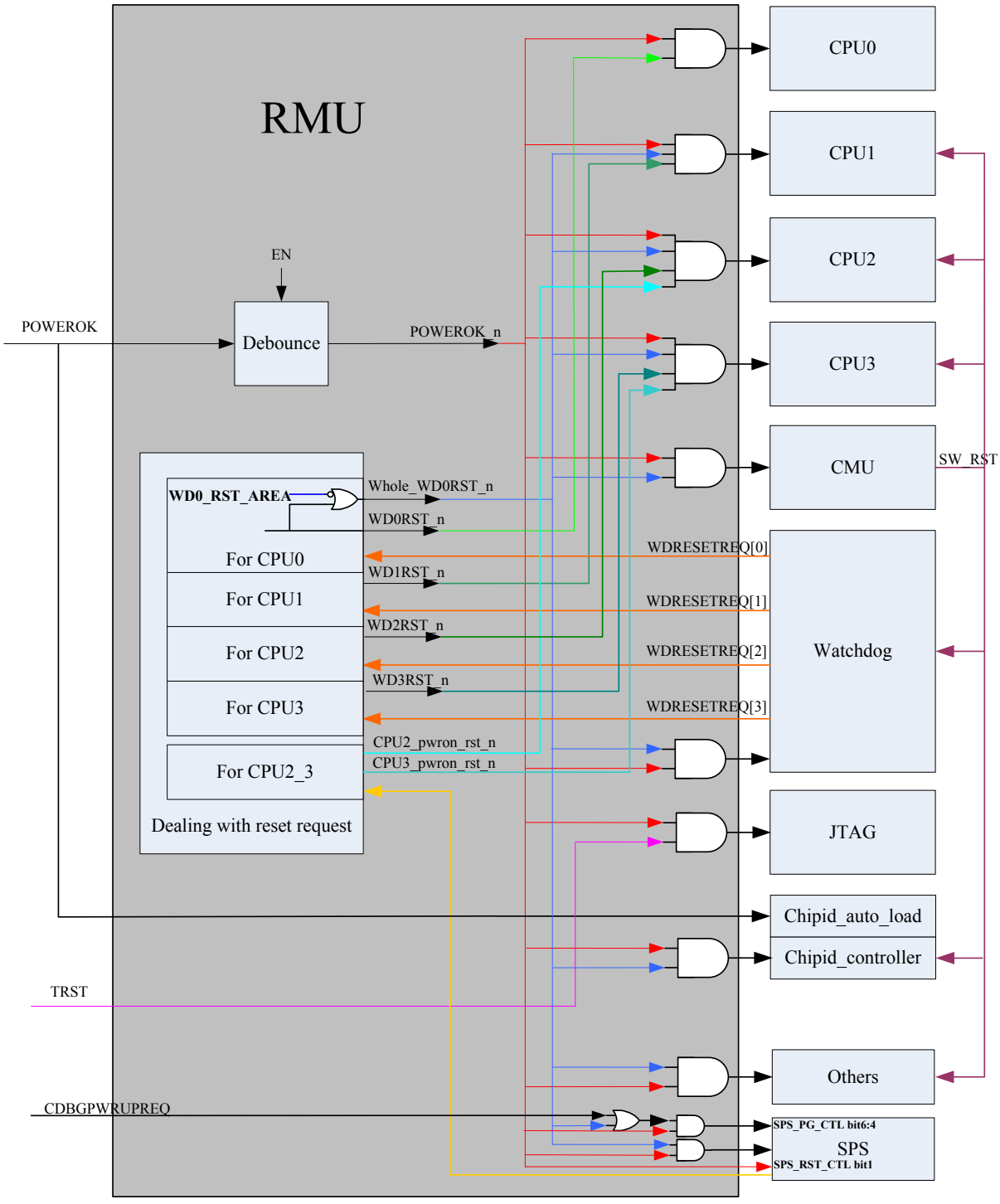


Figure 3-1 RMU Reset Tree

3.3 CMU (Clock Management Unit)

The clock management unit is designed for managing the clocks on S500. Clock originates from three analog sources: 24MHz HOSC (Host Oscillator), 8 PLLs and LOSC 32KHz (Local Oscillator) low frequency oscillator. The digital part of CMU include frequency dividing circuit, clock control circuit and MUX circuit, which are responsible for clock dividing and distributing.
Features are listed below:

- CMU clock source: HOSC, PLL and LOSC.
- The eight PLLs are embedded:
  - CORE_PLL for CPU
  - DDR_PLL for DDR
  - NAND_PLL for NAND Flash
  - DISPLAY_PLL for LCD Displayer
  - AUDIO_PLL for Audio subsystem
  - DEV_PLL for AHB and APB Devices
  - ETHERNET_PLL for external Ethernet block
  - CVBS_PLL is backup for GPU subsystem
- Other PLLs are integrated in the related subsystems, not in CMU, but their control logic is still in CMU. Such subsystems including USB3, USB2, HDMI, MIPI DSI, etc.
- HOSC is the source for all PLLs.

8.1.1 Block Diagram

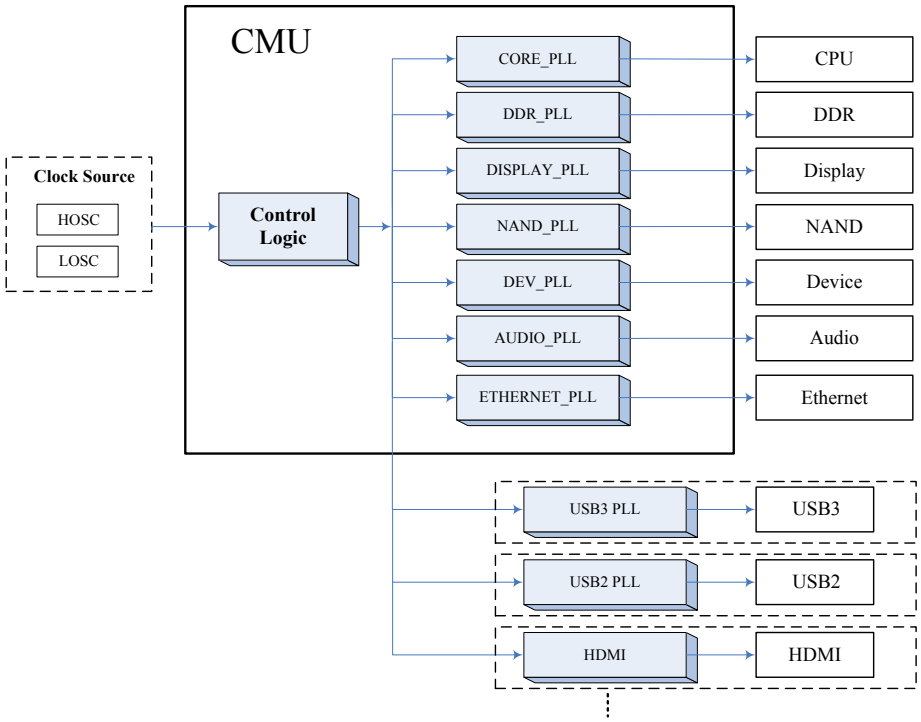


Figure 3-2 CMU Block Diagram

8.1.2 Register List

Table 3-2 CMU Controller Registers Address

Name	Physical Base Address
CMU	0xB0160000

Table 3-3 CMU Controller Registers

Offset	Register Name	Description
0x0020	CMU_SENSORCLK	Sensor Clock Control Register
0x0024	CMU_LCDCLK	LCD Clock Control Register
0x0028	CMU_DSIPLL_CLK	DSI PLL and Clock Control Register

0x002C	CMU_CSICLK	CSI Clock Control Register
0x0030	CMU_DECLK	DE Clock Control Register
0x0034	CMU_SICLK	SI Clock Control Register
0x005C	CMU_UART0CLK	UART0 Clock Control Register
0x0060	CMU_UART1CLK	UART1 Clock Control Register
0x0064	CMU_UART2CLK	UART2 Clock Control Register
0x0068	CMU_PWM4CLK	PWM4 Clock Control Register
0x006C	CMU_PWM5CLK	PWM5 Clock Control Register
0x0070	CMU_PWM0CLK	PWM0 Clock Control Register
0x0074	CMU_PWM1CLK	PWM1 Clock Control Register
0x0078	CMU_PWM2CLK	PWM2 Clock Control Register
0x007C	CMU_PWM3CLK	PWM3 Clock Control Register
0x00A0	CMU_DEVCLKEN0	Device Clock enable Control Register
0x00A4	CMU_DEVCLKEN1	Device Clock enable Control Register
0x00A8	CMU_DEVRST0	Device Reset Control Register
0x00AC	CMU_DEVRST1	Device Reset Control Register
0x00B0	CMU_UART3CLK	UART3 Clock Control Register
0x00B4	CMU_UART4CLK	UART4 Clock Control Register
0x00B8	CMU_UART5CLK	UART5 Clock Control Register
0x00BC	CMU_UART6CLK	UART6 Clock Control Register

8.1.3 Register Description

3.3.1.1 CMU_SENSORCLK

Sensor clock out Control Register
Offset=0x20

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	INVERTER1	INVERTER 1 enable: 0: disable 1: enable	RW	0
12	INVERTER0	INVERTER 0 enable: 0: disable 1: enable	RW	0
11:8	SEN1DIV	Sensor_clkout1 Divisor 0: /1 1: /2 2: /3 …… 11:/12 12,…,15: Reserved 50% duty	RW	0
7:5	-	Reserved	-	-
4	CLKSEL	Sensor clock out source select: 0: HOSC 1: SI_CLK	RW	0
3:0	SEN0DIV	Sensor_clkout0 Divisor 0: /1 1: /2	RW	0

		2: /3 …… 11:/12 12,…,15: Reserved 50% duty		

3.3.1.2 CMU_LCDCLK

LCD_CLK Control Register
Offset=0x24

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13:12	CLKSEL	LCD_CLK source select: 0: DISPLAY_PLL 1: DEV_CLK others: Reserved	RW	0
11. 9	-	Reserved	-	-
8	LCDCLKD	LCD_CLK Divisor: 0:/1 1:/7	RW	0
7. 4	-	Reserved	-	-
3:0	LCD0DIV	LCD0_CLK Divisor 0: /1 1: /2 2: /3 …… 11:/12 12,…,15: Reserved	RW	0

3.3.1.3 CMU_DSIPLL_CLK

DSI_HCLK Control Register
Offset=0x28

Bits	Name	Description	Access	Reset
31:6	-	Reserved	-	-
16	DSI_PLLEN	DSI clock enable 1: DSI PLL enable 0: DSI PLL disable	RW	0
15	-	Reserved	-	-
14:8	DSI_HSCLK	DSI HS clock multiple factor 0-6: Reserved 7:42MHz 8:48MHz 100:600MHz Other: Reserved	RW	0x7
7:2	-	Reserved	-	-
1:0	DIV	DSE_CLK Divisor: 0: /1 1: /2 2: /3 3: /4	RW	0

3.3.1.4 CMU_CSICLK

CSI_CLK Control Register
Offset=0x2C

Bits	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	CLKSEL	CSI_CLK source select: 0: DISPLAY_PLL 1: DEV_CLK	RW	0
3:0	DIV	CSI_CLK Divisor: 0: /1 1: /2 2: /3 …… 11:/12 12,…,15: Reserved	RW	0

3.3.1.5 CMU_DECLK

DE_CLK Control Register
Offset=0x30

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	CLKSEL	DE_CLK source select: 0: DISPLAY_PLL 1: DEV_CLK	RW	0
11:8	-	Reserved	-	-
`	DIV2	DE2_CLK Divisor: 0: /1 1: /1.5 2: /2 3:/2.5 4:/3 5:/4 6:/6 7:/8 8:/12 9…:15:Reserved	RW	0
3:0	DIV1	DE1_CLK Divisor: 0: /1 1: /1.5 2: /2 3:/2.5 4:/3 5:/4 6:/6 7:/8 8:/12 9…:15:Reserved	RW	0

3.3.1.6 CMU_SICLK

SI_CLK Control Register
Offset=0x34

Bits	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	CLKSEL	SI _CLK source select: 0: DISPLAY_PLL 1: DEV_CLK	RW	0
3:0	DIV	SI_CLK Divisor: 0: /1 1: /2 2: /3 …… 11:/12 12,…,15: Reserved	RW	0

3.3.1.7 CMU_UART0CLK

UART0 Clk Control Register
Offset=0x5C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
16	SOURCESEL	UART0 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART0DIV	UART0 Interface Clock Divisor 0: /1 1: /2 2: /3 …… 311: /312 312: /624 313…511: Reserved	RW	0

3.3.1.8 CMU_UART1CLK

UART1 Clk Control Register
Offset=0x60

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	SOURCESEL	UART1 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART1DIV	UART1 Interface Clock Divisor 0: /1 1: /2 2: /3 ……	RW	0

		311: /312 312: /624 313…511: Reserved		

3.3.1.9 CMU_UART2CLK

UART2 Clk Control Register
Offset=0x64

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	SOURCESEL	UART2 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART2DIV	UART2 Interface Clock Divisor 0: /1 1: /2 2: /3 …… 311: /312 312: /624 313…511: Reserved	RW	0

3.3.1.10 CMU_PWM4CLK

PWM2 Interface Clk Control Register
Offset=0x68

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	SRC_SEL	Source select 00: IC_32K 01: HOSC 24M	RW	0
11:10	-	Reserved	-	-
9:0	PWM4CLKDIV	PWM2 Clock Divisor 0: /1 1: /2 2: /3 …… 1023:/1024	RW	0

3.3.1.11 CMU_PWM5CLK

PWM0 Interface Clk Control Register
Offset=0x6C

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	SRC_SEL	Source select 00: IC_32K 01: HOSC 24M	RW	0

11:10	-	Reserved	-	-
9:0	PWM5CLKDIV	PWM3 Clock Divisor 0: /1 1: /2 2: /3 …… 1023:/1024	RW	0

3.3.1.12 CMU_PWM0CLK

PWM0 Interface Clk Control Register
Offset=0x70

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	SRC_SEL	Source select 00: IC_32K 01: HOSC 24M	RW	0
11:10	-	Reserved	-	-
9:0	PWM0CLKDIV	PWM0 Clock Divisor 0: /1 1: /2 2: /3 …… 1023:/1024	RW	0

3.3.1.13 CMU_PWM1CLK

PWM1 Interface Clk Control Register
Offset=0x74

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	SRC_SEL	Source select 00: IC_32K 01: HOSC 24M	RW	0
11:10	-	Reserved	-	-
9:0	PWM1CLKDIV	PWM1 Clock Divisor 0: /1 1: /2 2: /3 …… 1023:/1024	RW	0

3.3.1.14 CMU_PWM2CLK

PWM2 Interface Clk Control Register
Offset=0x78

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	SRC_SEL	Source select 00: IC_32K 01: HOSC 24M	RW	0

11:10	-	Reserved	-	-
9:0	PWM2CLKDIV	PWM2 Clock Divisor 0: /1 1: /2 2: /3 …… 1023:/1024	RW	0

3.3.1.15 CMU_PWM3CLK

PWM0 Interface Clk Control Register
Offset=0x7C

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	SRC_SEL	Source select 00: IC_32K 01: HOSC 24M	RW	0
11:10	-	Reserved	-	-
9:0	PWM3CLKDIV	PWM3 Clock Divisor 0: /1 1: /2 2: /3 …… 1023:/1024	RW	0

3.3.1.16 CMU_DEVCLKEN0

Device Clk Control Register
Offset=0xA0

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	HDMIA	HDMI audio interface clock enable Switch APB_clock and HDMIA_CLK	RW	0
21	I2SRX	I2S interface RX clock enable Switch APB_clock and I2SRX_CLK	RW	0
20	I2STX	I2S interface TX clock enable Switch APB_clock and I2STX_CLK	RW	0
19	-	Reserved	-	-
18	GPIO	GPIO interface clock enable Switch APB_clock	RW	1
17	KEY	KEY interface clock enable Switch APB_clock.	RW	0
16:15	-	Reserved	-	-
14	SI	SI interface clock enable Switch AHB clock and SI_CLK, sensor_clkout0 and sensor_clkout1	RW	0
13	CSI	CSI interface clock enable Switch AHB clock and CSI_CLK	RW	0
12	DSI	DSI interface clock enable	RW	0
11	Pwm4	PWM4 clock enable	RW	0
10	-	Reserved	-	-

9	LCD0	LCD0 interface clock enable Switch AHB clock and LCD0_CLK	RW	0
8	DE	DE interface clock enable Switch AHB clock and DE1_CLK/DE2_CLK/NOC0_CLK	RW	0
7:2	-	Reserved	-	-
0	Pwm5	PWM5 clock enable	RW	0

3.3.1.17 CMU_DEVCLKEN1

Device Clk Control Register
Offset=0xA4

Bits	Name	Description	Access	Reset
31	TWI3	TWI3 interface clock enable Switch APB_clock and special clk (100M)	RW	0
30	TWI2	TWI2 interface clock enable Switch APB_clock and special clk (100M)	RW	0
29:28	-	Reserved	-	-
27	TIMER	TIMER special clock enable	RW	0
26	PWM3	PWM3 special clock enable	RW	0
25	PWM2	PWM2 special clock enable	RW	0
24	PWM1	PWM1 special clock enable	RW	0
23	PWM0	PWM0 special clock enable	RW	0
22	-	Reserved	-	-
21	UART5	UART5 interface clock enable Switch APB_clock and UART5_CLK	RW	0
20	UART4	UART4 interface clock enable Switch APB_clock and UART4_CLK	RW	0
19	UART3	UART3 interface clock enable Switch APB_clock and UART3_CLK	RW	0
18	UART6	UART6 interface clock enable Switch APB_clock and UART6_CLK	RW	0
17:16	-	Reserved	-	-
15	TWI1	TWI1 interface clock enable Switch APB_clock and special clk (100M)	RW	0
14	TWI0	TWI0 interface clock enable Switch APB_clock and special clk (100M)	RW	0
13	SPI3	SPI3 interface clock enable Switch AHB clock	RW	0
12	SPI2	SPI2 interface clock enable Switch AHB clock	RW	0
11	SPI1	SPI1 interface clock enable Switch AHB clock	RW	0
10	SPI0	SPI0 interface clock enable Switch AHB clock	RW	1
9	IRC	Switch IRC special clock(200K).	RW	0
8	UART2	UART2 interface clock enable Switch APB_clock and UART2_CLK	RW	0
7	UART1	UART1 interface clock enable Switch APB_clock and UART1_CLK	RW	0
6	UART0	UART0 interface clock enable Switch APB_clock and UART0_CLK	RW	0

5:0	-	Reserved	-	-

3.3.1.18 CMU_DEVRST0

Device Reset Control Register
Offset = 0xA8

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17	AUDIO	AUDIO control block reset	RW	1
16	-	Reserved	-	-
15	GPIO	GPIO control block reset	RW	1
14	KEY	KEY control block reset	RW	1
13	-	Reserved	-	-
12	SI	SI block reset	RW	1
11	CSI	CSI control block reset	RW	1
10	DSI	DSI control block reset	RW	1
9	-	Reserved	-	-
8	LCD	LCD control block reset	RW	1
7	DE	DE interface reset	RW	1
6	PCM1	PCM1 control block reset	RW	1
5:0	-	Reserved	-	-

NOTE:
1. Write '0' to reset the block.

3.3.1.19 CMU_DEVRST1

Device Reset Control Register
Offset = 0xAC

Bits	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	TWI3	TWI3 control block reset	RW	1
18	TWI2	TWI2 control block reset	RW	1
17	UART5	UART5 control block reset	RW	1
16	UART4	UART4 control block reset	RW	1
15	UART3	UART3 control block reset	RW	1
14	-	Reserved	-	-
13	TWI1	TWI1 control block reset	RW	1
12	TWI0	TWI0 control block reset	RW	1
11	SPI3	SPI3 control block reset	RW	1
10	SPI2	SPI2 control block reset	RW	1
9	SPI1	SPI1 control block reset	RW	1
8	SPI0	SPI0 control block reset	RW	1
7	UART2	UART2 control block reset	RW	1
6	UART1	UART1 control block reset	RW	1
5	UART0	UART0 control block reset	RW	1
4	UART6	UART6 control block reset	RW	1
3:0	-	Reserved	-	-

3.3.1.20 CMU_UART3CLK

UART3 Clk Control Register
Offset=0xB0

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	SOURCESEL	UART3 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART3DIV	UART3 Interface Clock Divisor 0: /1 1: /2 2: /3 …… 311: /312 312: /624 313…511: Reserved	RW	0

3.3.1.21 CMU_UART4CLK

UART4 Clk Control Register
Offset=0xB4

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	SOURCESEL	UART4 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART4DIV	UART4 Interface Clock Divisor 0: /1 1: /2 2: /3 …… 311: /312 312: /624 313…511: Reserved	RW	0

3.3.1.22 CMU_UART5CLK

UART5 Clk Control Register
Offset=0xB8

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
16	SOURCESEL	UART5 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART5DIV	UART5 Interface Clock Divisor 0: /1 1: /2	RW	0

		2: /3 …… 311: /312 312: /624 313…511: Reserved		

3.3.1.23 CMU_UART6CLK

UART6 Clk Control Register
Offset=0xBC

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
16	SOURCESEL	UART6 clock source select 0: HOSC 1: DEV_PLL	RW	0
15. 9	-	Reserved	-	-
8:0	UART6DIV	UART6 Interface Clock Divisor 0: /1 1: /2 2: /3 …… 311: /312 312: /624 313…511: Reserved	RW	0

8.1.4 Application Note

The clocks of each subsystem can be set by relative registers, details about the configuration please refer to the register description and the subsystem chapter.

3.4 2Hz/Timer01

This part includes 2 individual units: 2Hz and Timer0/1, for IRQ generating based on different clock frequency.

8.1.5 Block diagram

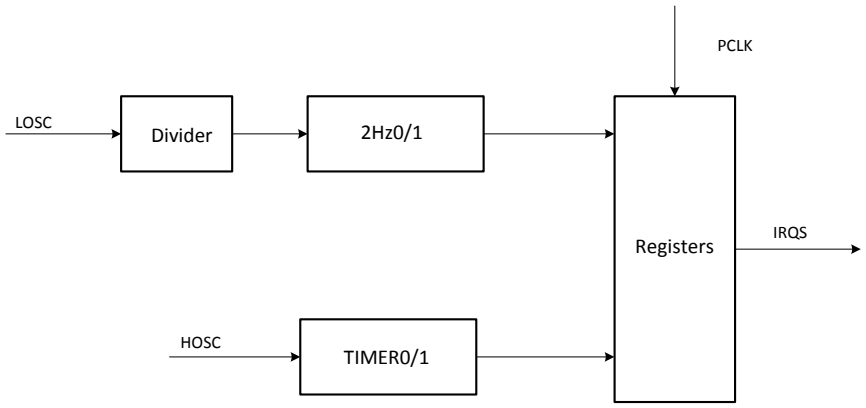


Figure 3-3 2Hz&Timer Block Diagram

8.1.6 Register List

Table 3-4 2Hz/Timer Base Address

Name	Physical Base Address
Timer_2HZ	0xB0168000

Table 3-5 2Hz/Timer Register List

Offset	Register Name	Description
0x0000	TWOHZ0_CTL	2Hz0 Control register
0x0008	T0_CTL	Timer0 Control register
0x000C	T0_CMP	Timer0 Compare Register
0x0010	T0_VAL	Timer0 Value Register
0x0014	T1_CTL	Timer1 Control register
0x0018	T1_CMP	Timer1 Compare Register
0x001C	T1_VAL	Timer1 Value Register
0x0020	TWOHZ1_CTL	2Hz1 Control register

Note: When Setting the 2Hz, TIMER0/1, program must disable the corresponding enable bit at first and then enable it after setting the value

8.1.7 Register Description

3.4.1.1 TWOHZ0_CTL

2Hz0 Control register (VDD)
Offset = 0x0000

Bits	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	2HIE0	2Hz0 IRQ Enable 1:Enable 0:Disable	RW	0
0	2HIP0	2Hz0 IPQ pending bit, writing 1 to this bit will clear it	RW	0

3.4.1.2 T0_CTL

Timer0 Control Register (VDD)
Offset = 0x0008

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	EN	Timer0 Enable 0:Disable,1:Enable	RW	0
1	IRQEN	T0 send IRQ Enable When this bit is enabled, If T0_VAL equals T0_CMP, IRQ signal will be sent out until the IRQ pending bit was cleared.	RW	0
0	PD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

3.4.1.3 T0_CMP

Timer0 compare Register (VDD)
Offset = 0x000C

Bits	Name	Description	Access	Reset
31:0	CMP	compare value	RW	0

3.4.1.4 T0_VAL

Timer0 Value Register (VDD)
Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write current Timer0 value	RW	0

3.4.1.5 T1_CTL

Timer1 Control Register (VDD)
Offset = 0x0014

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	EN	Timer1 Enable 0:Disable,1:Enable	RW	0
1	IRQEN	T1 send IRQ Enable When this bit is enabled, If T1_VAL equals T1_CMP, IRQ signal will be sent out until the IRQ pending bit was cleared.	RW	0
0	PD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

3.4.1.6 T1_CMP

Timer1 compare Register (VDD)
Offset = 0x0018

Bits	Name	Description	Access	Reset
31:0	CMP	compare value	RW	0

3.4.1.7 T1_VAL

Timer1 Value Register (VDD)
Offset = 0x001C

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write current Timer1 value	RW	0

3.4.1.8 TwoHz1_CTL

2Hz1 Control register (VDD)
Offset = 0x0020

Bits	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	2HIE1	2Hz1 IRQ Enable 1:Enable 0:Disable	RW	0
0	2HIP1	2Hz1 IPQ pending bit, writing 1 to this bit will clear it	RW	0

4 SPS (Smart Power System)

4.1 Overview

This part will introduce the power system of S500, it support divided power and voltage domains to distribute stable and adequate power for high-speed digital and sensitive analog circuit. Power domains can be switched on/off states for any combination of power domains to satisfy different power saving modes.

Features of SPS are listed below:

- Support 3 voltage domains
- Support 9 independent power domains which allows ON/OFF states switch according to different application scenarios
- 5 internal LDOs are for analog modules with high precision 1.5V reference voltage

4.2 Block Diagram

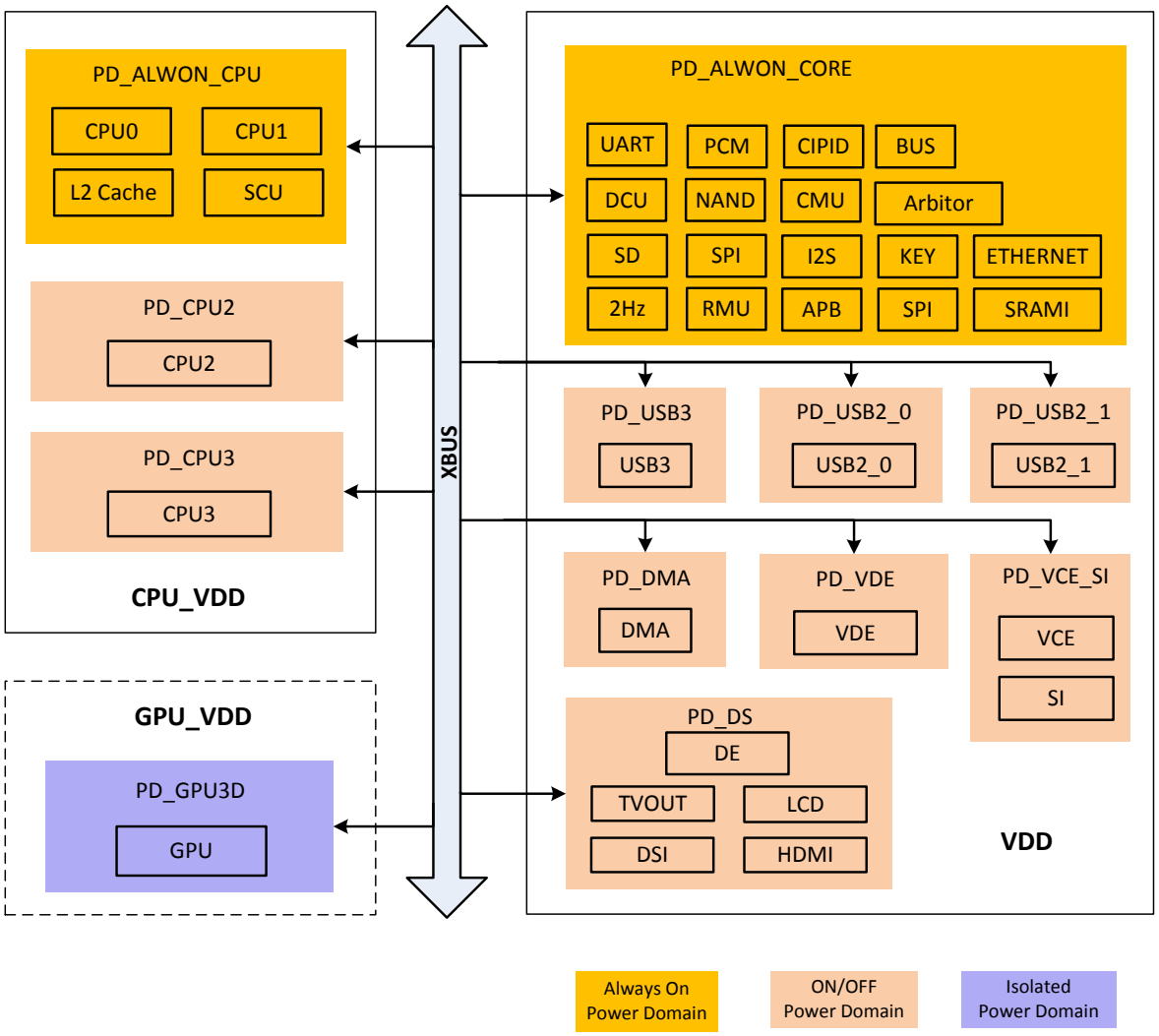


Figure 4-1 S500 Power Domain

In S500, there are nine Power Domains of PD_CPU2, PD_CPU3, PD_VDE PD_VCE_SI, PD_DS, PD_DMA, PD_USB3, PD_USB2_0 and PD_USB2_1, which can be powered off depend on the application, and one Power Domain (PD_GPU3D) can be isolated so that it can be powered off from the supply. The other Power Domains can't be powered off.

Table 4-1 S500 Power Domain and state

Voltage Domain	Power Domain	Module	Block Function	Power State
CPU_VDD	PD_ALWON_CPU	CPU0, CPU1, L2, SCU	ARM MPcore	Always on
	PD_CPU2	CPU2		ON/OFF
	PD_CPU3	CPU3		ON/OFF
GPU_VDD	PD_GPU3D	GPU	GPU	Isolated, can be OFF from the supply
VDD	PD_VDE	VDE	Video Decode & Encode and CMOS Sensor Interface subsystem	ON/OFF
	PD_VCE_SI	VCE, SI		ON/OFF
	PD_DS	DS (DE, LCD, DSI, HDMI, TVOUT)	Display	ON/OFF
	PD_DMA	DMA	Peripherals	ON/OFF
	PD_USB3	USB3	USB Interface	ON/OFF
	PD_USB2_0	USB2_0		ON/OFF

	PD_USB2_1	USB2_1		ON/OFF
	PD_ALWON_CORE	DCU, NAND, SD, SPI, MFP, 2Hz, RMU, CMU, I2S, KEY, BUS Arbitor, APB bridge, Ethernet, SRAMI (BROM), CHIPID, PCM, UGP, TWI, UART, tic, etc.	Peripheral subsystems	Always on

4.3 Power On Sequence

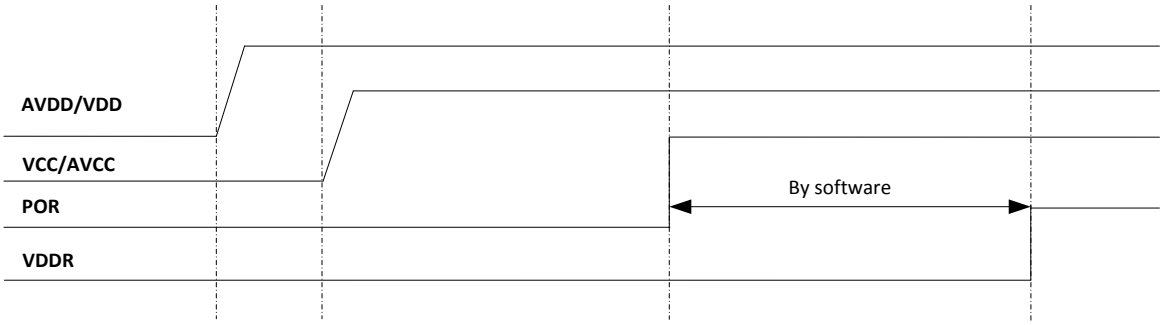


Figure 4-2 Power on Timing Sequence Diagram (Working with ATC260x)

The figure above is the power on sequence of S500 working with Actions' PMU ATC260x, and all the power S500 get is provided by ATC260x. The power on timing sequence can be adjusted on demand of S500. Different types of PMUs adopted, the power on sequence of AVDD/VDD, VCC/AVCC may vary, and the whole power on time will be different.

POR is high meaning the power provided from ATC260x is ready, system clock is steady. Note that VDDR is for DDR, can be configured by software according to the applications.

4.4 Function Description

The S500's power source is mainly provided by Actions' co-chip ATC260x PMU, S500 integrated 5 internal LDOs with high precision 1.5V reference voltage for some blocks such as HDMI and SDIO, etc, and the related control block is also integrated.

4.5 Register List

Table 4-2 SPS Registers Address

Name	Physical Base Address	KSEG1 Base Address
SPS_PG	0x101B0100	0xB01B0100

Table 4-3 SPS Registers

Offset	Register Name	Description
0x0000	SPS_PG_CTL	Power Gating controller Register
0x0004	SPS_RST_CTL	RMU controller register
0x0008	SPS_LDO_CTL	LDO controller register

4.6 Register Description

8.1.8 SPS_PG_CTL

POWER GATING controller Register. (VDD)
Offset=0x0000

Bit(s)	Name	Description	Access	Reset
31:30	PWRCTLO3	Power mode that CPU3 requests 00: CPU3 powered on or powered off 01: Reserved 10: Reserved 11: CPU3 can enter powered-off mode	R	0
29:28	PWRCTLO2	Power mode that CPU2 requests 00: CPU2 powered on or powered off 01: Reserved 10: Reserved 11: CPU2 can enter powered-off mode	R	0
27:23	-	Reserved	-	-
22	ACK_CPU3	CPU3 power on ACK 0: power off 1: power on	R	0
21	ACK_CPU2	CPU2 power on ACK 0: power off 1: power on	R	0
20:19	-	Reserved	-	-
18	ACK_ USB2_1	USB2_1 power on ACK 0: power off 1: power on	R	0
17	ACK_VCE_SI	VCE_SI power on ACK 0: power off 1: power on	R	0
16	ACK_VDE	VDE power on ACK 0: power off 1: power on	R	1
15	ACK_ USB2_0	USB2_0 power on ACK 0: power off 1: power on	R	0
14	ACK_ USB3	USB3 power on ACK 0: power off 1: power on	R	0
13	ACK_DS	DS power on ACK 0: power off 1: power on	R	0
12	ACK_ DMA	DMA power on ACK 0: power off 1: power on	R	0
11	PWR_USB2_0	USB2_0 power on enable Switch USB2_0 power 0: Disable 1: Enable	RW	0
10	PWR_USB3	USB3 power on enable Switch USB3 power 0: Disable 1: Enable	RW	0

9	PWR_DS	DS power on enable Switch DS power 0: Disable 1: Enable	RW	0
8	PWR_DMA	DMA power on enable Switch DMA power 0: Disable 1: Enable	RW	0
7	-	Reserved	-	-
6	PWR_CPU3	CPU3 power on enable Switch CPU3 power 0: Disable 1: Enable	RW	0
5	PWR_CPU2	CPU2 power on enable Switch CPU2 power 0: Disable 1: Enable	RW	0
4	-	Reserved	-	-
3	ISO_GPU3D	GPU3D isolation enable 0: isolation 1: no isolation	RW	0
2	PWR_USB2_1	USB2_1 power on enable Switch USB2_1 power 0: Disable 1: Enable	RW	0
1	PWR_VCE_SI	VCE& SI power on enable Switch VCE& SI power 0: Disable 1: Enable	RW	0
0	PWR_VDE	VDE power on enable Switch VDE power 0: Disable 1: Enable	RW	1

8.1.9 SPS_RST_CTL

RMU controller Register. (VDD)
Offset=0x0004

Bit(s)	Name	Description	Access	Reset
31:2	-	Reserved	RW	0
1	WD0_RST_AREA	Select the area of WDRESETREQ[0]: 0: Only CPU0 1: The Whole Chip (excluding this bit and WDRESET[0])	RW	0
0	POR_FED_EN	POR Falling Edge Debounce Enable: 0: Disable 1: Enable	RW	1

8.1.10 SPS_LDO_CTL

LDO controller Register. (VDD)
Offset=0x0008

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	RW	0
11	MIPI_AVDD_EN	MIPI_AVDD_EN: 0: Disable 1: Enable	RW	0
10:6	MIPI_AVDD_VSEL	MIPI_AVDD voltage control: 00011: 0.775V 10000: 1.100V 00100: 0.800V 10001: 1.125V 00101: 0.825V 10010: 1.150V 00110: 0.850V 10011: 1.175V 00111: 0.875V 10100: 1.200V 01000: 0.900V 10101: 1.225V 01001: 0.925V 10110: 1.250V 01010: 0.950V 10111: 1.275V 01011: 0.975V 11000: 1.300V 01100: 1.000V 11001: 1.325V 01101: 1.025V 11010: 1.350V 01110: 1.050V 11011: 1.375V 01111: 1.075V 11100: 1.400V 10000: 1.100V 11101: 1.425V 10001: 1.125V 11110: 1.450V 10010: 1.150V 11111: 1.475V	RW	0xC
5	USB_AVDD_EN	USB_AVDD_EN: 0: Disable 1: Enable	RW	0
4:0	USB_AVDD_VSEL	USB_AVDD voltage control: 00011: 0.775V 10000: 1.100V 00100: 0.800V 10001: 1.125V 00101: 0.825V 10010: 1.150V 00110: 0.850V 10011: 1.175V 00111: 0.875V 10100: 1.200V 01000: 0.900V 10101: 1.225V 01001: 0.925V 10110: 1.250V 01010: 0.950V 10111: 1.275V 01011: 0.975V 11000: 1.300V 01100: 1.000V 11001: 1.325V 01101: 1.025V 11010: 1.350V 01110: 1.050V 11011: 1.375V	RW	0xC

		01111: 1.075V 11100: 1.400V 10000: 1.100V 11101: 1.425V 10001: 1.125V 11110: 1.450V 10010: 1.150V 11111: 1.475V		

4.7 Application Note

5 MPCore Processor (ARM Cortex-A9R4)

5.1 Overview

The Cortex-A9 R4 MPCore processor is the fourth revision of Cortex-A9 MPcore, it's a high-performance, low-power, ARM macrocell, with L1 cache subsystem that provides full virtual memory capabilities. In S500, the four individual cores are based on Symmetric Multi Processing (SMP) architecture and linked in a cache-coherent cluster, under control of a Snoop Control Unit (SCU), which maintains L1 data cache coherency for shared memory. The Cortex-A9 R4MPCore processor implements the ARMv7-A architecture and runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java™ bytecodes in Jazelle state.

The Cortex-A9 R4 MPCore processor consists of:

- Four Cortex-A9 R4 processors in a cluster and a Snoop Control Unit (SCU) used to ensure coherency within the cluster.
- A set of private memory-mapped peripherals, including a global timer, a watchdog and private timer for each Cortex-A9 R4 processor present in the cluster.
- An integrated Interrupt Controller that is an implementation of the Generic Interrupt Controller (GIC) architecture. The integrated Interrupt Controller registers are in the private memory region of the Cortex-A9 R4 MPCore processor.

5.2 Features

The Cortex-A9 processor includes the following features:

- ARM Cortex-A9 R4 CPU
- Low power and efficient multi-core architecture provides effective single-core, dual-core, and quad-core applications
- Fully comply to ARM cortex V7A instruction set 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative integrated
- Harvard level 1 memory system with MMU (Memory Management Unit) SCU (Snoop Control Unit) interface in charge of memory coherency between the four CPUs
- NEON (advanced SIMD) and VFPv3 D-32 instructions supported, accelerating the performance of multimedia applications such as 3D graphics and image processing
- Support VFP (Vector Floating Point) architecture and compliant with the IEEE 754 standard for floating-point calculation
- In-order pipeline with dynamic branch prediction equipped
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
- Two 64-bit AXI master interfaces with Master 0 for the data side bus and Master 1 for the instruction side bus
- Support for advanced power management with up to three power domains
- Optional Preload Engine
- Optional Jazelle hardware acceleration
- GIC (General Interrupt Controller) support 58 interrupt

L2 Cache

- 512KB L2 Cache, with 16-Way set associative L2 Cache

System Debug:

- Full core-sight debug solution

- ARMv7 Debug architecture
- Support trace with the Program Trace Macrocell (PTM) interface

System Security:

- ARM TrustZone supported

5.3 Block Diagram

Figure below shows the block diagram of S500 implementing four Cortex-A9 R4 CPU cores.

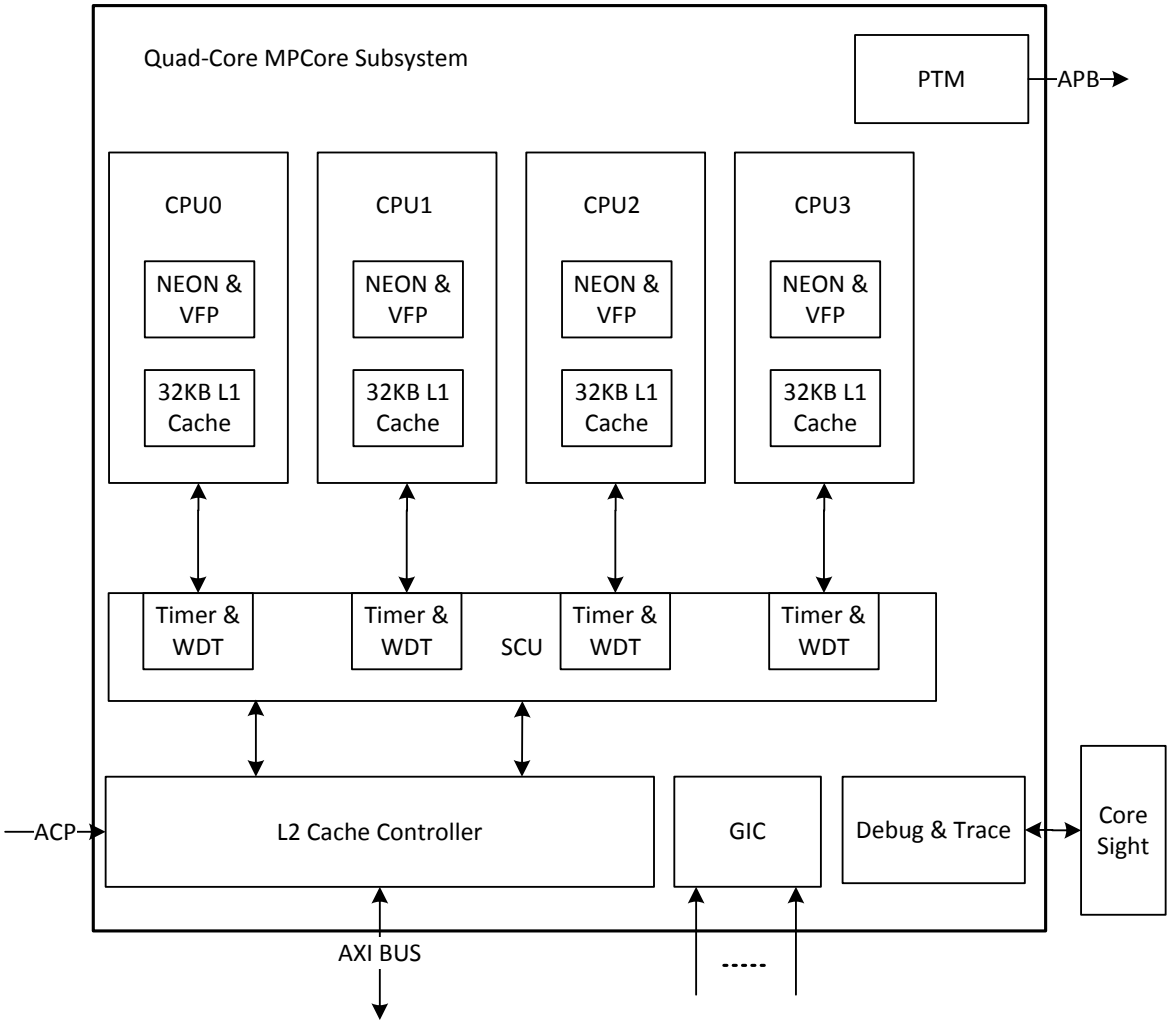


Figure 5-1 Topview of S500 Cortex-A9 R4 CPU MPCore system

5.4 Function Description

8.1.11 Interfaces

The processor has the following external interfaces:

- AXI interface
- APB external debug interface
- Program Flow Trace and Program Trace Macrocell

For more detail, please refer to *<DDI0388H_cortex_a9_r4p0_trm>*

5.4.1.1 AXI Interface

The AXI Interface is short for the AMBA Advanced eXtensible Interface bus protocol. For detail information please refer to <*AMBA AXI™ and ACE™ Protocol Specification*>.

5.4.1.2 PTM interface

The Cortex-A9 processor optionally implements a Program Trace Macrocell (PTM) interface, which is compliant with the Program Flow Trace (PFT) instruction-only architecture protocol. Waypoints, changes in the program flow or events such as changes in context ID, are output to enable the trace to be correlated with the code image. For detailed information, please refer to:
<*IHI0035B_cs_pft_v1_1_architecture_spec*>

8.1.12 SCU (Snoop Control Unit)

The SCU connects between one and four cores in the MPCore processor to the memory system, maintaining data cache coherency between the cores and arbitrating requests from L2 cache and the ACP. The SCU model also support for data security using TrustZone memory model.

8.1.13 GIC (Generic Interrupt Controller)

The Interrupt Controller is a single functional unit that is located in a Cortex-A9 R4 MPCore processor. One processor interface for per core in the processor. The Interrupt Controller is used to collate and arbitrate between a number of different interrupt sources in the system.
Please refer to *Chapter GIC (General Interrupt Controller)* for details about GIC.

8.1.14 L2 Cache and Cache Controller

5.4.1.3 Overview

Level 2 or L2 cache, is an on-chip secondary cache and recognized as a method of improving the performance of ARM-based systems when significant memory traffic is generated by the processor. By definition a secondary cache assumes the presence of a Level 1 or primary cache, closely coupled or internal to the processor.
The Level 2 Cache Controller (L2C) used in S500 works efficiently with ARM processors that implement AXI interfaces. It directly interfaces on the data and instruction interface. It features TrustZone architecture and AMBA AXI interface for enhanced OS security and high performance system.
The cache controller is a unified, physically addressed, physically tagged cache with up to 16 ways. You can lock the replacement algorithm on a way basis, enabling the associativity to be reduced from 16-way down to 1-way (direct mapped). The cache controller does not have snooping hardware to maintain coherency between caches, so the memory coherency is maintained by software. For more information about L2 Cache, please refer to <*DDI0246G_l2c310_trm*>.

5.4.1.4 Features

The L2 cache controller in S500 has the following features:

- 512KB L2 cache in S500
- Physically addressed and physically tagged.
- Lockdown format C (or way locking) supported, for data and instructions.
- Direct mapped to 16-way associativity, depending on the configuration and the use of lockdown

registers. The associativity is RTL configurable as 16.
- Fixed line length of 32 bytes, 256 bits.
- Interface to data RAM is byte writable.
- Banking on data RAM supported.
- Supports all AXI cache modes
- TrustZone support, with the following features:
  - Non-Secure (NS) tag bit added in tag RAM and used for lookup in the same way as an address bit. The NS-tag bit is added in all buffers.
  - Restrictions for NS accesses for control, configuration, and maintenance registers to restrict access to secure data.

5.4.1.5 Application Notes

Cache Initialization:

A typical cache controller start-up programming sequence consists of the following register operations:

1. Write to the Auxiliary, Tag RAM Latency, Data RAM Latency, Prefetch, and Power Control registers using a read-modify-write to set up global configurations:
   - associativity, Way Size
   - latencies for RAM accesses
   - allocation policy
   - prefetch and power capabilities.
2. Secure write to the Invalidate by Way, offset 0x77C, to invalidate all entries in cache:
   - Write 0xFFFF to 0x77C
   - Poll cache maintenance register until invalidate operation is complete.
3. Write to the Lockdown D and Lockdown I Register 9 if required.
4. Write to interrupt clear register to clear any residual raw interrupts set.
5. Write to the Interrupt Mask Register if you want to enable interrupts.
6. Write to Control Register 1 with the LSB set to 1 to enable the cache.

If you write to the Auxiliary, Tag RAM Latency, or Data RAM Latency Control Register with the L2 cache enabled, this results in a SLVERR. You must disable the L2 cache by writing to the Control Register 1 before writing to the Auxiliary, Tag RAM Latency, or Data RAM Latency Control Register.

6 DMA (Direct Memory Access)

6.1 Overview

The S500 DMA is the data transmission engine for CPU system memory and peripheral slaves including AXI, AHB and APB. The AXI slave devices include DDR, ShareRAM, NAND FLASH, SD/MMC, HDCP2.0. AHB slave consist of SRAMI, SPI, and HDCP.
The DMA support 4 interrupt lines, and the 12 logic channels that can be mapped to one of the 4 lines by software configuration, each channel has a set of independent configuration registers. 32 bytes burst transfer, 4 read outstanding requests, link list mode transfers are supported.

6.2 Block Diagram

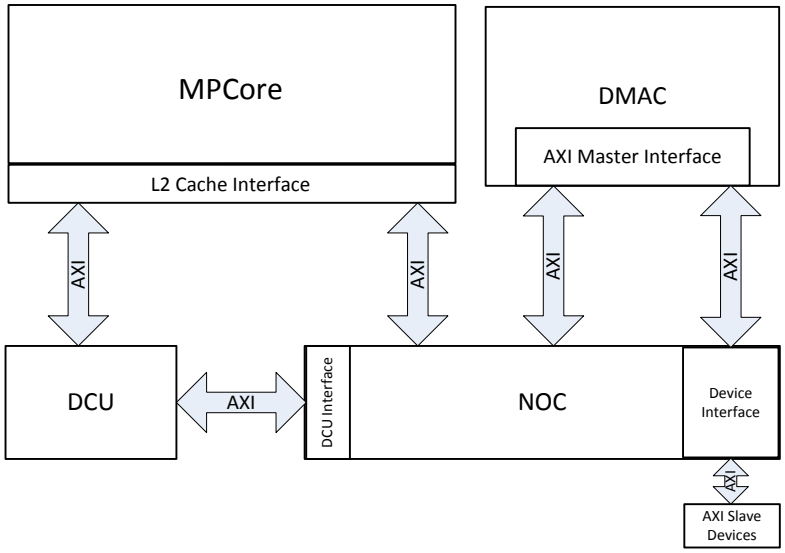


Figure 6-1 DMA Block Diagram

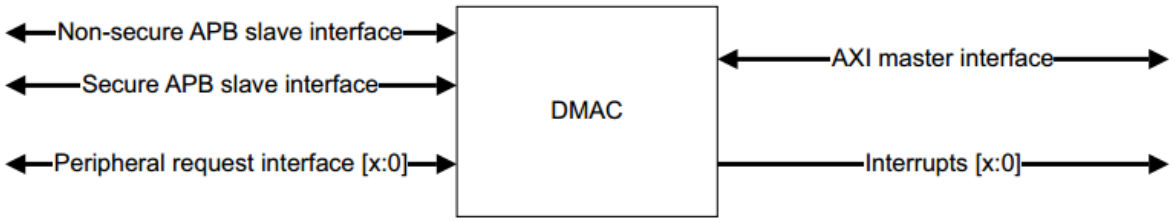


Figure 6-2 Interfaces on DMAC

As shown in the figures above, DMA suppot transfers between memories and peripherals without intervention from CPUs. DMA has two interfaces to NOC, one access DCU directly, the other access the devices through device Interface on NOC.

6.3 Function Description

DMA support 4 software programmable interrupt lines. Interrupt events include: super block transmission complete (for link list), block transmission complete, frame transmission complete, half of frame transmission

complete, start of last frame transmission complete, and address unaligned error. DMA receives request trigger from sources listed in the table below.

Table 6-1 The DRQ (DMA Request) trigger source table

DRQ Source	DRQ_Trig Field(5bit)	DRQ Connect	Simultaneous Task num	FIFO Depth	FIFO Wide	DRQ Threshold	Operation Wide
DCU	0	DRQ0	>2(SRC|DST)	RAM	32	Always	64
ShareRAM	1	DRQ1	>2(SRC|DST)	0	0	Always	64
SD0	2	DRQ2	1(SRC|DST)	512B	32	8	32
SD1	3	DRQ3	1(SRC|DST)	512B	32	8	32
SD2	4	DRQ4	1(SRC|DST)	512B	32	8	32
-	5	Reserved	-	-	-	-	-
NAND	6	DRQ6	1(SRC|DST)	1KB	0	0	32
I2S_t	7	DRQ7	1(DST)	32	24	16	32
I2S_r	8	DRQ8	1(SRC)	16	24	8	32
PCM0_t	9	DRQ9	1(DST)	16	16	16	32
PCM0_r	10	DRQ10	1(SRC)	16	16	8	32
PCM1_t	11	DRQ11	1(DST)	16	16	16	32
PCM1_r	12	DRQ12	1(SRC)	16	16	8	32
SPDIF	13	DRQ13	1(DST)	32	24	16	32
HDMIaudio	14	DRQ14	1(DST)	32	24	16	32
I2STX_SPDIF_HDMI	15	DRQ15	1(DST)	32	24	16	32
UART0_t	16	DRQ16	1(DST)	16	8	1	32
UART0_r	17	DRQ17	1(SRC)	32	8	1	32
UART1_t	18	DRQ18	1(DST)	16	8	1	32
UART1_r	19	DRQ19	1(SRC)	32	8	1	32
UART2_t	20	DRQ20	1(DST)	16	8	1	32
UART2_r	21	DRQ21	1(SRC)	32	8	1	32
UART3_t	22	DRQ22	1(DST)	16	8	1	32
UART3_r	23	DRQ23	1(SRC)	32	8	1	32
UART4_t	24	DRQ24	1(DST)	16	8	1	32
UART4_r	25	DRQ25	1(SRC)	32	8	1	32
UART5_t	26	DRQ26	1(DST)	16	8	1	32
UART5_r	27	DRQ27	1(SRC)	32	8	1	32
SPI0_t	28	DRQ28	1(DST)	32	32	16	32
SPI0_r	29	DRQ29	1(SRC)	32	32	16	32
SPI1_t	30	DRQ30	1(DST)	32	32	16	32
SPI1_r	31	DRQ31	1(SRC)	32	32	16	32
SPI2_t	32	DRQ32	1(DST)	32	32	16	32
SPI2_r	33	DRQ33	1(SRC)	32	32	16	32
SPI3_t	34	DRQ34	1(DST)	32	32	16	32
SPI3_r	35	DRQ35	1(SRC)	32	32	16	32
DSI_t	36	DRQ36	1(SRC)	32	32	11/16	32
DSI_r	37	DRQ37	1(DST)	32	32	11/16	32
SRAMI	38	DRQ38	>2(SRC|DST)	0	0	0	32
-	39	Reserved	-	-	-	-	-
TSIF	40	DRQ40	1(SRC)	4	32	1	32
UART6_t	42	DRQ42	1(DST)	16	8	1	32
UART6_r	43	DRQ43	1(SRC)	32	8	1	32
HDCP2_r	44	DRQ44	1(DST)	12	32	8	32
HDCP2_t	45	DRQ45	1(SRC)	12	32	8	32

6.4 Register List

Table 6-2 DMA Controller Registers Address

Name	Physical Base Address
DMA_GLOBAL	0xB0260000
DMA0	0xB0260100
DMA1	0xB0260200
DMA2	0xB0260300
DMA3	0xB0260400
DMA4	0xB0260500
DMA5	0xB0260600
DMA6	0xB0260700
DMA7	0xB0260800
DMA8	0xB0260900
DMA9	0xB0260A00
DMA10	0xB0260B00
DMA11	0xB0260C00

Table 6-3 DMA Controller Registers

Offset	Register Name	Description
0x0000	DMA_IRQ_PD0	DMA IRQ Pending 0 Register
0x0004	DMA_IRQ_PD1	DMA IRQ Pending 1 Register
0x0008	DMA_IRQ_PD2	DMA IRQ Pending 2 Register
0x000C	DMA_IRQ_PD3	DMA IRQ Pending 3 Register
0x0010	DMA_IRQ_EN0	DMA IRQ enable 0 Register
0x0014	DMA_IRQ_EN1	DMA IRQ enable 1 Register
0x0018	DMA_IRQ_EN2	DMA IRQ enable 2 Register
0x001C	DMA_IRQ_EN3	DMA IRQ enable 3 Register
0x0024	DMA_NOC_QOS	QOS of DMA to NOC

Table 6-4 DMA Logical Channel Controller Registers

Offset	Register Name	Description
0x0000	DMAx_MODE	Mode Register
0x0004	DMAx_SOURCE	Source address Register
0x0008	DMAx_DESTINATION	Destination Address Register
0x000C	DMAx_FRAME_LEN	Frame Length Register
0x0010	DMAx_FRAME_CNT	Frame Count Register
0x0014	DMAx_REMAIN_FRAME_CNT	Remain Frames in the Current Block
0x0018	DMAx_REMAIN_CNT	Remain Count in the Current Frame
0x001C	DMAx_SOURCE_STRIDE	Source Stride Register
0x0020	DMAx_DESTINATION_STRIDE	Destination Stride Register
0x0024	DMAx_START	Start DMA demand
0x002C	DMAx_CHAINED_CTL	Chained Control Register
0x0030	DMAx_CONSTANT	Constant Fill Mode Data Register
0x0034	DMAx_LINKLIST_CTL	Link list Control Register
0x0038	DMAx_NEXT_DESCRIPTOR	Link list Next DESCRIPTOR Pointer Register
0x003C	DMAx_CURRENT_DESCRIPTOR_NUM	Link list Next DESCRIPTOR Pointer Register
0x0040	DMAx_INT_CTL	Interrupt Control Register

0x0044	DMAx_INT_STATUS	Interrupt Status Register
0x0048	DMAx_CURRENT_SOURCE_POINTER	Current Source Pointer Register
0x004C	DMAx_CURRENT_DESTINATION_POINTER	Current Destination Pointer Register

6.5 Register Description

8.1.15 DMA_IRQ_PDx

DMA IRQx Pending Register
Offset=0x0000+x*0x0004, 0≤x≤3

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	DMA11PD	DMA11 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA11 has no interrupt request on interrupt line x 1:DMA11 has interrupt request on interrupt line x	RW	0
10	DMA10PD	DMA10 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA10 has no interrupt request on interrupt line x 1:DMA10 has interrupt request on interrupt line x	RW	0
9	DMA9PD	DMA9 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA9 has no interrupt request on interrupt line x 1:DMA9 has interrupt request on interrupt line x	RW	0
8	DMA8PD	DMA8 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA8 has no interrupt request on interrupt line x 1:DMA8 has interrupt request on interrupt line x	RW	0
7	DMA7PD	DMA7 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA7 has no interrupt request on interrupt line x 1:DMA7 has interrupt request on interrupt line x	RW	0
6	DMA6PD	DMA6 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA6 has no interrupt request on interrupt line x 1:DMA6 has interrupt request on interrupt line x	RW	0
5	DMA5PD	DMA5 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA5 has no interrupt request on interrupt line x 1:DMA5 has interrupt request on interrupt line x	RW	0
4	DMA4PD	DMA4 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA4 has no interrupt request on interrupt line x 1:DMA4 has interrupt request on interrupt line x	RW	0
3	DMA3PD	DMA3 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA3 has no interrupt request on interrupt line x 1:DMA3 has interrupt request on interrupt line x	RW	0
2	DMA2PD	DMA2 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA2 has no interrupt request on interrupt line x	RW	0

		1:DMA2 has interrupt request on interrupt line x		
1	DMA1PD	DMA1 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA1 has no interrupt request on interrupt line x 1:DMA1 has interrupt request on interrupt line x	RW	0
0	DMA0PD	DMA0 Interrupt Pending:(write 1 to reset, write 0 takes no effect) 0:DMA0 has no interrupt request on interrupt line x 1:DMA0 has interrupt request on interrupt line x	RW	0

8.1.16 DMA_IRQ_ENx

DMA IRQx Enable Register
Offset=0x0010+x*0x0004, 0≤x≤3

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	DMA11IRQEN	DMA11 Interrupt Enable: 0:DMA11 disabled interrupt on interrupt line x 1:DMA11 enabled interrupt on interrupt line x	RW	0
10	DMA10IRQEN	DMA10 Interrupt Enable: 0:DMA10 disabled interrupt on interrupt line x 1:DMA10 enabled interrupt on interrupt line x	RW	0
9	DMA9IRQEN	DMA9 Interrupt Enable: 0:DMA9 disabled interrupt on interrupt line x 1:DMA9 enabled interrupt on interrupt line x	RW	0
8	DMA8IRQEN	DMA8 Interrupt Enable: 0:DMA8 disabled interrupt on interrupt line x 1:DMA8 enabled interrupt on interrupt line x	RW	0
7	DMA7IRQEN	DMA7 Interrupt Enable: 0:DMA7 disabled interrupt on interrupt line x 1:DMA7 enabled interrupt on interrupt line x	RW	0
6	DMA6IRQEN	DMA6 Interrupt Enable: 0:DMA6 disabled interrupt on interrupt line x 1:DMA6 enabled interrupt on interrupt line x	RW	0
5	DMA5IRQEN	DMA5 Interrupt Enable: 0:DMA5 disabled interrupt on interrupt line x 1:DMA5 enabled interrupt on interrupt line x	RW	0
4	DMA4IRQEN	DMA4 Interrupt Enable: 0:DMA4 disabled interrupt on interrupt line x 1:DMA4 enabled interrupt on interrupt line x	RW	0
3	DMA3IRQEN	DMA3 Interrupt Enable: 0:DMA3 disabled interrupt on interrupt line x 1:DMA3 enabled interrupt on interrupt line x	RW	0
2	DMA2IRQEN	DMA2 Interrupt Enable: 0:DMA2 disabled interrupt on interrupt line x 1:DMA2 enabled interrupt on interrupt line x	RW	0
1	DMA1IRQEN	DMA1 Interrupt Enable: 0:DMA1 disabled interrupt on interrupt line x 1:DMA1 enabled interrupt on interrupt line x	RW	0
0	DMA0IRQEN	DMA0 Interrupt Enable: 0:DMA0 disabled interrupt on interrupt line x 1:DMA0 enabled interrupt on interrupt line x	RW	0

8.1.17 DMA_NOC_QOS

Value of DMA QOS for noc
Offset=0x0024

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:4	DMA_QOS_CRITICAL	Qos value when critical set	RW	0
3:0	DMA_QOS_NORMAL	Qos value when critical not set	RW	0

Note:when DMA channel is not set critical, QOS using DMA_QOS_NORMAL, when the channel set critical, QOS transmission uses DMA_QOS_NORMAL.

8.1.18 DMA_IDLE_STAT

DMA restart ok status register
Offset=0x002C

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	CH_IDLE_STATUS	Channel idle status, high means this channel is idle	R	0xFFF

8.1.19 DMAx_MODE

DMAx Mode Register
Offset=0x0100+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31	CME	Chained Mode Enable: 0:Disable 1:Enable	RW	0
30	LME	Link list Mode Enable: 0:Disable 1:Enable	RW	0
29	CFE	Constant Fill Mode Enable: 0:Disable 1:Enable	RW	0
28	NDDBW	NOC Device Data Bus Width: 0:32 1:8 (only for UART byte transfer, not applicable for other device)	RW	0
27:24	-	Reserved	-	-
23	CB	Critical Bit:(only take effect in AXI ID field) 0:Identify the request sent to DCU as non-real time request 1:Identify the request sent to DCU as real time request	RW	0
22:20	PW	Priority Weight:N 0:1 1:2 2:4 3:8 4:16 5:32 6:64 7:128	RW	0

19:18	DAM	Destination Address Mode: 0:Constant 1:Increment 2:Stride 3:Reserved	RW	0
17:16	SAM	Source Address Mode: 0:Constant 1:Increment 2:Stride 3:Reserved	RW	0
15:12	-	Reserved	-	-
11:10	DT	Destination Type: 0:Device 1:Reserved 2:DCU 3:ShareRAM	RW	0
9:8	ST	Source Type: 0:Device 1:Reserved 2:DCU 3:ShareRAM	RW	0
7:6	-	Reserved	-	-
5:0	TS	Trigger Source: Refer to the 2nd column of Trig source Table, named DRQ connect	RW	0

8.1.20 DMAx_SOURCE

DMAx Source Register
Offset=0x0104+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DSA	DMA Source Address	RW	0

8.1.21 DMAx_DESTINATION

DMAx Destination Register
Offset=0x0108+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DDA	DMA Destination Address	RW	0

8.1.22 DMAx_FRAME_LEN

DMAx Frame Length Register
Offset=0x010C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19:0	DFL	DMA Frame Length (by bytes)	RW	0

8.1.23 DMAx_FRAME_CNT

DMAx Frame Count Register
Offset=0x0110+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	DFC	DMA Frame Count (by frames)	RW	0

Note:limitations about the transmission length and address aligning are listed below:

1. *If logic channel is constant fill mode, frame length must be multiples of 4-byte*
2. *Device only support constant mode as writing port*
3. *As APB device address is 32-bit, so when APB device using DMA, the frame length should be multiples of word size.*
4. *Srami access must be word aligned, and frame length must be multiples of word size*

Besides all these limitations, address is not request to be aligned; frame length and stride are not limited.

8.1.24 DMAx_REMAIN_FRAME_CNT

DMAx Remain Frame Count Register
Offset=0x0114+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	DTRC	DMA Remain Frame Count in the Current Block (by frames)	R	0

8.1.25 DMAx_REMAIN_CNT

DMAx Current Frame Remain Count Register
Offset=0x0118+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19:0	DCFRC	DMA Remain Count in the Current Frame (by bytes)	R	0

8.1.26 DMAx_SOURCE_STRIDE

DMAx Source Stride Register
Offset=0x011C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DSS	DMA Source Stride (by bytes)	RW	0

8.1.27 DMAx_DESTINATION_STRIDE

DMAx Destination Stride Register
Offset=0x0120+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DDS	DMA Destination Stride (by bytes)	RW	0

8.1.28 DMAx_START

DMAx Start Register
Offset=0x0124+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	DSE	DMA Start Enable: 0:Disable 1:Enable *Note:* *After a transfer has been finished, the bit will be auto cleared. Writing 0 to START bit can terminate this DMA task whenever transfer is going on.*	RW	0

8.1.29 DMAx_CHAINED_CTL

DMAx Chained Control Register
Offset=0x012C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	NLCN	Next Logical Channel Number (which will be hardware auto started after this DMA task finishes)	RW	0

8.1.30 DMAx_CONSTANT

DMAx Constant Data Register
Offset=0x0130+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DCD	DMA Constant Data	RW	0

8.1.31 DMAx_LINKLIST_CTL

DMAx Link list Control Register
Offset=0x0134+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	SUSPEND	Suspend the linked-list transfer at completion of the current block transfer. 0x0:Linked list is active. 0x1:Linked list is suspended at the boundary of next descriptor loading.	RW	0
15:12	-	Reserved	-	-
11:10	DAV	Destination Address Valid 0x0:The destination address is not present in the next descriptor and continuous incrementing is enabled. 0x1:The destination address must be reloaded in the next descriptor transfer. 0x2:The destination start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous	RW	0

		descriptor. 0x3:Reserved		
9:8	SAV	Source Address Valid 0x0:The source address is not present in the next descriptor and continuous incrementing is enabled. 0x1:The source address must be reloaded in the next descriptor transfer. 0x2:The source start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3:Reserved	RW	0
7:2	-	Reserved	-	-
1:0	NDT	Next Descriptor Type: 0:Type 0 1:Type 1 2:Type 2 3:Reserved	RW	0

8.1.32 DMAx_NEXT_DESCRIPTOR

DMAx Next DESCRIPTOR Register
Offset=0x0138+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:2	NDP	Next Descriptor Pointer: This register contains the Next descriptor Address Pointer for the link list	RW	0
1:0	-	Reserved	-	-

8.1.33 DMAx_CURRENT_DESCRIPTOR_NUM

DMAx Current Descriptor Number Register
Offset=0x013C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	NDP	This register contains the current active descriptor number in the link list when it is read	R	0

8.1.34 DMAx_INT_CTL

DMAx Interrupt Control Register
Offset=0x0140+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	ESTE	Enable the Secure Transaction Error Event Interrupt: 0:Disable 1:Enable	RW	0
5	EAME	Enable the Address Misaligned Error Event Interrupt: 0:Disable 1:Enable	RW	0
4	ELF	Enable Last Frame Interrupt (start of last frame): 0:Disable	RW	0

		1:Enable		
3	EEHF	Enable End of Half Frame Interrupt: 0:Disable 1:Enable	RW	0
2	EEF	Enable End of Frame Interrupt: 0:Disable 1:Enable	RW	0
1	EESB	Enable End of Super Block Interrupt: 0:Disable 1:Enable	RW	0
0	EEB	Enable End of Block Interrupt: 0:Disable 1:Enable	RW	0

8.1.35 DMAx_INT_STATUS

DMAx Interrupt Status Register
Offset=0x0144+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	STE	the Secure Transaction Error Event Interrupt: 0:Not Take Place 1:Take Place	RW	0
5	AME	the Address unaligned Error Event Interrupt: 0:Not Take Place 1:Take Place	RW	0
4	LF	Last Frame Interrupt (start of last frame): 0:Not Take Place 1:Take Place	RW	0
3	EHF	End of Half Frame Interrupt: 0:Not Take Place 1:Take Place	RW	0
2	EF	End of Frame Interrupt: 0:Not Take Place 1:Take Place	RW	0
1	ESB	End of Super Block Interrupt: 0:Not Take Place 1:Take Place	RW	0
0	EB	End of Block Interrupt: 0:Not Take Place 1:Take Place	RW	0

8.1.36 DMAx_CURRENT_SOURCE_POINTER

DMAx Current Source Pointer Register
Offset=0x0148+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DCSP	DMA Current Source Pointer	R	0

8.1.37 DMAx_CURRENT_DESTINATION_POINTER

DMAx Current Destination Pointer Register
Offset=0x014C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DCDP	DMA Current Destination Pointer	R	0

6.6 Application Note

1. To enable the pending register DMA_IRQ_PDx of DMA, either DMA_IRQ_ENx or DMA_INT_CTLx should be configured.
2. DMA send 4 interrupts to CPU, DMA_IRQ_PDx will be checked when process the interrupt.
3. Super block interrupt is for linklist mode, there's no such interrupt for chain mode.
4. Since APB Slave address is 32-bit, so the framelength of APB device should be integral multiple of word.
5. SRAMI accessing address should be word aligned, and framelenght should be integral multiple of word.
6. When the source is memory, and source address is not 32byte aligned, the maximum length of a frame is 0xFFFE0.
7. If a block transmits multiple frames, DMAx_FRAME_CNT should be set larger than 1, and either the source address type or destination address type should be set as stride type. If neither the source address type nor the destination address type is stride, though DMAx_FRAME_CNT is larger than 1, DMA only transmit one frame.

7 GIC (General Interrupt Controller)

7.1 Overview

The General Interrupt Controller (GIC) is a single function and AMBA compliant peripheral that located in a Cortex-A9 R4 MPCore processor. There is one processor interface per core in the processor. The Interrupt Controller is used to collate and arbitrate between a number of different interrupt sources in the system. The GIC in S500 support 58 interrupt lines.
The interrupt sources can be masked and prioritized before being distributed to the appropriate cores in the processor. The Interrupt Controller programmers' model also enables interrupts to be generated directly from software. The Cortex-A9 R4 MPCore processor has the interrupt types of SGI, PPI, SPI and LSPI.

7.2 Block Diagram

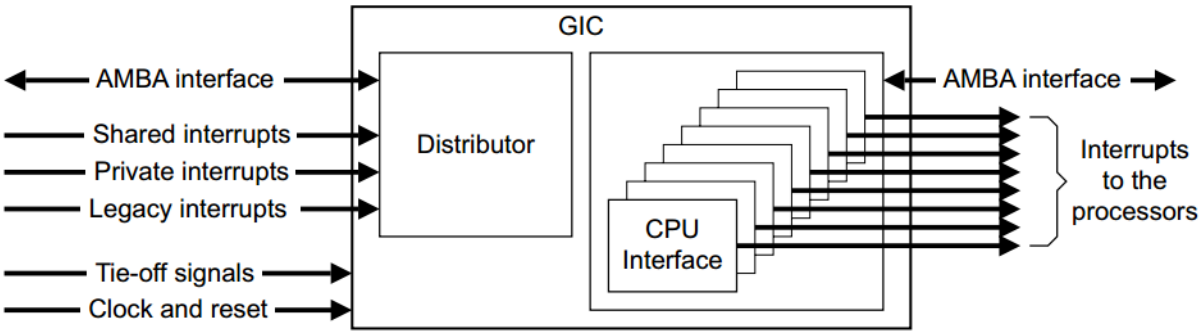


Figure 7-1 Interfaces on the GIC

Interfaces available on GIC are shown in the figure above, in which the AMBA interface can be configured as AXI or AHB, and the CPU Interfaces number is also configurable.Two kinds of IRQ and FIQ interrupts are supported.

7.3 Function Description

8.1.38 Software Generated Interrupt (SGI)

Each core in the Cortex-A9 MPCore processor has private interrupts, ID0-ID15, that can only be triggered by software. These interrupts are aliased so that there is no requirement for a requesting core to determine its own CPU ID when it deals with SGIs. The priority of an SGI depends on the value set by the receiving core in the banked SGI priority registers, not the priority set by the core sending the request.
SGIs are Generated by writing to the Software Generated Interrupt Register (ICDSGIR).
A maximum of 16 SGIs can be generated for each processor interface.

8.1.39 Private Peripheral Interrupt (PPI)

An interrupt generated by a peripheral that is specific to a single core in the processor. There are 5 PPIs for each processor interface.

Legacy nIRQ signal, PPI[4]
In legacy IRQ mode, the external nIRQ[3:0] signal bypasses the interrupt distributor logic and directly drives interrupt requests into the appropriate core in the processor. When a core uses the Interrupt Controller, rather than the legacy IRQ signal, by enabling its own processor interface, the nIRQ[3:0] signal is treated like other interrupt lines and uses ID31.
The bits are read-only and a bit-pair always reads as b01. Interrupt is active LOW level sensitive.
Watchdog timers, PPI[3]
Each processor has its own watchdog timers that can generate interrupts, using ID30.
The bits are read-only and a bit-pair always reads as b11. Interrupt is rising-edge sensitive.
Private timer, PPI[2]
Each processor has its own private timers that can generate interrupts, using ID29.
The bits are read-only and a bit-pair always reads as b11. Interrupt is rising-edge sensitive.
Legacy nFIQ[3:0] signal, PPI[1]
In legacy FIQ mode, the external nFIQ[3:0] signal bypasses the interrupt distributor logic and directly drives interrupt requests into the appropriate core in the processor. When a core uses the Interrupt Controller, rather than the legacy FIQ signal, by enabling its own processor interface, the nFIQ[3:0] signal is treated like other interrupt lines and uses ID28.
The bits are read-only and a bit-pair always reads as b01. Interrupt is active LOW level sensitive.
Global timer, PPI[0]
The global timer can generate interrupts using ID27 which is common across all cores in the processor. Interrupt is rising-edge sensitive.

8.1.40 Shared Peripheral Interrupt (SPI)

An interrupt generated by a peripheral that the Interrupt Controller can route to any, or all, processor interfaces.
SPIs are triggered by events generated on associated interrupt input lines. The Interrupt Controller can support up to 224 interrupt input lines corresponding to the external signal INT[223:0]. The interrupt input lines can be configured to be edge sensitive (posedge) or level sensitive (high level). SPIs start at ID32. The Cortex-A9 MPCore processor can be configured with a range of supported SPIs from 0 up to 224.
The LSB of a bit-pair is read-only and is always b1. You can program the MSB of the bit-pair to alter the triggering sensitivity as follows:
b01 interrupt is active LOW level sensitive
b11 interrupt is active HIGH level sensitive.

Table There are 58 SPIs in S500, as shown below:

Table 7-1 SPIs List

Interrupt ID	Sources	Type
ID32	Ethernet	Low Level
ID33	DE(Display Engine)	Low Level
ID34	Reserved	Low Level
ID35	GPU_3D	Low Level
ID36	PC0(CPU0 PMU interrupt)	Low Level
ID37	PC1(CPU1 PMU interrupt)	Low Level
ID38	PC2(CPU2 PMU interrupt)	Low Level
ID39	PC3(CPU3 PMU interrupt)	Low Level
ID40	2Hz0	Low Level
ID41	2Hz1	Low Level
ID42	Timer0	Low Level
ID43	Timer1	Low Level

ID44	SI	Low Level
ID45	SIRQ0	Low Level
ID46	SIRQ1	Low Level
ID47	SIRQ2	Low Level
ID48	KEY	Low Level
ID49	PCM0	Low Level
ID50	PCM1	Low Level
ID51	SPI0	Low Level
ID52	SPI1	Low Level
ID53	SPI2	Low Level
ID54	SPI3	Low Level
ID55	USB3	Low Level
ID56	USBH0	Low Level
ID57	TWI0	Low Level
ID58	TWI1	Low Level
ID59	TWI2	Low Level
ID60	TWI3	Low Level
ID61	UART0	Low Level
ID62	UART1	Low Level
ID63	UART2	Low Level
ID64	UART3	Low Level
ID65	UART4	Low Level
ID66	UART5	Low Level
ID67	UART6	Low Level
ID68	GPIOA	Low Level
ID69	GPIOB	Low Level
ID70	GPIOC	Low Level
ID71	GPIOD	Low Level
ID72	GPIOE	Low Level
ID73	NAND	Low Level
ID74	SD0/MMC	Low Level
ID75	SD1	Low Level
ID76	SD2	Low Level
ID77	LCD	Low Level
ID78	HDMI	Low Level
ID79	Reserved	Low Level
ID80	AUDIO_INOUT	Low Level
ID81	VCE	Low Level
ID82	VDE	Low Level
ID83	DSI	Low Level
ID84	CSI	Low Level
ID85	HDCP2.0Tx	Low Level
ID86	Reserved	-
ID87	L2	Low Level
ID88	TSIF	Low Level
ID89	DMA0	Low Level
ID90	DMA1	Low Level
ID91	DMA2	Low Level
ID92	DMA3	Low Level
ID93	USBH1	Low Level

8.1.41 Lockable Shared Peripheral Interrupts (LSPI)

There are 31 LSPIs. You can configure and then lock these interrupts against further change using CFGSDISABLE. The LSPIs map onto the interrupt IDs used for the first 31 SPIs(ID32-ID61) and are present only if the SPIs are present.

8 DCU (DDR SDRAM Control Unit)

8.2 Overview

There are two DRAM controllers use the same architecture, the two DCUs and the off-chip DDR3/ DDR3L/ LPDDR2/ LPDDR3 memory constitute the main memory system of S500. Each DRAM controller has same features. Detailed features are list below:

- Supports 1.5V/1.35V JEDEC compliant with DDR3 device. Capacity ranges from 128MB to 2GB
- Supports JEDEC compliant LPDDR2 device. Capacity range from 128MB to 2GB
- Supports JEDEC compliant DDR2 device. Capacity range from 128MB to 2GB
- 2-GB SDRAM address (1GB per CS)
- Supports the highest DDR interface clock frequency up to 666MHz. This interface speed depends on the package of the IC, the PCB layout constrain, the PCB stack. So the actual speed value may vary and need system verification
- Provide rich DDR device control command to change DDR device operation mode
- Supports single or double rank addressing
- Built-in hardware monitor to improve system debug
- Built-in hardware bandwidth performance counter
- Support more than 4 command processing concurrently in one cycle

8.3 Block Diagram

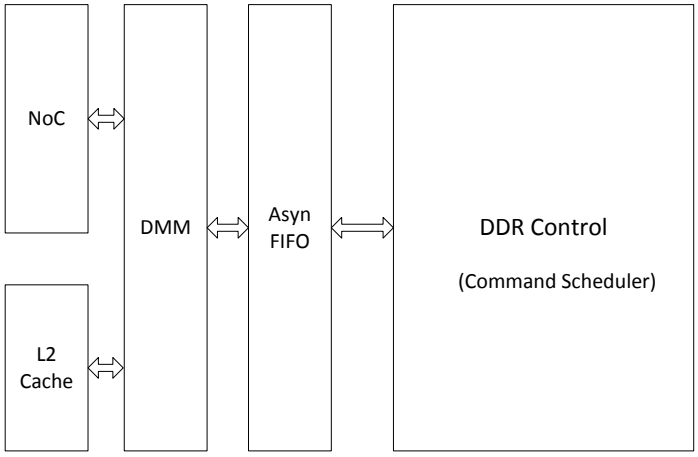


Figure 8-1 Main Memory Architecture

8.4 Function Description

Table 8-1 DDR3 device organization per cs#

Width	Capacity	Org	Piece	Bank	Bank Addr	Row addr	Col addr	Page size
32bits	1Gb	2*32M*16	2	8	BA0-BA2	A0 - A11	A0 - A9	2*2 KB
	2Gb	2*64M*16	2	8	BA0-BA2	A0 - A12	A0 - A9	2*2 KB
	4Gb	2*128M*16	2	8	BA0-BA2	A0 - A13	A0 - A9	2*2 KB
	8Gb	2*256M*16	2	8	BA0-BA2	A0 - A14	A0 - A9	2*2 KB

	2Gb	4*64M*8	4	8	BA0-BA2	A0 - A12	A0 - A9	4*1 KB
	4Gb	4*128M*8	4	8	BA0-BA2	A0 - A13	A0 - A9	4*1 KB
	8Gb	4*256M*8	4	8	BA0-BA2	A0 - A14	A0 - A9	4*1 KB
16bits	512Mb	32M*16	1	8	BA0-BA2	A0-A11	A0-A9	2KB
	1Gb	64M*16	1	8	BA0-BA2	A0-A12	A0-A9	2KB
	2Gb	128M*16	1	8	BA0-BA2	A0-A13	A0-A9	2KB
	4Gb	256M*16	1	8	BA0-BA2	A0-A14	A0-A9	2KB
	8Gb	512M*16	1	8	BA0-BA2	A0-A15	A0-A91	2KB
	1Gb	2*64M*8	2	8	BA0-BA2	A0-A12	A0-A9	2*1KB
	2Gb	2*128M*8	2	8	BA0-BA2	A0-A13	A0-A9	2*1KB
	4Gb	2*256M*8	2	8	BA0-BA2	A0-A14	A0-A9	2*1KB
	8Gb	2*512M*8	2	8	BA0-BA2	A0-A15	A0-A9	2*1KB

Table 8-2 LPDDR2 SDRAM Addressing

Items		**64 Mb**	**128 Mb**	**256 Mb**	**512 Mb**	**1Gb**		**2Gb**		**4Gb**	**8Gb**
Device Type		**S2/S4**	**S2/S4**	**S2/S4**	**S2/S4**	**S2**	**S4**	**S2**	**S4**	**S2/S4**	**S2/S4**
Number of Banks		4	4	4	4	4	8	4	8	8	8
Bank Addresses		BA0-BA1	BA0-BA1	BA0-BA1	BA0-BA1	BA0-BA1	BA0-BA2	BA0-BA1	BA0-BA2	BA0-BA2	BA0-BA2
t_{REFI}(us)		15.6	15.6	7.8	7.8	7.8	7.8	3.9	3.9	3.9	3.9
x8	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14
	Column Addresses	C0-C8	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10	C0-C10	C0-C10	C0-C11	C0-C11
x16	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14
	Column Addresses	C0-C7	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9	C0-C9	C0-C9	C0-C10	C0-C10
x32	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14
	Column Addresses	C0-C6	C0-C7	C0-C7	C0-C8	C0-C8	C0-C8	C0-C8	C0-C8	C0-C9	C0-C9

9 SRAMI (BROM and SRAM Interface Controller)

9.1 Overview

SRAMI consists of a built-in BROM (Boot ROM) block. The SRAMI controller can be accessed by CPU and DMA

- Read or write clock from AHB bus, frequency from 1MHz to 50MHz
- BROM map: 0xFFFF0000~0xFFFF7FFF (32kB)
- The beginning of the BROM (4KB) can be instead of BOOT_RAM
- NORflash map: 0xFD000000——0xFEFFFFFF (32MB)

9.2 Timing Diagram

SRAMI module contains a BROM. The CPU can boot up either from BROM. The BROM can be access by CPU or DMA.

9.3 Register List

Table 9-1 SRAMI base address

Name	Physical Base Address
SRAMI	0xB0240000

Table 9-2 SRAMI configuration Registers List

Offset	Register Name	Description
0x00	SRAMI_CTL	SRAMI control register

9.4 Register Description

9.4.1 SRAMI_CTL

SRAM IF Control Register
Offset=0x0000

Bit	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	RMEND	boot RAM remap end pending flag 0: normal . write '0' to this bit will not change it. 1: boot RAM remap end status. Write '1' to this bit will clear it.	RW	0x0
18	REMAP	BOOT_RAM Select 0: BROM; 1: BOOT_RAM	RW	0x0
17:0	-	Reserved	-	-

10 NAND Controller

10.1 Overview

The NAND Flash Interface controller is used to manage data transmission between host and Flash devices. NAND Flash is connected to host through AHB or AXI interface. Features of NAND Controller are listed below:

- 24bit/40bit/50bit/60bit/72bit Error Correction support
- multiple NAND interfaces: asynchronous; NV-DDR, NV-DDR2 (ONFI 3.0); toggle NAND 2.0
- Data error Corrected by HW automatically
- Seven bytes address support for new NAND Flash support
- SLC, MLC & TLC NAND Flash support
- 8 bit wide NAND support
- Monitor the NAND flash Ready/Busy signal by HW support

10.2 Function Description

The general purpose NAND Flash Interface controller is a State Machine configurable interface to external NAND Flash/SMC. The highly configurable and flexible interface can attach to using most of readily available NAND Flash device. The flash data bus can be configured to be 8bit access.

10.2.1 Flash State Machine

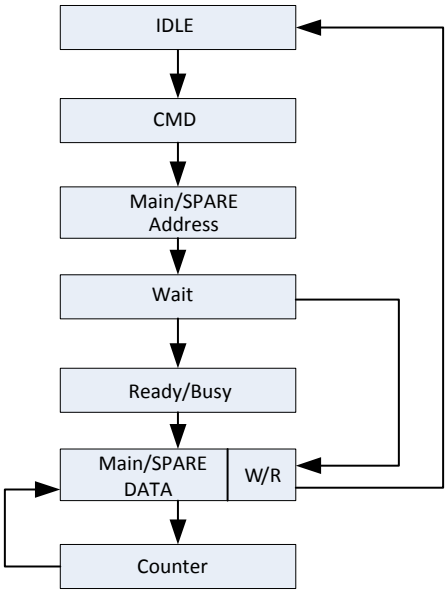


Figure 10-1 Flash Mini State Machine

10.2.2 NAND Controller Interface

The flash State machine provides automatic timing control for the using data read and write access signal line. The interface automatically maintains proper CLE, ALE and CE setup and hold up as well as proper read/write DMA practical. The Controller will transfer the data between the Int_RAM Mem and ext_Flash

Mem by AHB or DMA.
The Controller module can monitor the relatively interval transitions of the NAND flash device's Ready/Busy signal. Ir includes an interrupt that can monitor the rising edge of the busy signal and that can be set to generate a timeout interrupt if the NAND flash devices hang up, etc.
There are 3 sets of NAND Flash device interfaces in the controller: asynchronous Interface; Synchronous DDR Nand Interface, and toggle NAND Interface. It is a kind of compatible mode that Asynchronous Interface can be regarded as for most mainstream NAND devices. Synchronous DDR NAND I.F. meets the timing for ONFI 2.3 SPEC. Toggle NAND Interface can be applied for Toggle Mode DDR Data Interface.

10.2.3 BCH Encoder/Decoder

The forward error correction module is used to provide S500 applications with a reliable interface to various storage media, especially storage media that would otherwise have unacceptable bit error rates. The ECC module comprises 5 different error correcting code processors:
• 24bit BCH correcting encoder/decoder.
• 40bit BCH correcting encoder/decoder.
• 50bit BCH correcting encoder/decoder
• 60bit BCH correcting encoder/decoder.
• 72bit BCH correcting encoder/decoder.
The purpose of the BCH decoder is to process a coded block (data block followed by "parity" check data) to determine if there are errors, where they are located and how to correct them. For example, The purpose of the BCH24 encoder is to read a block of 1024 bytes from RAM, calculate and append **42** bytes parity to form a maximum 1074 bytes (1024 + 8 +42) BCH24-codeword.

11 SDC (SD/MMC Controller)

11.1 Overview

The general purpose of the SDC is to translate the host bus protocol to the SD bus protocol. Our management is based on a state machine which has 11 transfer modes to select. Every mode has a certain consequence to fellow and a certain state to be update to the registers.

- Support SD/HCSD/SDXC (SRD50 mode), miniSD, microSD, memory card, MMC/RSMMC/MMCPLUS card, INAND, MOVINAND, eMMC, SDIO card etc.
- Support 1 bit, 4bit, 8bit, bus mode.
- Clock max rate up to 100MHz.
- Contain 512-Byte SRAM*2
- Read/Write CRC Status Hardware auto checked.
- Support Auto multi Block read/write mode.
- Support SDIO function.
- Support boot mode based on MMC43. SPEC.
- Hardware timeout/delay function.
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing.
- Built-in pull up resistance for CMD/DAT lines.

11.2 Block Diagram

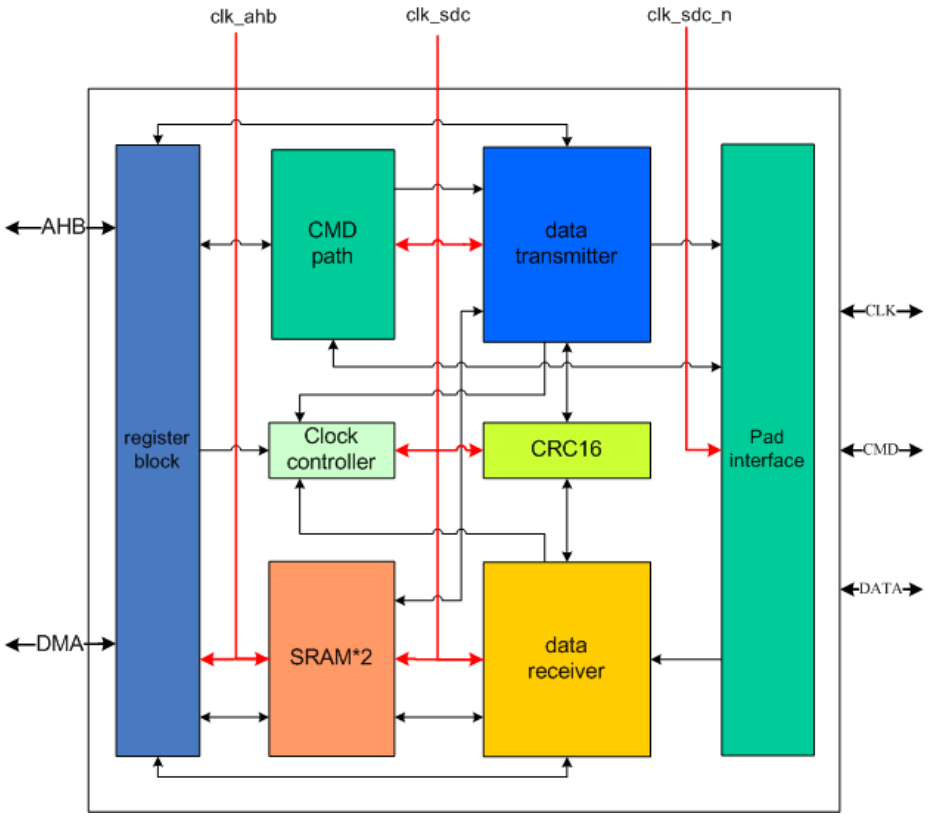


Figure 11-1 SDC block diagram

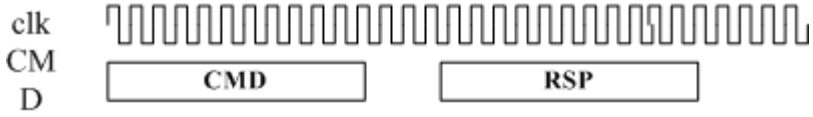
11.3 Function Description

The general purpose of the SDC is to translate the host bus protocol to the SD bus protocol. The SDC is based on a state machine which has 11 transfer modes to select. Every mode has a certain consequence to follow and a certain state to be updated to the registers. This module is managing the data transfers between RAM and SD devices. The RAM may be the SRAM or the DDR. The SD devices maybe a SD card, MMC card, eMMC flash, or a SDIO device.

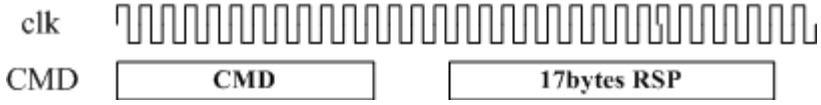
11.3.1 Transfer Mode

All SD card operation is ranged into 10 transfer modes, on which the design of SD controller is based. Use the propriety mode, can manage every SD bus operation.
The transfer modes are described as following:
Transfer only CMD(TM_mode0):

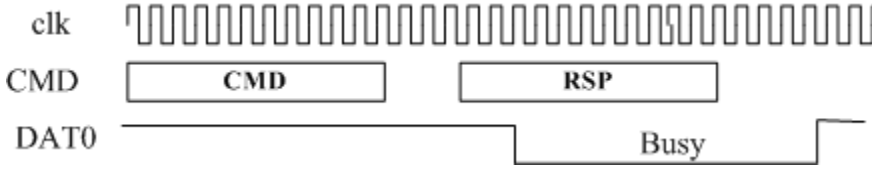
Transfer CMD and 6 byte response (TM_mode1):



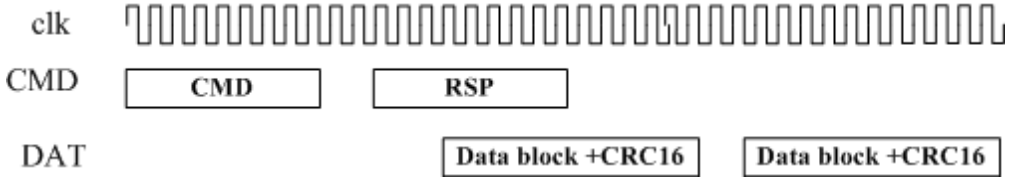
Transfer CMD and 17byte response (TM_mode2):



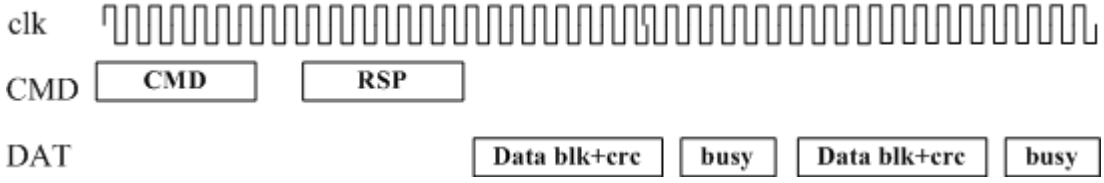
Transfer command and 6byte response with busy signal (TM_Mode3):



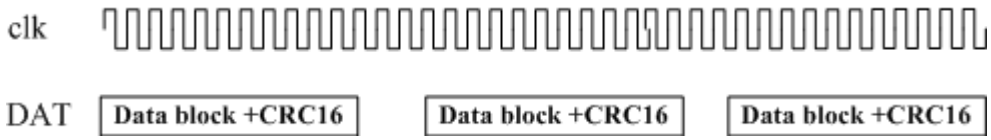
Transfer command and 6byte response and data in mode.(TM_mode4):



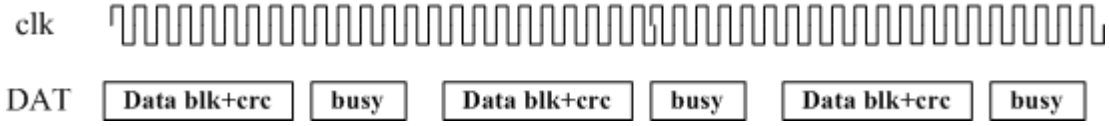
Transfer command and 6byte response and data out mode.(TM_mode5):



Transfer data in without command and response(TM_mode6):

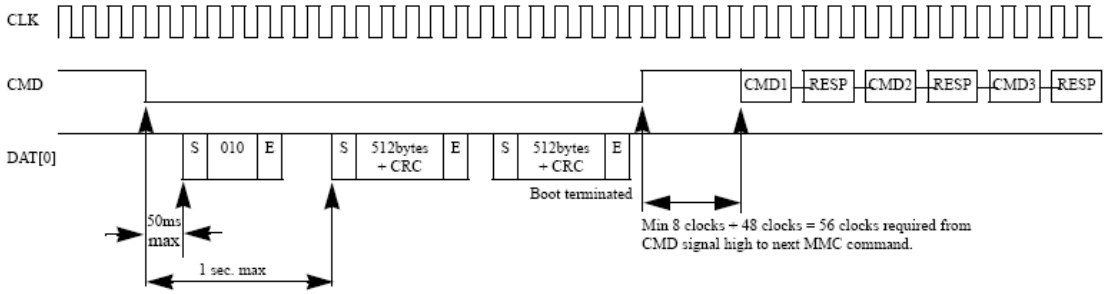


Transfer data out without command and response (TM_mode7):



Transfer only CLK.(TM_mode8):

BOOT mode Transfer data in (TM_mode9).(hardware check data crc16 ,do not check boot mode acknowledge.):



BOOT mode Transfer data in mode. (TM_mode10)(hardware check data crc16, check boot modeacknowledge).TM_mode10.the same as mode9 except the controller need to check boot acknowledge.

11.3.2 Hardware Time Out

If Transfer Watchdog timeout function Enabled (SD_CTL bit31 is set), Then Hardware Watchdog timer inside the SD host controller starts counting after Transfer Start. The value of the counter is auto cleared at the correct end of every transfer, keep counting if the Transfer not ends .when the counter's value equals to the value set in TOUTCNT(SD_CTL,bit30~24),then a timeout error will be set in SD_STATE bit 15,and The current transfer will stop at the same time.
The time out clock is described following:

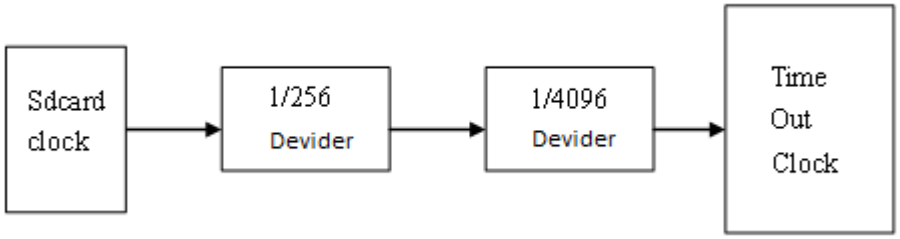


Figure 11-2 Timeout Clock Generation Diagram

Hardware Timeout was only used in data in or data out mode, or busy check in mode, such as mode3, 4, 5, 6, 7or boot mode.
If Hardware Timeout Counter equal 0, the timeout time is 128*(Timeout Clock Period), the Max Timeout time. If Hardware Timeout Counter equal 1, the timeout time is 1*(Timeout Clock Period),
The Minimum Timeout time: for Example, If SD Card Clock frequency is 10MHZ, Card Clock period is 100ns, Hardware Timeout clock frequency is 10/256/4096MHZ, Timeout clock period is100*256*4096ns = 104.8576ms. If Hardware Timeout Counter equal 0, the timeout time is 128*104.8576ms; If Hardware Timeout Counter equal 1, the timeout time is 1*104.8576ms.

Table 11-1 Hardware Timeout Time

Card Clock	Min Timeout Time	Max Timeout Time
10MHz	104.8576ms	13.4218s
20MHz	104.8576ms/2	13.4218s /2
30MHz	104.8576ms/3	13.4218s /3
40MHz	104.8576ms/4	13.4218s /4
50MHz	104.8576ms/5	13.4218s /5

11.4 Register List

Table 11-2 SDC Base Address

Name	Physical Base Address
SD0	0xB0230000
SD1	0xB0234000
SD2	0xB0238000

Table 11-3 SDx Register List

Offset	Register Name	Description
0x0000	SDx_EN	SDC card enable register
0x0004	SDx_CTL	SDC control register
0x0008	SDx_STATE	SDC STATU register
0x000C	SDx_CMD	SDC command register
0x0010	SDx_ARG	SDC argument register
0x0014	SDx_RSPBUF0	SDC RSP Buffer0 (Bit31~0)register
0x0018	SDx_RSPBUF1	SDC RSP Buffer1 (Bit63~32)register
0x001C	SDx_RSPBUF2	SDC RSP Buffer2 (Bit95~64)register
0x0020	SDx_RSPBUF3	SDC RSP Buffer3 (Bit127~96)register
0x0024	SDx_RSPBUF4	SDC RSP Buffer4 (Bit135~128)register
0x0028	SDx_DAT	SDC DATA register
0x002C	SDx_BLK_SIZE	SDC block size register
0x0030	SDx_BLK_NUM	SDC block number register
0x0034	SDx_BUF_SIZE	SDC Buffer Size Ping-pong

11.5 Register Description

11.5.1 SDx_EN

SDCx Enable Register
Offset = 0x0000

Bits	Name	Description	Access	Reset
31	RANE	Randomize enable 1: enable rand0mize 0: disable randomize	RW	0
30	-	Reserved	R	0
29:24	RAN_SEED	Randomize seed The randomize function will has a	RW	0

		initial seed as this five bits.		
23:13	-	Reserved	R	0
12	S18EN (REG_SDC18V_EN)	Pad power and pull on level SEL bit 0:Enable default 3.3V signaling; 1:Enable1.8V signaling	RW	0
11	-	Reserved	R	0
10	RESE	Build-in Pull up resistance enable. When set ,CMD,DATAS will be pull up to VCC. The number of data lines will be pulled up is equal to SD DATA BUS WIDTH. 1: Eenable 0: Disable	RW	0
9	DAT1_S	SD MMC DAT1 pad select 0: DAT1 to pad SD0_D1A 1: DAT1 to pad SD0_D1B	RW	0
8	CLK_S	SD MMC CLK pad select 0: CLK to pad SD0_CLKA 1: CLK to pad SD0_CLKB	RW	0
7	EN	SD module Enable 1: Enable 0: Disable	RW	0
6	BSEL	Bus or DMA Special Channel Selection 0: AHB Bus 1: DMA special channel	RW	0
5:4	-	Reserved	R	0
3	SDIOEN	1: SDIO function enable; 0: SDIO function disabled;	RW	0
2	DDREN	When enabled, the SDC will send and receive data use the DDR mode. the CMD line has no effect whether this bit is set or not. 1:DDR mode enabled 0:DDR mode disabled	RW	0
1:0	DATAWID	SD Interface Data Width select 00b : 1 bit 01b: 4 bit 10b: 8 bit 11b: Reserved	RW	0

11.5.2 SDx_CTL

SDC control register
Offset = 0x0004

Bits	Name	Description	Access	Reset
31	TOUTEN	Enable hardware r/w time out function. 0: Disable Hardware Timeout. 1: Enable Hardware Timeout. The timeout period is configured by Data Timeout Counter	RW	0
30-24	TOUTCNT	Hardware Time out counter value: This counter determine the timeout time of SD card data output.	RW	0

<table>
<tr><td></td><td></td><td>(used in TM_mode3~7 and boot mode)</td><td></td><td></td></tr>
<tr><td>23-20</td><td>RDELAY</td><td>Latch Input DATA delay Time select (when host controller latching data , delay the inside latching data clock to compensate signal transmission delay):
<table>
<tr><td>value</td><td>delay(ns)</td></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>0.4</td></tr>
<tr><td>0x02</td><td>0.8</td></tr>
<tr><td>0x03</td><td>1.2</td></tr>
<tr><td>0x04</td><td>1.6</td></tr>
<tr><td>0x05</td><td>2</td></tr>
<tr><td>0x06</td><td>2.4</td></tr>
<tr><td>0x07</td><td>2.8</td></tr>
<tr><td>0x08</td><td>3.2</td></tr>
<tr><td>0x09</td><td>3.6</td></tr>
<tr><td>0x0A</td><td>4.6</td></tr>
<tr><td>0x0B</td><td>5.6</td></tr>
<tr><td>0x0C</td><td>6.6</td></tr>
<tr><td>0x0D</td><td>7.6</td></tr>
<tr><td>0x0E</td><td>8.6</td></tr>
<tr><td>0x0F</td><td>13.6</td></tr>
</table></td><td>RW</td><td>0x4</td></tr>
<tr><td>19-16</td><td>WDELAY</td><td>OUT DATA delay Time select (when host controller OUT put data , delay the inside output data clock to compensate signal transmission delay):
<table>
<tr><td>value</td><td>delay(ns)</td></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>0.4</td></tr>
<tr><td>0x02</td><td>0.8</td></tr>
<tr><td>0x03</td><td>1.2</td></tr>
<tr><td>0x04</td><td>1.6</td></tr>
<tr><td>0x05</td><td>2</td></tr>
<tr><td>0x06</td><td>2.4</td></tr>
<tr><td>0x07</td><td>2.8</td></tr>
<tr><td>0x08</td><td>3.2</td></tr>
<tr><td>0x09</td><td>3.6</td></tr>
<tr><td>0x0A</td><td>4.6</td></tr>
<tr><td>0x0B</td><td>5.6</td></tr>
<tr><td>0x0C</td><td>6.6</td></tr>
<tr><td>0x0D</td><td>7.6</td></tr>
<tr><td>0x0E</td><td>8.6</td></tr>
<tr><td>0x0F</td><td>13.6</td></tr>
</table></td><td>RW</td><td>0x4</td></tr>
<tr><td>15:14</td><td>-</td><td>Reserved</td><td>R</td><td>0</td></tr>
<tr><td>13</td><td>CMDLEN</td><td>CMD LOW Enable
Enable CMD line drive low level by Software
1: Drive CMD line to low level
0: not drives CMD line to low.</td><td>RW</td><td>0</td></tr>
</table>

		NOTE: The software can set this bit to 1 to drive CMD line to low level. After power up, the card can be maintained in boot mode if the CMD line is always low level. So you can read boot data using mode 9 or mode 10.		
12	SCC	Sending continuous clock. 1: Enable 0: Disable, write 0 to this bit, stop continuance sending clock(should clear it after transfer start bit is set)	RW	0
11:8	TCN	Transfer clock number. The clock number is 16 times of this field value. ”0” means 256 clks. (used with TM_MODE8)	RW	0
7	TS	Transfer Start: 1: When write 1 by software to set this bit, SDC transfer starts according to The Transfer Mode, access mode, and other control field. It will automatically clear to 0 after transfer complete or any Err oroccurred. 0 : When write 0 by software to clear this bit. The controller needs a few CLKs to stop transfer and reset the state machine fully so the software must check the result after writing “0” to it. Note: Software can not start a new transfer until it comes to “0” actually.	RW	0
6	LBE	Data in mode the last block enable bit 0: Disable 1: Enable When set , at the end of the read last block, SDC will send more 8 clocks for the card to complete the operation.	RW	0
5	C7EN	Command CRC Check 1: Disable CRC7 checked 0: Enable CRC7 checked When set, this indicates don’t check CRC7	RW	0
4	-	Reserved	RW	0
3:0	TM	Transfer Mode[3:0] Specifies the transfer mode when transfer start bit is set 0000: Transfer command without response 0001: Transfer command with 6 bytes response (not including Data transfer) 0010: Transfer command with 17 bytes response (not including Data transfer) 0011: Transfer command with 6 bytes response, and with busy (not including Data transfer) 0100: Transfer data in mode with command and response (include crc16 checked) 0101: Transfer data out mode with command and	RW	0xF

		response (include CRC and busy checked) 0110: Transfer data in mode without command and response 0111: Transfer data out mode without command and respon (include CRC and busy checked) 1000: Transfer only clock (without any command, response, and data) 1001: BOOT mode ,Transfer data in mode with Command (hardware check data CRC16 , do not check boot mode acknowledge.) 1010: BOOT mode ,Transfer data in mode with Command (hardware check data CRC16, check boot mode acknowledge). 1011~1111: Reserved		

11.5.3 SDx_STATE

SDC STATU register
Offset = 0x0008

Bits	Name	Description	Access	Reset
31:19	-	Reserved	R	0
18	D1B_S	SD0_D1B Status: This bit reflects the level of the DAT1 Signal of SD/MMC cardB	R	1
17	SDIOB_P	SDIOB IRQ pending bit 1: One SDIOB interrupt has happened 0: No SDIOB interrupt happened. Write1 to this bit will clear it.	RW	0
16	SDIOB_EN	SDIOB IRQ enable 1: SDIOB IRQ enable (the interrupt trigger form SD0_D1B PIN) 0: SDIOA interrupt disable	RW	0
15	TOUTE	Time out error If set means a timeout error has happened. Next transfer started will clear it.	R	0
14	BAEP	Boot mode acknowledge error When in TM_MODE9, (boot mode with hardware check acknowledge), if set means a acknowledge error or timeout has happened. Next transfer started will clear it.	R	0
13	-	Reserved	R	0
12	MEMRDY	Memory ready 1: memory ready for read or write 0: memory is not ready for read and write	R	0
11	CMDS	CMD Status: This bit reflects the level of the CMD Signal of SD/MMC card	R	1
10	D1A_S	SD0_D1A Status: This bit reflects the level of the DAT1 Signal of SD/MMC cardA	R	1

9	SDIOA_P	SDIOA IRQ pending bit 1: One SDIOA interrupt has happened 0: No SDIOA interrupt happened. Write1 to this bit will clear it.	RW	0
8	SDIOA_EN	SDIOA IRQ enable 1: SDIOA IRQ enable (the interrupt trigger form SD0_D1A PIN) 0: SDIOA interrupt disable	RW	0
7	DAT0S	DAT0 Status: This bit reflects the level of the DAT0 Signal of SD/MMC card	R	1
6	TEIE	Transfer end IRQ enable: When set, enable interrupt request.	RW	0
5	TEI	Transfer end IRQ pending. Write1 to this bit will clear it.	R	0
4	CLNR	Command Line No response (only for command with response) This bit is auto cleared when Transfer Start is set.	R	0
3	CLC	Command Line transfer Complete: This bit is auto cleared when Transfer Start is set, and is set when command line transfer is complete.	R	0
2	WC16ER	CRC Write data Error: When set, this indicated a CRC write error detected over the data line. This bit is auto cleared when Transfer Start is set.	R	0
1	RC16ER	CRC Read data Error: When set, this indicated a CRC16 error detected over the received data. This bit is auto cleared when Transfer Start is set.	R	0
0	CRC7ER	CRC command response Error: When set, this indicated CRC7 error detected over the response. This bit is auto cleared when Transfer Start is set.	R	0

11.5.4 SDx_CMD

SDC send command register
Offset = 0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved		0
7:0	CMD	Command register. Fixed the bit7 is '0' The bit6 is '1'	RW	0b01xxxxxx

11.5.5 SDx_ARG

SD MMC 0 argument register
Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	ARG	Be written before SD_CMD	RW	0

11.5.6 SDx_RSPBUF0

SDC RSP Buffer0 (Bit[31:0])register
Offset = 0x0014

Bits	Name	Description	Access	Reset
31:0	RSP0	Bit[31:0]	R	0

11.5.7 SDx_RSPBUF1

SDC RSP Buffer1 (Bit63~32)register
Offset = 0x0018

Bits	Name	Description	Access	Reset
31:0	RSP1	Bit[63:32]	R	0

11.5.8 SDx_RSPBUF2

SDC RSP Buffer2 (Bit[95:64])register
Offset = 0x001C

Bits	Name	Description	Access	Reset
31:0	RSP2	Bit[95:64]	R	0

11.5.9 SDx_RSPBUF3

SDC RSP Buffer3 (Bit[127:96])register
Offset = 0x0020

Bits	Name	Description	Access	Reset
31:0	RSP3	Bit[127:96]	R	0

11.5.10 SDx_RSPBUF4

SDC RSP Buffer4 (Bit[135:128])register
Offset = 0x0024

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:0	RSP4	Bit[135:128]	R	0

11.5.11 SDx_DAT

SDC DATA register
Offset = 0x0028

Bits	Name	Description	Access	Reset
31:0	DATA	Data register	R	x

11.5.12 SDx_BLK_SIZE

SDC Block size
Offset = 0x002C

Bits	Name	Description	Access	Reset

31:11	-	Reserved	-	-
9:0	BS	Block Size[9:0]. This field determines a block size, that is how many bytes found a block. In SDR50 mode, only 512bytes/block can be set.	RW	0

11.5.13 SDx_BLK_NUM

SDC Block number
Offset = 0x0030

Bits	Name	Description	Access	Reset
31:14	-	Reserved	R	0
13:0	BN	This field determines block number in one read or write operations. Default value is 1. “0” means no block will be transferred.	RW	1

11.5.14 SDx_BUF_SIZE

SDC BUFFER SIZER PER PING-PONG
Offset = 0x0034

Bits	Name	Description	Access	Reset
31:10	-	Reserved	R	0
9:0	BUFS	This field determines BUFFER SIZE in one PING-PONG read or write operations. Default value is 0X200. “0” means no block will be transferred.	RW	0x200

11.6 Application Note

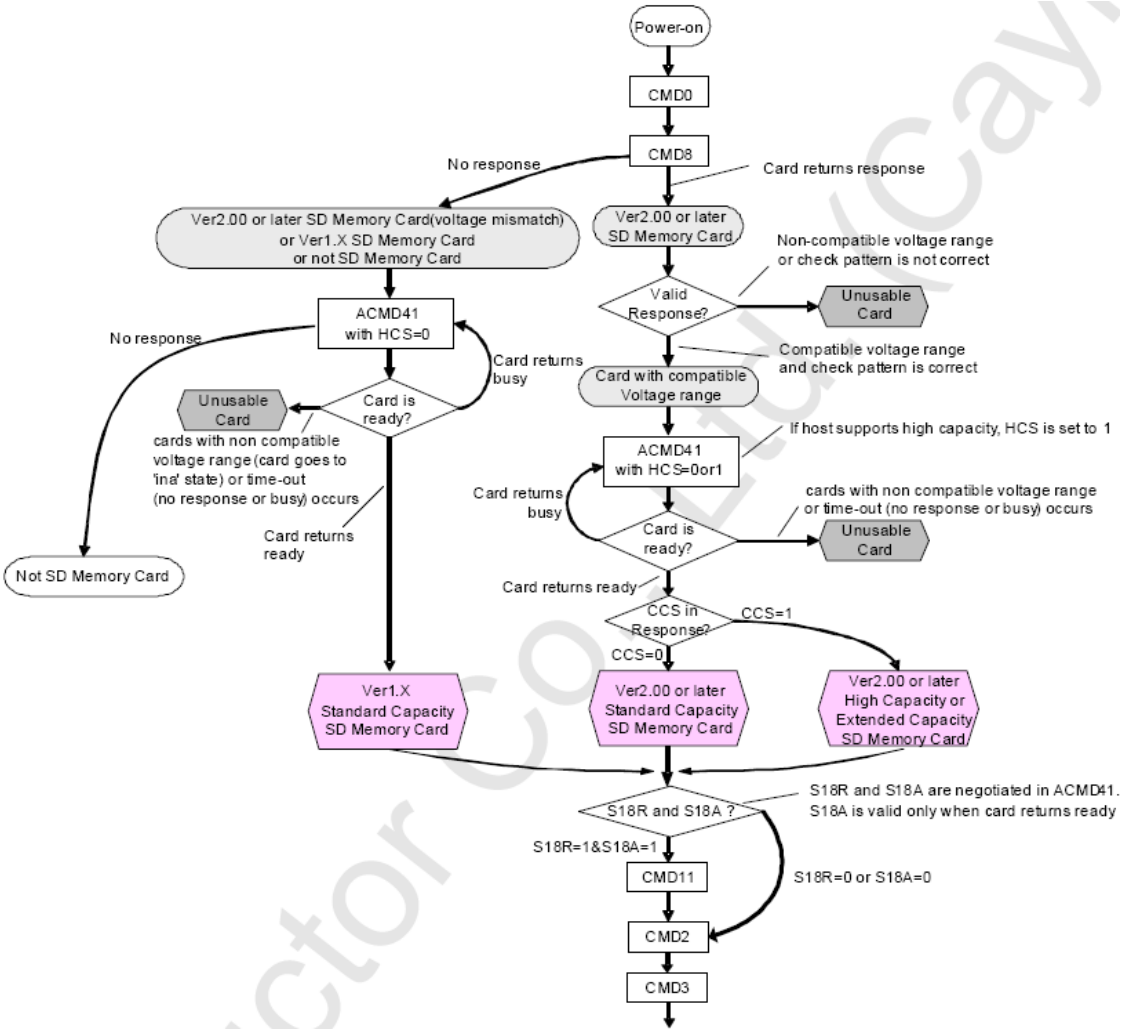


Figure 11-3 Card Initialization and Identification Flow(SD mode)

SD Card Initialization and Idification progress is shown in the figure above:

a) SD module CMU, MFP and etc. initialization
b) Setting low speed clok Fod;
c) Recogniztion card type: by sending CMD8 and CMD1 commands and receiving response:
   i. Both CMD8 and CMD1 no response: no card inserted;
   ii. CMD8 no response, CMD1 response: MMC inserted, then CMD9 can be sent to confirm whether this card support MMC4.0;
   iii. Only CMD8 response: SD card inserted, then by sending ACMD41 can confirm if the SD Card support the high speed SD 3.0;
d) If this card support 1.8V IO, then the IO working voltage should be switched by setting CMD11, SDx_EN and SDx_CTL;
e) When the CMD2, CMD3, and RCA is allocated, switch to data transfer mode;

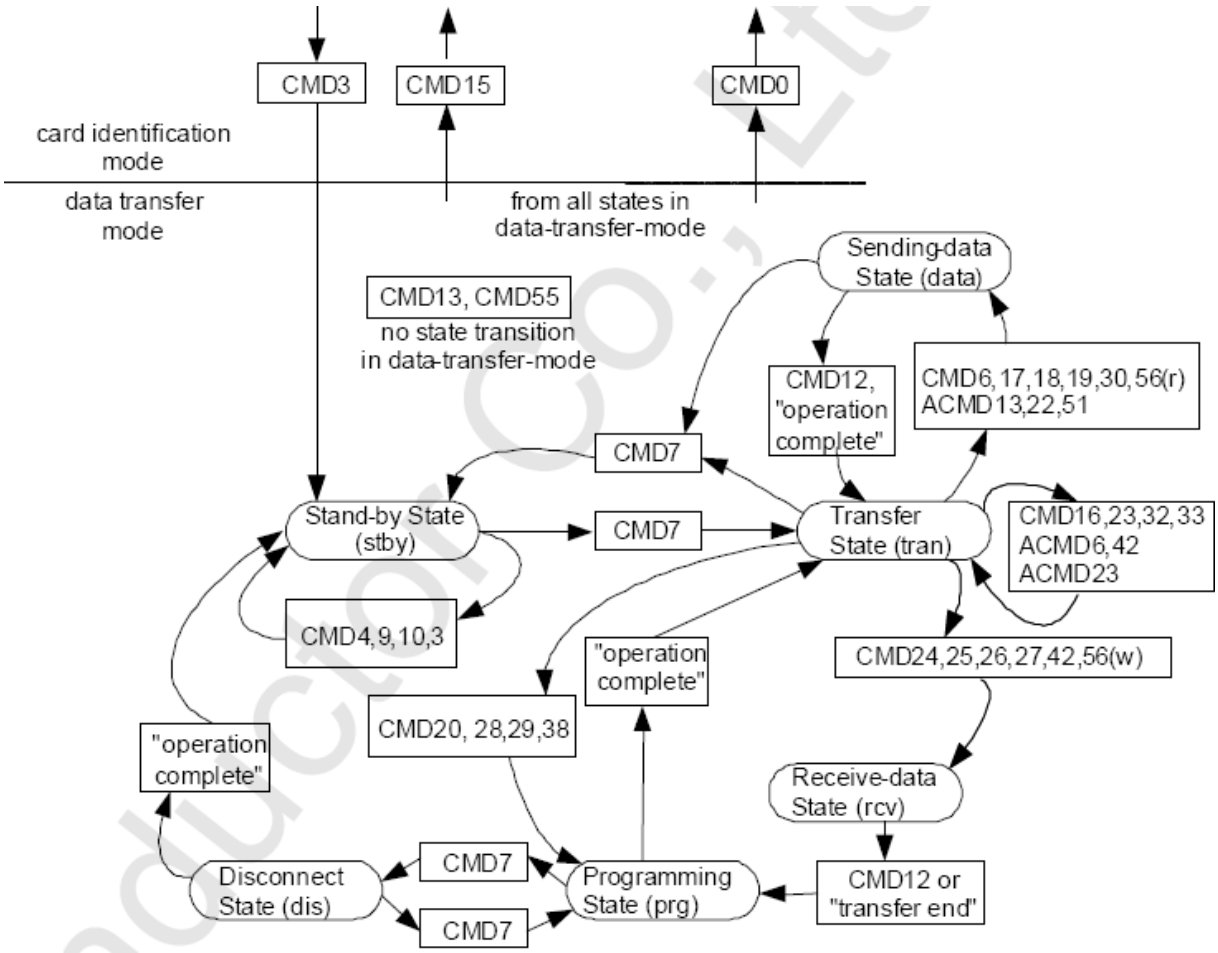


Figure 11-4 SD Memory Card Data Transfer mode State Flow

Data transfer mode working flow is shown in the figure above, and the process canbe described as:

a) CMD7 select the card;
b) Switching the working frequency to high speed data transfer mode clock: Fpp;
c) ACMD6 setting the bus width;
d) If 1.8V IO is supported, then the working mode should be switched by CMD6;
e) SDx_CTL should be configured before reading/writing operations, and setting the appropriate DelayChain;
f) Using CMD24, CMD25 for writing operations, CMD12 can stop writing process at any point;
g) Using CMD17, CMD18 for reading operations, by using CMD12 will stop the writing at any point;
h) When the operation is done, enter Standby mode, and wait for the next command.

12 GPU

12.1 Overview

PowerVR SGX544MP is one of Imagination's PowerVR Series5XT family of 3D/2D graphics engine, it can be implemented as high-performance 4-pipe single core, or in multiprocessor (MP) configurations of between 2 and 16 cores (8 to 64 pipes),features of SGX544MP is listed below.

- Industry standard supported
  - OpenGL-ES 1.1
  - OpenGL-ES 2.0
  - OpenVG 1.0.1
- Texture support
  - Cube Map
  - Projected Textures
  - Non square Textures
  - Volume Textures
  - Texture Arrays
- Texture Formats
  - RGBA 8888, 565, 1555, 1565
  - Mono chromatic 8, 16, 16f, 32f, 32int
  - Dual channel, 8:8, 16:16, 16f:16f
  - Compressed Textures PVR-TC1, PVR-TC2, ETC1
  - Programmable support for all YUV formats
- Resolution Support
  - Frame buffer max size = 4096*4096
  - Texture max size = 4096*4096
  - Max volume extent = 2048
  - Max texture repeat = 8192

12.2 Block Diagram

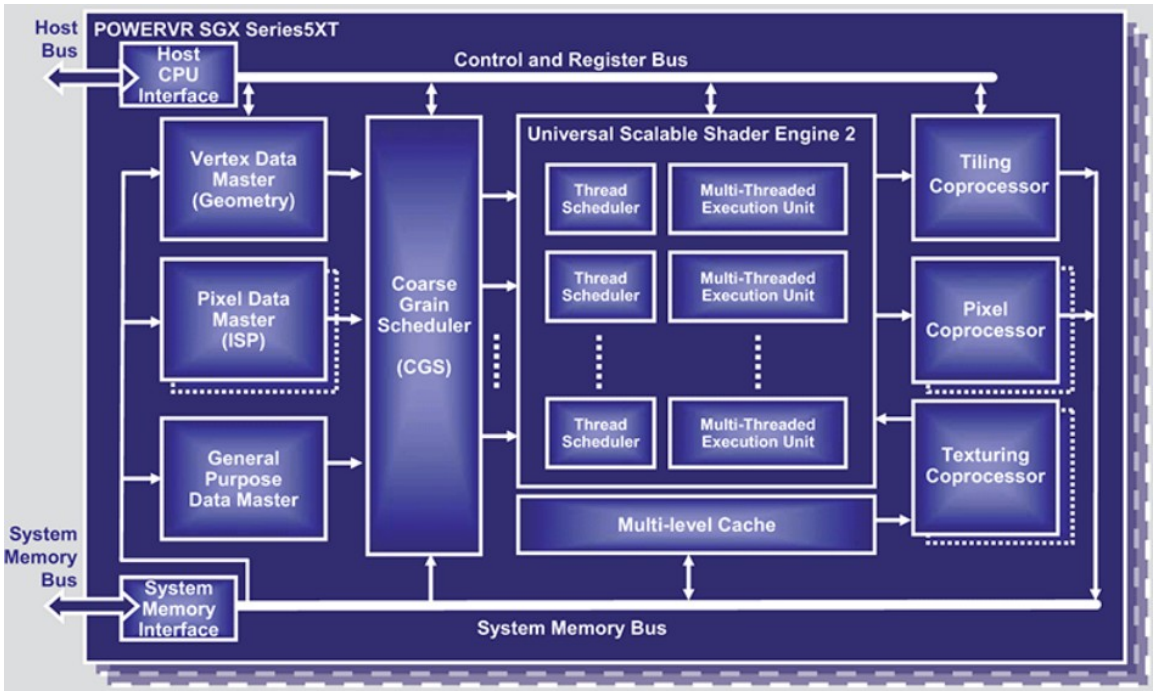


Figure 12-1 PowerVR SGX544MP GPU Block Diagram

The SGX544 core provides two interfaces and is connect with AMBA AXI bus for System memory access and Host CPU configuration.

12.3 Function Description

Detailed please refer to PowerVR website.

12.4 Register List

Detailed please refer to PowerVR website.

12.5 Register Description

Detailed please refer to PowerVR website.

12.6 Application Note

Detailed please refer to PowerVR website.

13 SI (CMOS Sensor Interface)

13.1 Overview

The CMOS Sensor Interface is for camera interface, it receives data from camera sensor and transfers the data to system memory for further processing. Features of SI is listed below:

- Windowing function
- 8-bit data parallel with Hsync, Vsync, Pclk
- MIPI CSI interface
- YUV input sequence selection and storing format selection
- Max support 5M pixel input

13.2 Block Diagram

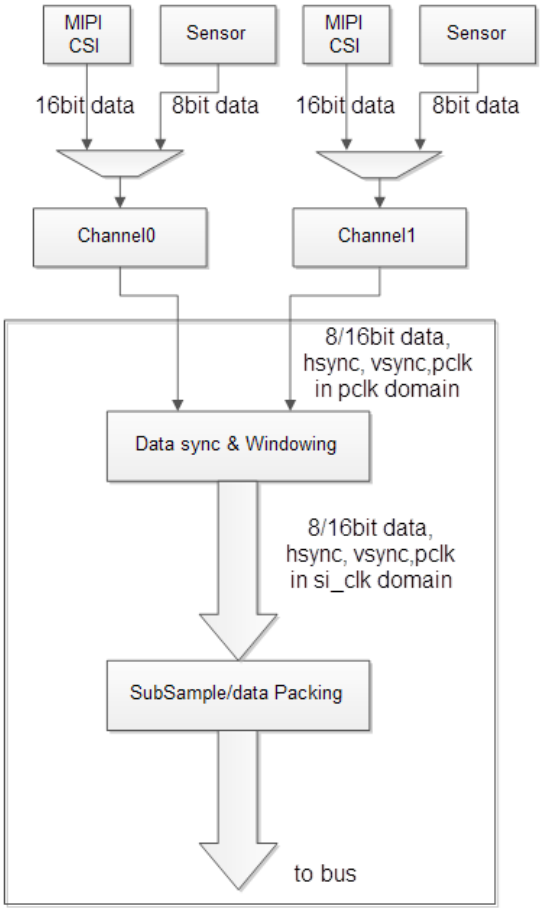


Figure 13-1 Video Generating Diagram

13.3 Function Description

13.3.1 Data Synchronization

SI takes the Sensor VSYNC as the start signal of one frame processing, when one frame is over, the final statistic data will be written into DDR memory and a set of FLAGs will be genenrated for reset.

13.3.2 Windowing

The windowing function can clip the sensor image into sub-region. Both width and height of sub-region can be defined via setting the starting position and ending poison of the X and Y coordinate.
The unit of the size of the window is pixel. So for the YUYV input, need to clip 2 byte of the stream. Input sequence
The SI support YUYV pattern sensor interface

13.3.3 Storing format

The SI support YUYV pattern sensor interface, and the data will be stored in the following formats.

YUV semi-planar:
Y format

Y3	Y2	Y1	Y0

31bit 0bit

UV format

V1	U1	V0	U0

31bit 0bit

YUV planar:
Y format

Y3	Y2	Y1	Y0

31bit 0bit

U format

U3	U2	U1	U0

31bit 0bit

V format

V3	V2	V1	V0

31bit 0bit

13.4 Register List

Table 13-1 SI register Base Address

Name	Physical Base Address
SI	0xB0270000

Table 13-2 SI Configuration Registers List

Offset	Register Name	Description
0x00	SI_ENABLE	Enable and Preline setting

0x04	SI_INT_STAT	Interrupt control and pending
0x08	SI_CH0_CTRL	Ch0 Sensor input signal polarity and input/output format
0x0C	SI_CH0_ROW_RANGE	Ch0 Window height
0x10	SI_CH0_COL_RANGE	Ch0 Window width
0x14	SI_CH0_ADDRY	Ch0 SI Y output address
0x18	SI_CH0_ADDRU	Ch0 SI U/UV output address
0x1C	SI_CH0_ADDRV	Ch0 SI V output address
0x20	SI_CH1_CTRL	Ch1 Sensor input signal polarity and input/output format
0x24	SI_CH1_ROW_RANGE	Ch1 Window height
0x28	SI_CH1_COL_RANGE	Ch1 Window width
0x2C	SI_CH1_ADDRY	Ch1 SI Y output address
0x30	SI_CH1_ADDRU	Ch1 SI U/UV output address
0x34	SI_CH1_ADDRV	Ch1 SI V output address

Note:Some or all the register bits of the Registers except SI_ENABLE need to be double-buffered

13.5 Register Description

13.5.1 SI_ENABLE

Enable and Preline setting
Offset = 0x00

Bits	Name	Description	Access	Reset
31	CH1 ENABLE	Enable CH1	RW	0
30:28	-	Reserved	-	-
27:16	CH1 PRELINE	CH1 Predefine line number	RW	0
15	CH0 ENABLE	Enable CH0	RW	0
14:12	-	Reserved	-	-
11:0	CH0 PRELINE	CH0 Predefine line number	RW	0

13.5.2 SI_INT_STAT

Interrupt control and pending
Offset = 0x04

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15	CH1_IN_OVERFLOW_PEND	Ch1 Sensor input overflow interrupt pending 0:no pending 1:pending	RW	0
14	CH1_OUT_OVERFLOW_PEND	Ch0 SI output overflow interrupt pending 0:no pending 1:pending	RW	0
13	CH1_PRELINE_PEND	Ch1 Preline interrupt pending 0:no pending 1:pending *Note:write 1 to clear*	RW	0
12	CH1_FRAME_PEND	Ch1 Frame end interrupt pending 0:no pending 1:pending	RW	0

		Note:write 1 to clear		
11	CH0_IN_OVERFLOW_PEND	Ch1 Sensor input overflow interrupt pending 0:no pending 1:pending	RW	0
10	CH0_OUT_OVERFLOW_PEND	Ch0 SI output overflow interrupt pending 0:no pending 1:pending	RW	0
9	CH0_PRELINE_PEND	Ch0 Preline interrupt pending 0:no pending 1:pending *Note:write 1 to clear*	RW	0
8	CH0_FRAME_PEND	Ch0 Frame end interrupt pending 0:no pending 1:pending *Note:write 1 to clear*	RW	0
7:4	-	Reserved	-	-
3	CH1_PRELINE_IRQ_EN	Ch1 Preline interrupt enable	RW	0
2	CH1_FRAME_EN_IRQ_EN	Ch1 Frame end interrupt enable	RW	0
1	CH0_PRELINE_IRQ_EN	Ch0 Preline interrupt enable	RW	0
0	CH0_FRAME_EN_IRQ_EN	Ch0 Frame end interrupt enable	RW	0

13.5.3 SI_CH0_CTRL

CH0 input signal polarity and input/output format
Offset = 0x08

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	SYNC_POL_HSYNC	Hsync Polarity 0:data active during Hsync low, 1:data active during Hsync high	RW	0
12	SYNC_POL_VSYNC	Vsync Polarity 0:data active during Vsync low, 1:data active during Vsync high	RW	0
11	-	Reserved	-	-
10	SEMI_UV_INV	0:NO reverse 1:UV reverse (only in semi mode)	RW	0
9:8	YUV_OUTPUT_FORMAT	Output YUV format 0:YUV 4:2:2 planar 1:YUV 4:2:0 planar, 2:YUV 4:2:2 semi-planar 3:YUV 4:2:0 semi-planar	RW	0
7:6	-	Reserved	-	-
5:4	YUV_INPUT_FORMAT	Input YUV format(first->next) 0:U0Y0V0Y1 1:V0Y0U0Y1 2:Y0U0Y1V0 3:Y0V0Y1U0	RW	0
3	SRC_INTF	0:Sensor 1:CSI	RW	0
2:0	IN_FMT	011:YUV	RW	0

		Other:Reserved		

13.5.4 SI_CH0_ROW_RANGE

Window size - height
Offset = 0x0C

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	ROW_END	Active Window Ending Line Number	RW	0
15:12	-	Reserved	-	-
11:0	ROW_START	Window Starting Line Number [11:0]	RW	0

13.5.5 SI_CH0_COL_RANGE

Window size - width
Offset = 0x10

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:16	COL_END	Active Window Ending column Number	RW	0
15:13	-	Reserved	-	-
12:0	COL_START	Window Starting column Number	RW	0

13.5.6 SI_CH0_ADDRY

SI output data addressY
Offset = 0x14

Bits	Name	Description	Access	Reset
31:0	OUT_ADDRY	SI output Y address(word aligned)	RW	0

13.5.7 SI_CH0_ADDRU

SI output data addressU
Offset = 0x18

Bits	Name	Description	Access	Reset
31:0	OUT_ADDRU	SI output U/UV address(word aligned)	RW	0

13.5.8 SI_CH0_ADDRV

SI output data addressV
Offset = 0x1C

Bits	Name	Description	Access	Reset
31:0	Out_addrV	SI output V address(word aligned)	RW	0

13.5.9 SI_CH1_CTRL

CH1 input signal polarity and input/output format
Offset = 0x20

Bits	Name	Description	Access	Reset

31:14	-	Reserved	-	-
13	SYNC_POL_HSYNC	Hsync Polarity 0:data active during Hsync low, 1:data active during Hsync high	RW	0
12	SYNC_POL_VSYNC	Vsync Polarity 0:data active during Vsync low, 1:data active during Vsync high	RW	0
11	-	Reserved	-	-
10	SEMI_UV_INV	0:NO reverse 1:UV reverse (only in semi mode)	RW	0
9:8	YUV_OUTPUT_FORMAT	Output YUV format 0:YUV 4:2:2 planar 1:YUV 4:2:0 planar, 2:YUV 4:2:2 semi-planar 3:YUV 4:2:0 semi-planar	RW	0
7:6	-	Reserved	-	-
5:4	YUV_INPUT_FORMAT	Input YUV format(first->next) 0:U0Y0V0Y1 1:V0Y0U0Y1 2:Y0U0Y1V0 3:Y0V0Y1U0	RW	0
3	SRC_INTF	0:Sensor 1:CSI	RW	0
2:0	IN_FMT	011:YUV Other:Reserved	RW	0

13.5.10 SI_CH1_ROW_RANGE

Window size - height
Offset = 0x24

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	ROW_END	Active Window Ending Line Number	RW	0
15:12	-	Reserved	-	-
11:0	ROW_START	Window Starting Line Number [11:0]	RW	0

13.5.11 SI_CH1_COL_RANGE

Window size - width
Offset = 0x28

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:16	COL_END	Active Window Ending column Number	RW	0
15:13	-	Reserved	-	-
12:0	COL_START	Window Starting column Number	RW	0

13.5.12 SI_CH1_ADDRY

SI output data addressY
Offset = 0x2C

Bits	Name	Description	Access	Reset
31:0	OUT_ADDRY	SI output Y address(word aligned)	RW	0

13.5.13 SI_CH1_ADDRU

SI output data addressU
Offset = 0x30

Bits	Name	Description	Access	Reset
31:0	OUT_ADDRU	SI output U/UV address(word aligned)	RW	0

13.5.14 SI_CH1_ADDRV

SI output data addressV
Offset = 0x34

Bits	Name	Description	Access	Access
31:0	OUT_ADDRV	SI output V address(word aligned)	RW	0

13.6 Application Note

14 MIPI CSI2

14.1 Overview

The Mobile Industry Processor Interface (MIPI) Alliance defines Camera Serial Interface-2 (CSI2) between a peripheral device (camera) and a host processor (AP). Features of MIPI CSI2 are listed below:

- Compliant with MIPI CSI-2 Specification version 1.0 and the D-PHY specification version 0.9
- High-Speed Mode:80 Mbps to 1 Gbps synchronous
- Low-Power Mode: spaced one-hot encoding for data
- Ultra low power support
- Support Data Type:YUV422-8bit
- 1-4 Data Lanes Configurable
- Support NTSC and PAL format for CVBS output
- Four 12-bit video DAC outputs sample rate up to 300MHz
- Support Standard 8bit BT.656 Output for 625-line and 525-line

14.2 Function Description

The MIPI CSI-2 Receiver only receives data. Normally, it receives data in High-Speed mode in form of packet, then it unpack the packet and push the data into FIFO. It supports several data format of input data stream, including YUV422 8-bit, Generic 8-bit Long Packet Data Types, User Define Byte-based Data. Detailed about MIPI CSI2, please refer to the document *< MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2)>.*

14.3 Register List

Table 14-1 CSI-2 Receiver Registers Address

Name	Physical Base Address
CSI	0xB02D0000

Table 14-2 CSI-2 Receiver Registers

Offset	Register Name	Description
0x00	CSI_CTRL	CSI-2 Receiver Control Register
0x04	SHORT_PACKET	Short Packet Register
0x08	ERROR_PENDING	Error Pending Register
0x0C	STATUS_PENDING	Status Pending Register
0x10	LANE_STATUS	Lane Status Register
0x14	CSI_PHY_T0	CSI PHY Timing0 Register
0x18	CSI_PHY_T1	CSI PHY Timing1 Register
0x1C	CSI_PHY_T2	CSI PHY Timing2 Register
0x20	CSI_ANALOG_PHY	CSI analog PHY config Register
0x100	CONTEXT0_CFG	Context Configuration Register
0x104	CONTEXT0_STATUS	Context Status Register
0x120	CONTEXT1_CFG	Context Configuration Register
0x124	CONTEXT1_STATUS	Context Status Register

Each Context is configured independently with a register block as follows:

Table 14-3 Data Lane configuration register block base address

Data Lane	REGS BLOCK Base Address Offset
Context0	0x100
Context1	0x120

Table 14-4 Context config register

Offset	Register Name	Description
0x00	CONTEXTx_CFG	Context Configuration Register
0x04	CONTEXTx_STATUS	Context Status Register

14.4 Register Description

14.4.1 CSI_CTRL

This register is mainly used to configure the CSI-2 Receiver to fit the application.

CSI_CTRL Offset=0x00

Bits	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	HSCLK_EDGE	HSCLK Sample Edge 0:Rising Edge 1:Falling Edge	RW	0
09	PHY_INIT_SEL	0:check the init LP11 sequence 1:don't check init LP11 sequence	RW	0
08	CLK_LANE_HS	Force receiving hs clock omitting hs entry sequence: 0:Disable 1:Enable	RW	0
07	CCE	CRC Check Enable 0:Disable 1:Enable	RW	0
06	ECE	ECC Check Enable 0:Disable 1:Enable	RW	0
05:04	LANE_NUM	Data Lane Number 00:Data Lane 0 (1 Data Lane) 01:Data Lane 0 ~ 1 (2 Data Lanes) 10:Data Lane 0 ~ 2 (3 Data Lanes) 11:Data Lane 0 ~ 3 (4 Data Lanes)	RW	0
03	PHY_CALEN	Init the D-PHY calibration 0:do not operate 1:Init the D-PHY calibration *Note:After D-PHY is calibration done, this bit will be changed to '0' .*	RW	0
02	D_PHY_EN	D-PHY Block Enable 0:Disable (D-PHY is powered off) 1:Enable (D-PHY is powered on)	RW	0
01	-	Reserved	-	-
00	EN	CSI-2 Receiver ENABLE Enable logical operation of CSI-2 Receiver	RW	0

		1:Enable 0:Disable *Note:When CSI-2 Receiver is enable, Data Lane and Clock Lane are both enable, and Data Lane is forced into Receive mode and wait for Stop State.* *When CSI-2 Receiver is disabled, the state of digital logic goes to initial state.*		

14.4.2 SHORT_PACKET

This register is mainly used to store the short packet information from Image Sensor.
SHORT_PACKET Offset=0x04

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:00	SHORT_PACKET	Short Packet Information (Not include ECC)	R	0

14.4.3 ERROR_PENDING

This register reflects the error pending bit of CSI-2 Receiver .
ERROR_PENDING Offset=0x08

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29	OVF	FIFO Overflow 0:no Fifo Overflow Error 1:Fifo Overflow Error Write 1 to clear the bit	RW	0
28	ERR_CONTROL_CLK	False Control Error of Clock Lane 0:no error occurred 1:an incorrect line state sequence is detected. Write 1 to clear the bit	RW	0
27:24	ERR_SOTSYNCHS_D	Start-of-Transmission (SoT) Error 0:no error occurred 1:An incorrect synchronization sequence is detected (more than 1 bit error). Write 1 to clear the bit	RW	0
23:20	ERR_CONTROL_D	False Control Error 0:no error occurred 1:an incorrect line state sequence is detected. For example, if a BTA request or escape mode request is immediately followed by a Stop state instead of the required Bridge state. Write 1 to clear the bit	RW	0
19:16	ERR_ESC_D	Escape Entry Error Pending Bit 0:no error occurred 1:an unrecognized escape entry command is received. Write 1 to clear the bit	RW	0
15:14	-	Reserved	-	-
13	ERR_CRC	Receive CRC Error Bit 0:no error occurred 1:a CRC Error occurred when receiving long	RW	0

		packet Write 1 to clear the bit		
12	ERR_ECC	Receive ECC Error Bit 0:no error occurred or a single-bit error occurs and corrected 1:multi-bit errors occur Write 1 to clear the bit	RW	0
11:08	ERR_ID_VC	An error Identification on Virtual Channel 0~3 is received 0:no error occurred 1:an unrecognized or unimplemented data ID is received. Write 1 to clear the bit	RW	0
07:04	EFS_VC	Error of Frame Sync Packet on Virtual Channel 0~3 0:No error occurred 1:Error occurred Write 1 to clear the bit	RW	0
03:00	ELS_VC	Error of Line Sync Packet on Virtual Channel 0~3 0:No error occurred 1:Error occurred Write 1 to clear the bit	RW	0

14.4.4 STATUS_PENDING

This register reflects the status pending bit of CSI-2 Receiver .
STATUS_PENDING
Offset=0x0C

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	SOFT_ERROR	Soft Error Pending Bit 0:No error occurred 1:Error occurred Write 1 to clear the bit	RW	0
21	HARD_ERROR	Hard Error Pending Bit 0:No error occurred 1:Error occurred Write 1 to clear the bit	RW	0
20	SP_RX_DONE	Short Packet received done 0:no short packet is received 1:a short packet is received Write 1 to clear the bit	RW	0
19:18	-	Reserved	-	-
17	CONTEXT1	Context 1 Event Complete bit 0:Context 1 Event doesn't complete 1:Context 1 Event completes *Note:The corresponding FE of the context is received indicates that event completes.* *Write 1 to clear the bit*		
16	CONTEXT0	Context 0 Event Complete bit 0:Context 0 Event doesn't complete 1:Context 0 Event completes	RW	0

		Note:The corresponding FE of the context is received indicates that event completes. *Write 1 to clear the bit*		
15:06	-	Reserved	-	-
05	HARD_ERROR_EN	Hard Error Interrupt Enable 0:Disable 1:Enable	RW	0
04	SP_RX_DONE_EN	Short Packet received done Interrupt Enable 0:Disable 1:Enable	RW	0
03:02	-	Reserved	-	-
1	CONTEXT1_EN	Context 1 Event Complete Interrupt Enable 0:Disable 1:Enable	RW	0
0	CONTEXT0_EN	Context 0 Event Complete Interrupt Enable 0:Disable 1:Enable	RW	0

14.4.5 LANE_STATUS

This register specifies the Lane Status of the CSI-2 Receiver

LANE_STATUS Offset=0x10

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
09:06	DULP	Data Lane is in Ultra-Low Power State 0:Data Lane is not in Ultra-Low Power State 1:Data Lane is in Ultra-Low Power State *Note:Bit 9 for Data Lane 3, Bit 8 for Data Lane 2, Bit 7 for Data Lane 1, Bit 6 for Data Lane 0*	R	0
05:02	DST	Data Lane is in RX Stop-State 0:Data Lane is not in RX Stop State 1:Data Lane is in RX Stop State *Note:Bit 5 for Data Lane 3, Bit 4 for Data Lane 2, Bit 3 for Data Lane 1, Bit 2 for Data Lane 0*	R	0
01	CULP	Clock Lane is in Ultra-Low Power State 0:Lane is not in Ultra-Low Power State 1:Lane is in Ultra-Low Power State	R	0
00	CST	Clock Lane is in RX Stop State 0:Lane is not in RX Stop State 1:Lane is in RX Stop State	R	0

14.4.6 CSI_PHY_T0

CSI D-PHY Operation Timing0 Register – For Clock Lane/Data Lane initial time.

CSI_PHY_T0 Offset=0x14

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:00	$T_{INITIAL}$	Initial Time for Clock Lane/Data Lane. $T = 16 * (T_{INITIAL} + 1) * T_{CSI2\_Clk}$ *Note:The timing parameter in multiples of CSI2_Clk period.*	RW	0x1FF

14.4.7 CSI_PHY_T1

CSI D-PHY Operation Timing1 Register – For Clock Lane
CSI_PHY_T1 Offset=0x18

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:04	T_{CLK_SETTLE}	Settle Time for Clock Lane. $T = (T_{CLK\_SETTLE} + 1) * T_{CSI2\_Clk}$ *Note:The timing parameter in multiples of CSI2_Clk period.*	RW	0xF
03:00	$T_{CLK\_TERM\_EN}$	Time to enable clk Lane receiver line termination measured from when DN crossed Vilmax. $T = (T_{CLK\text{-}TERM\text{-}EN} + 1) * T_{CSI2\_Clk}$ *Note:The timing parameter in multiples of CSI2_Clk period.*	RW	0x3

14.4.8 CSI_PHY_T2

CSI D-PHY Operation Timing2 Register – For Data Lane
CSI_PHY_T2 Offset=0x1c

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:04	T_{HS_SETTLE}	Settle Time for Data Lane. $T = (T_{HS\text{-}SETTLE} + 1) * T_{CSI2\_Clk}$ *Note:The timing parameter in multiples of CSI2_Clk period.*	RW	0xF
03:00	$T_{D\_TERM\text{-}EN}$	Time to enable Data Lane receiver line termination measured from when DN crossed Vilmax. $T = (T_{D\text{-}TERM\text{-}EN} + 1) * T_{CSI2\_Clk}$ *Note:The timing parameter in multiples of CSI2_Clk period.*	RW	0x3

14.4.9 CSI_ANALOG_PHY

CSI analog-PHY Operation config
CSI_Analog_PHY Offset=0x20

Bit(s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:6	$D_{DATALANE}$	Direction of csi datalane3,2,1,0 0:obverse 1:inverse	RW	0
5	$D_{CLKLANE}$	Direction of csi clklane 0:obverse 1:inverse	RW	0
4:0	CLK_DATA_EN	Clk lane and four data lane enable signal Order is D4 D3 D2 D1 CK	RW	0

14.4.10 CSI_MAP

CSI Mapping
Offset=0x28

Bit(s)	Name	Description	Access	Reset

31:12	-	Reserved	-	-
11:9	DLane3_MAP	MIPI CSI Lane 3 Mapping: 0x0:Analog Lane0 0x1:Analog Lane1 0x2:Analog Lane2 0x3:Analog Lane3 Others:Reserved	RW	0x3
8:6	DLane2_MAP	MIPI CSI Lane 2 Mapping: 0x0:Analog Lane0 0x1:Analog Lane1 0x2:Analog Lane2 0x3:Analog Lane3 Others:Reserved	RW	0x2
5:3	DLane1_MAP	MIPI CSI Lane 1 Mapping: 0x0:Analog Lane0 0x1:Analog Lane1 0x2:Analog Lane2 0x3:Analog Lane3 Others:Reserved	RW	0x1
2:0	DLane0_MAP	MIPI CSI Lane 0 Mapping: 0x0:Analog Lane0 0x1:Analog Lane1 0x2:Analog Lane2 0x3:Analog Lane3 Others:Reserved	RW	0x0

14.4.11 CONTEXT0_CFG

This register is mainly used to configure the format of Context x.
Offset=0x100
Note:In the register description, the postfix "x" means each Context has the register

Bit(s)	Name	Description	Access	Reset
31:09	-	Reserved	-	-
08:07	VCN	Virtual Channel Number	RW	0
06:01	DT	Data Type of received Long Packet 0x10:Null 0x11:Blanking Data 0x12:Embedded 8-bit non Image Data 0x13 - 0x17:Reserved 0x18:YUV420 8-bit 0x19:YUV420 10-bit 0x1A:Legacy YUV420 8-bit 0x1B:Reserved 0x1C:YUV420 8-bit (Chroma Shifted Pixel Sampling) 0x1D:YUV420 10-bit (Chroma Shifted Pixel Sampling) 0x1E:YUV422 8-bit 0x1F:YUV422 10-bit 0x30:User Defined 8-bit Data Type 1 0x31:User Defined 8-bit Data Type 2 0x32:User Defined 8-bit Data Type 3 0x33:User Defined 8-bit Data Type 4	RW	0x1E

		Others:Reserved (CSI-2 Receiver part of these) *Note:Hardware will use the data type to detect the desired long packet.*		
00	EN	Enable the Context 0:disable 1:enable	RW	0

14.4.12 CONTEXT0_STATUS

This register is mainly used to store the status of Context x.
Offset=0x104
Note:In the register description, the postfix "x" means each Context has the register

Bit(s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:00	LINE_NUM	Current Line Number	R	0

14.4.13 CONTEXT1_CFG

This register is mainly used to configure the format of Context x.
Offset=0x120
Note:In the register description, the postfix "x" means each Context has the register

Bit(s)	Name	Description	Access	Reset
31:09	-	Reserved	-	-
08:07	VCN	Virtual Channel Number	RW	0
06:01	DT	Data Type of received Long Packet 0x10:Null 0x11:Blanking Data 0x12:Embedded 8-bit non Image Data 0x13 - 0x17:Reserved 0x18:YUV420 8-bit 0x19:YUV420 10-bit 0x1A:Legacy YUV420 8-bit 0x1B:Reserved 0x1C:YUV420 8-bit (Chroma Shifted Pixel Sampling) 0x1D:YUV420 10-bit (Chroma Shifted Pixel Sampling) 0x1E:YUV422 8-bit 0x1F:YUV422 10-bit 0x30:User Defined 8-bit Data Type 1 0x31:User Defined 8-bit Data Type 2 0x32:User Defined 8-bit Data Type 3 0x33:User Defined 8-bit Data Type 4 Others:Reserved (CSI-2 Receiver only support part of these) *Note:Hardware will use the data type to detect the desired long packet.*	RW	0x1E
00	EN	Enable the Context 0:disable 1:enable	RW	0

14.4.14 CONTEXT1_STATUS

This register is mainly used to store the status of Context x.
Offset=0x124
Note:In the register description, the postfix "x" means each Context has the register

Bit(s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:00	LINE_NUM	Current Line Number	R	0

14.5 Application Note

Please refer to the document < *MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2)*>.

15 Video Codec

15.1 Overview

Video codec consists of VDE (Video Decoder Engine) and VCE (Video Coder Engine). Features of Video Codec are listed below:

Video Decoder

- Support Real-time video decoder of most popular video formats (some are supported by the 3rd party applications), such as MPEG-4, H.264, etc.
- Error detection and concealment support for all video formats
- With 2D reference data cache to reduce DDR bandwidth
- Output data format is YUV420 semi-planar
- Average data rate 60Mbps, peak rate up to 120Mbps

Video Encoder

- Support video encoder for baseline H.264
- Input data formats:
  - YUV420SP
  - YVU420SP
  - YUV420P
  - ARGB
  - ABGR
  - ARGBA
  - BGRA
  - RGB565
  - BGR565
- Support VBR and CBR
- Max fps is up to 60fps@1920*1088, 5M pixel and 13M pixel
- Video size from 176*144 to 1920*1088
- Support upscale and downscale, from 1⁄2 to 8
- Low latency data encoder

JPEC Decoder

- Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:4 ,211H, 211V sampling formats
- Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
- JPEG Baseline Decoder size is from 48*48 to 30000*30000 (900Mpixels)
- For Progressive Decoder size is from 48*48 to 8192*8192
- Support JPEG ROI (Region of Image) decode
- Maximum data rate is up to 100 million pixels per second

JPEG Encoder

- Input data format:
  - YUV420sp
  - YVU420sp
  - YUV420P
  - ARGB
  - ABGR
  - ARGBA
  - BGRA
  - RGB565
  - BGR565

- Max data rate up to 70 million pixels per second
- Image size is from 48*48 to 8176*8176
- Support upscale and downscale, from 1⁄2 to 8

16 TSIF (Transport Stream Interface)

16.1 Overview

The TSIF is used to receive MPEG-2 data as a slave, the received data will be stored into DDR with 188 byte/unit. During the transfer, data is shifted in serial or parallel. The TS_CLK line synchronizes the shifting and sampling of the data.

Features of TSIF are listed below:

- MPEG-2 transport stream interface
- Serial and parallel I/F with synchronous mode.
- Data bus width is 1 bit on serial I/F and 8 bits on parallel I/F.
- Input buffer 256 byte (64 bit × 32 word).
- Input data is stored into DDR in 32-bit little-endian mode only with 188 byte/unit.

16.2 Block Diagram

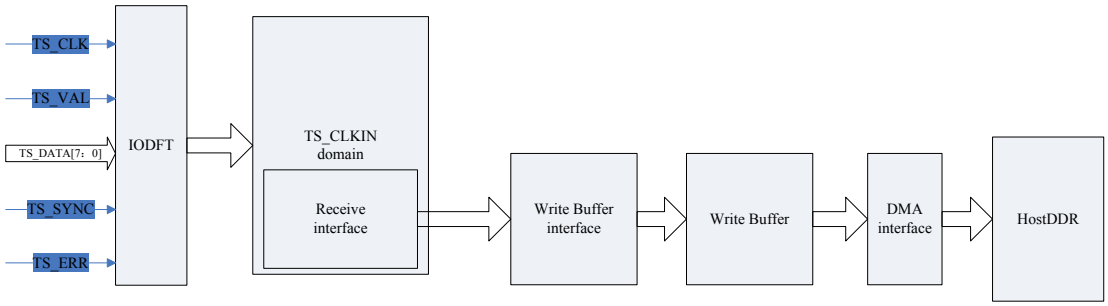


Figure 16-1 TSIF Block Diagram

16.3 Function Description

16.3.1 Timing Specifications

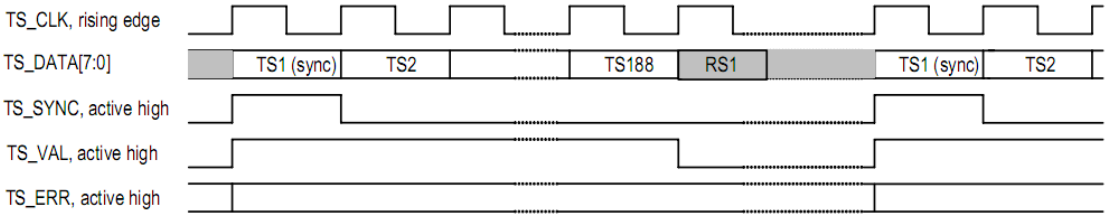


Figure 16-2 MPEG-2 TS parallel output interface

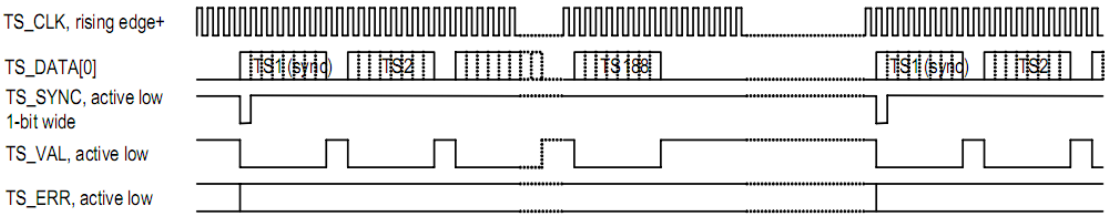


Figure 16-3 MPEG-2 TS serial output interface

16.4 Register List

Table 16-1 TSIF Controller Registers Address

Name	Physical Base Address
TSIF	0xB023C000

Table 16-2 TSIF Controller Registers

Offset	Register Name	Description
0x00	TS_CTRL	TSIF Control Register
0x04	TS_STATUS	TS STATUS Register
0x08	TS_RXDATA	TS Receive FIFO Data Register

16.5 Register Description

16.5.1 TS_CTRL

TS Control Register
Offset=0x00

Bits	Name	Description	Access	Default
31:14	-	Reserved	-	-
13	TSBL	Transport stream big little endian 0:big endian 1:little endian	RW	0
12	DRQEN	RX DRQ Enable. 0: Disable 1: Enable	RW	0
11	RIEN	RX IRQ Enable. 0: Disable 1: Enable	RW	0
10	TSER	Transport Stream Error Control 0 = error packet receive (default) 1 = error packet reject	RW	0
09	TSEP	Transport Stream Error Polarity. 0 = Active high (default) 1 = Active low	RW	0
08	TSVP	Transport Stream Valid Polarity. 0 = Active high (default) 1 = Active low	RW	0
07	TSSP	Transport Stream Sync Polarity. 0 = Active high (default) 1 = Active low	RW	0
06	TSSL	Transport Stream Start Length. 0 = Byte wide (default) 1 = Bit wide Note: This bit is ignored in parallel mode.	RW	0
05	TSCE	Transport Stream Clock Edge. 0 = Data transitions on rising edge (default) 1 = Data transitions on falling edge	RW	0

04	TSDF	Transport Stream Serial Data Format 0 = MSB first (default) 1 = LSB first Note: This bit is ignored in parallel mode	RW	0
01	TSM	Transport Stream Mode. 0 = Serial (default) 1 = Parallel	RW	0
00	EN	0: TSIF is inactivated. 1: TSIF is activated.	RW	0

Note: This register is mainly used to configure the controller to fit the application.

16.5.2 TS_STATUS

TS STATUS Register
Offset=0x04

Bits	Name	Description	Access	Default
31:3	-	Reserved	-	-
2	PIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to this bit will clear it.	RW	0
1	overflow	0: buffer no over flow 1:buffer over flow Write 1 clear	RW	0
0	PKT_ERR_STATUS	Receive packet status error. 0:No err condition occurs. 1: err has occurred. Write 1 clear	RW	0

16.5.3 TS_RXDATA

TS Receive FIFO Data Register
Offset=0x08

Bits	Name	Description	Access	Default
31:0	RXDAT	Receive Data. The depth of RXFIFO is 32bit×64 levels.	R	x

16.6 Application Note

17 LCDC (LCD Controller)

17.1 Overview

LCDC is the display interface controller between application processor and the display panel. Its main purpose is to convert the pixel stream output from the display engine to the standard LCD display panels. Features of LCDC are listed below.

- Support active (TFT) LCD panels with 24-bits digital RGB input interface
- Programmable timing control for various panels
- Pixel stream input without strict timing requirements
- Resolutions up to 1920*1080
- Maximum 16777216 simultaneous display color
- Fill the empty field when output size is smaller than LCD display size
- Support VBI, HBI, AVSI, FEI (Frame end interrupt)

LVDS

- Support dual channel LVDS interface LCD
- Comply with the TIA/EIA-644-A LVDS standard
- Support reference clock frequency range from 10MHz to 148.5MHz
- Support LVDS RGB 24/18 bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, Odd/Even channel Mirror/Swap,

17.2 Block Diagram

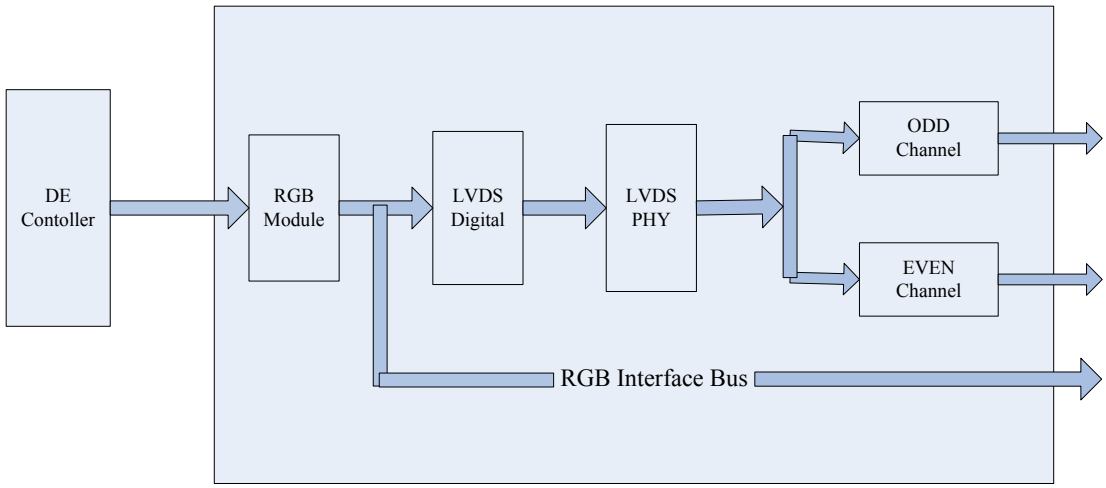


Figure 17-1 LCDC interface & data flow Diagram

17.3 Function Description

17.3.1 RGB LCD Interface

17.3.1.1 RGB LCD Pin Mapping

For RGB interface, system keep continuously input data frame by frame and keep the display LCD refreshing meanwhile the timing generator output the Vsync, Hsync, LDE and DCLK signals.

Table 17-1 RGB interface

RGB										
Pin Name	Serial 8-bit Bus						Parallel 24-bit Bus			
	18-bit			24-bit			8-color	16-bit	18-bit	24-bit
	1st	2nd	3rd	1st	2nd	3rd				
LCD_DO										B0
LCD_D1										B1
LCD_D2	R2	G2	B2	R0	G0	B0			B2	B2
LCD_D3	R3	G3	B3	R1	G1	B1		B3	B3	B3
LCD_D4	R4	G4	B4	R2	G2	B2		B4	B4	B4
LCD_D5	R5	G5	B5	R3	G3	B3		B5	B5	B5
LCD_D6	R6	G6	B6	R4	G4	B4		B6	B6	B6
LCD_D7	R7	G7	B7	R5	G5	B5	Bmsb	B7	B7	B7
LCD_D8										G0
LCD_D9										G1
LCD_D10				R6	G6	B6		G2	G2	G2
LCD_D11				R7	G7	B7		G3	G3	G3
LCD_D12								G4	G4	G4
LCD_D13								G5	G5	G5
LCD_D14								G6	G6	G6
LCD_D15							Gmsb	G7	G7	G7
LCD_D16										R0
LCD_D17										R1
LCD_D18									R2	R2
LCD_D19								R3	R3	R3
LCD_D20								R4	R4	R4
LCD_D21								R5	R5	R5
LCD_D22								R6	R6	R6
LCD_D23							Rmsb	R7	R7	R7

17.3.1.2 RGB Timing

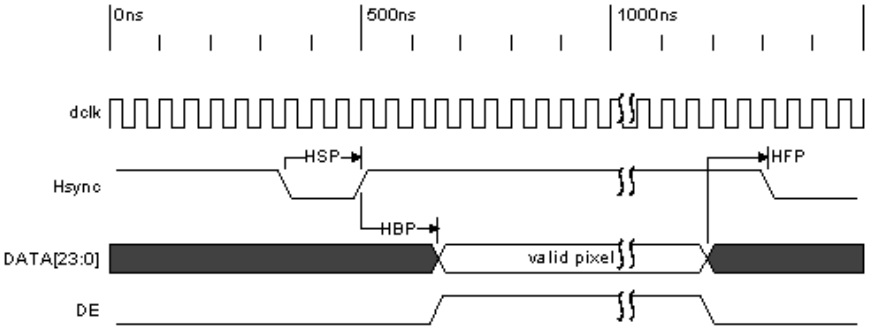


Figure 17-2 Parallel Mode Timing 1

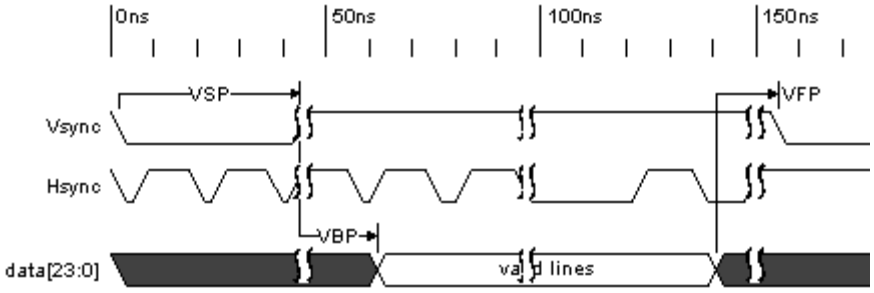


Figure 17-3 Parallel Mode Timing 2

Make a reference to the “Parallel Mode Timing”. The only difference between parallel timing and serial timing is: when in serial mode, the RED,GREEN and BLUE ingredients of each pixel should be transmitted in serial (for example, 1st phase R[7:0], 2nd phase G[7:0], 3rd phase B[7:0], so the DCLK frequency will be triple as it’s in parallel mode.)

Make a reference to the “Parallel Mode Timing”. The only difference between parallel timing and serial timing is: when in serial mode, the RED,GREEN and BLUE ingredients of each pixel should be transmitted in serial (for example, 1st phase R[7:0], 2nd phase G[7:0], 3rd phase B[7:0], so the DCLK frequency will be triple as it’s in parallel mode.)

17.3.1.3 RGB AC characters

Table 17-2 AC characters list

parameter	symbol	Min.	Typ.	Max.	Unit.	remark
Dclk frequence	f_dclk	3		33	MHz	
Dclk dutycycle	Tcw	40	50	60	%	
signal setup	Tst	3	6	-	ns	
signal hold	Thld	3	6	-	ns	
signal raise	Ts	3			ns	
signal fall	Tf	3			ns	
Bus load	Cload	10	-	15	pf	Single signal

17.3.2 LVDS LCD Interface

17.3.2.1 Bit Mapping

The LVDS Tx interface consists of 8 data channels & 2 clock channels (5 even channels, 5 odd channels), each channel is 7-bit width. Figure below shows the bit mapping diagram of the LVDS Tx interface under single channel mode.

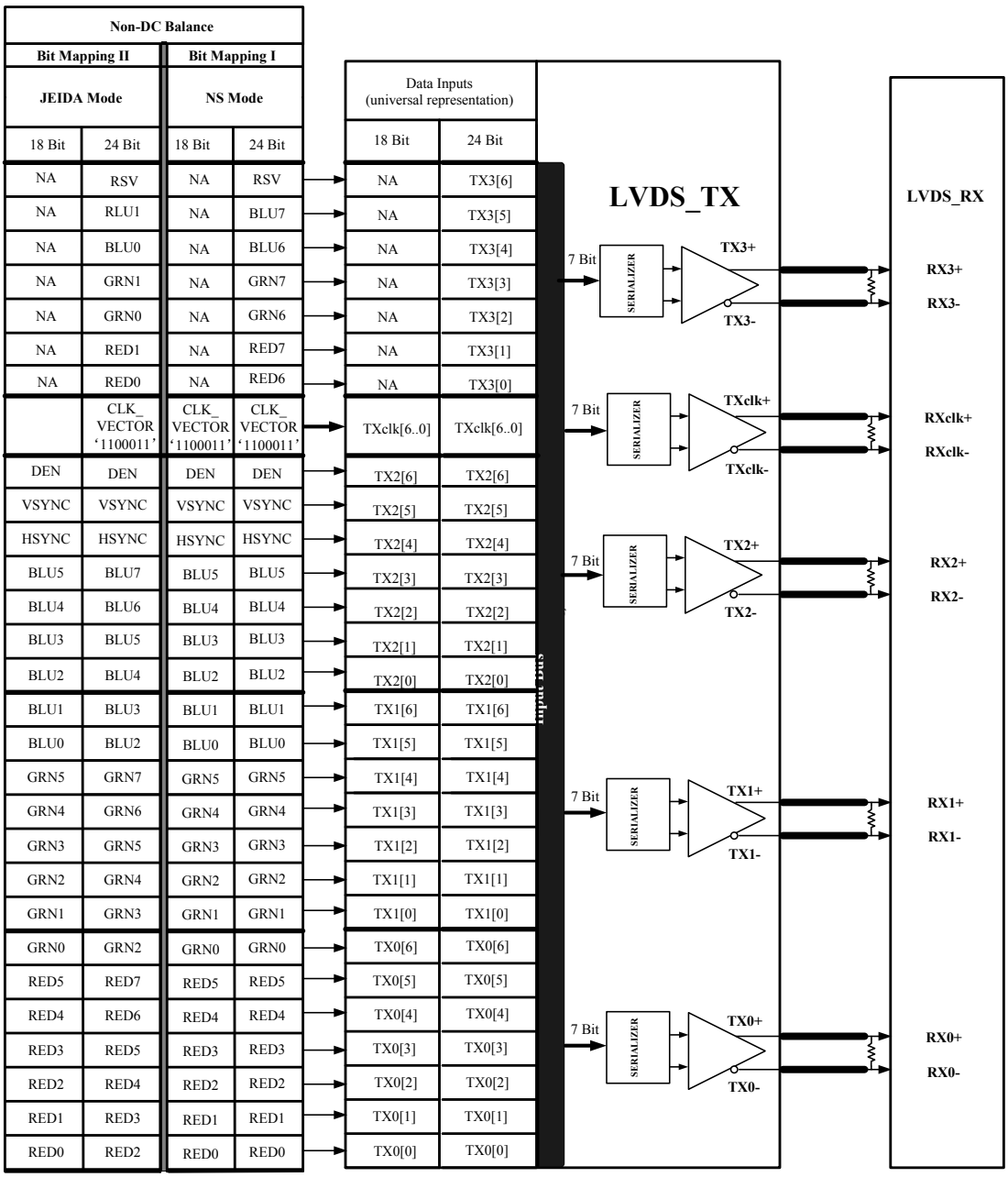


Figure 17-4 LVDS Bit Mapping

Table below shows port mapping of the LVDS Tx channels. The mapping format is chosen according to the following operation mode & swap functions:

1. 18-bit or 24-bit data format.
2. Single or dual channel mode.
3. Odd/even channel swap.
4. Mirror swap.

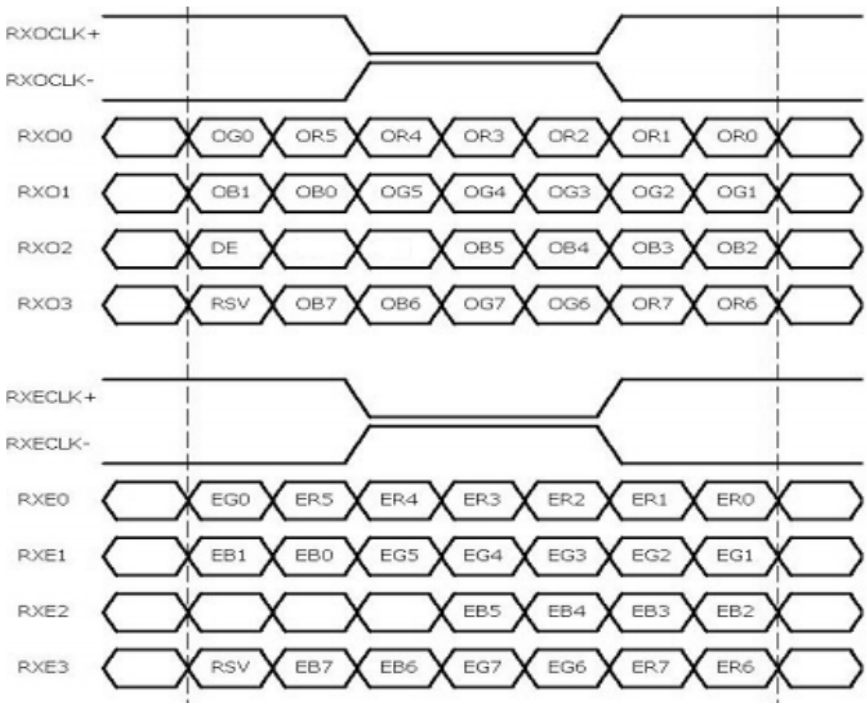


Figure 17-5 LVDS Data Format

Table 17-3 LVDS Port Mapping

PIN	1	2	3	4	5	6	7	8	9	10	11	12
EAN	Tx0-	TxCLK+	TxO0-	TxECLK+	TxE0-	TxOCLK+	Tx0-	Tx3+	TxO0-	TxE3+	TxE0-	TxO3+
EAP	Tx0+	TxCLK-	TxO0+	TxECLK-	TxE0+	TxOCLK-	Tx0+	Tx3-	TxO0+	TxE3-	TxE0+	TxO3-
EBN	Tx1-	Tx2+	TxO1-	TxE2+	TxE1-	TxO2+	Tx1-	TxCLK+	TxO1-	TxECLK+	TxE1-	TxOCLK+
EBP	Tx1+	Tx2-	TxO1+	TxE2-	TxE1+	TxO2-	Tx1+	TxCLK-	TxO1+	TxECLK-	TxE1+	TxOCLK-
ECN	Tx2-	Tx1+	TxO2-	TxE1+	TxE2-	TxO1+	Tx2-	Tx2+	TxO2-	TxE2+	TxE2-	TxO2+
ECP	Tx2+	Tx1-	TxO2+	TxE1-	TxE2+	TxO1-	Tx2+	Tx2-	TxO2+	TxE2-	TxE2+	TxO2-
EDN	TxCLK-	Tx0+	TxOCLK-	TxE0+	TxECLK-	TxO0+	TxCLK-	Tx1+	TxOCLK-	TxE1+	TxECLK-	TxO1+
EDP	TxCLK+	Tx0-	TxOCLK+	TxE0-	TxECLK+	TxO0-	TxCLK+	Tx1-	TxOCLK+	TxE1-	TxECLK+	TxO1-
EEN							Tx3-	Tx0+	TxO3-	TxE0+	TxE3-	TxO0+
EEP							Tx3+	Tx0-	TxO3+	TxE0-	TxE3+	TxO0-
OAN			TxE0-	TxOCLK+	TxO0-	TxECLK+			TxE0-	TxO3+	TxO0-	TxE3+
OAP			TxE0+	TxOCLK-	TxO0+	TxECLK-			TxE0+	TxO3-	TxO0+	TxE3-
OBN			TxE1-	TxO2+	TxO1-	TxE2+			TxE1-	TxOCLK+	TxO1-	TxECLK+
OBP			TxE1+	TxO2-	TxO1+	TxE2-			TxE1+	TxOCLK-	TxO1+	TxECLK-
OCN			TxE2-	TxO1+	TxO2-	TxE1+			TxE2-	TxO2+	TxO2-	TxE2+
OCP			TxE2+	TxO1-	TxO2+	TxE1-			TxE2+	TxO2-	TxO2+	TxE2-
ODN			TxECLK-	TxO0+	TxOCLK-	TxE0+			TxECLK-	TxO1+	TxOCLK-	TxE1+
ODP			TxECLK+	TxO0-	TxOCLK+	TxE0-			TxECLK+	TxO1-	TxOCLK+	TxE1-
OEN									TxE3-	TxO0+	TxO3-	TxE0+
OEP									TxE3+	TxO0-	TxO3+	TxE0-
	18bit						24bit					

17.4 Register List

Table 17-4 LCD BLOCK Base Address

Name	Physical Base Address
LCD	0xB02A0000
LVDS	0xB02A0200

Table 17-5 LCD0 BLOCK Registers List

Offset	Register Name	Description
0x0000	LCD0_CTL	LCD Control register

0x0004	LCD0_SIZE	LCD Size register
0x0008	LCD0_STATUS	LCD Status register
0x000C	LCD0_TIM0	LCD RGB Timing0 register
0x0010	LCD0_TIM1	LCD RGB Timing1 register
0x0014	LCD0_TIM2	LCD RGB Timing2 register
0x0018	LCD0_COLOR	LCD Color register
0x002c	LCD0_IMG_XPOS	LCD image x position in the screen
0x0030	LCD0_IMG_YPOS	LCD image y position in the screen

Table 17-6 LVDS BLOCK Registers List

Offset	Register Name	Description
0x0000	LVDS_CTL	LVDS Control Register
0x0004	LVDS_ALG_CTL0	LVDS Anlaog Control Regiser 0

17.5 Register Description

17.5.1 LCD0_CTL

LCD RGB Control register
This register is mainly used to configure the controller to fit the specified RGB IF panel
Offset = 0x0000

Bits	Name	Description	Access	Reset
31	-	Reserved	-	-
30	SELF_RST	Self reset enable 0:disable, do not reset when DE_LCD_ST rising edge 1:enable, reset when DE_LCD_ST rising edge	RW	0
29	3D_EN	3D mode output enable 0:disable 1:enable	RW	0
28:21	-	Reserved	-	-
20	PD_IDL_STA	LCD pad idle state configration: 0:default level. 1:all LCD pad are drive low. *Note:* *1,if you set this bit, the output of all LCD pads will be low .* *2,if you want send normal data to LCD, this bit must be cleared.*	RW	0
19	-	Reserved	-	-
18:16	PAR_SER_SEL	Panel RGB Interface Type Select 000:24-bit parallel 001:18-bit parallel 010:16-bit(5-6-5 format) parallel 011:8-color mode parallel 100:24-bit(8-8-8 format) serial 101:18-bit(6-6-6 format) serial 110,111:Reserved *Note:* *The unused pins of LD[23:0] should be in stable*	RW	0

		output state to avoid EMI. FOR RGB IF ONLY		
15:13	CC_ODD	LCD color sequence configuration for odd line 000:RGB 001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other: Reserved	RW	0
12:10	CC_EVEN	LCD color sequence configuration for even line 000:RGB 001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other:Reserved	RW	0
9:8	PAD	Color padding to 32 bit/pixel 00:do not pad 01:pad X after 10:pad X before 11:Reserved For example: f CC_ODD=0 and PAD=01, then the serial output should be RGBX. FOR RGB IF ONLY	RW	0
7:6	VOM	Video Output Mode 10:Drive the LCD0 with video from DE0. 11:Drive the LCD0 with default color.	RW	0x3
5:1	-	Reserved	-	-
1	RB_SWAP	Swap R,B in input data 0:R,B NO SWAP 1:R,B SWAP	RW	0
0	EN	LCDC ENABLE 0:disable 1:enable	RW	0

17.5.2 LCD0_SIZE

LCD RGB Size register
Offset = 0x0004

Bits	Name	Description	Access	Reset
31:27	-	Reserved	-	-
26:16	Y	Screen Height (in pixels) for RGB IF Panel height is Y+1	RW	0
15:12	-	Reserved	-	-
11:0	X	Screen Width (in pixels) for RGB IF Panel width is X+1	RW	0

17.5.3 LCD0_STATUS

LCD0 Status register
Offset = 0x0008

Bits	Name	Description	Access	Reset
31	VBI	Vertical Blanking pending Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period Write '1' clear.	RW	0
30	VBE	VB interrupt enable	RW	0
29	HBI	Horizontal Blanking state Asserted during horizontal no-display period every scan line. Interrupt triggered at the beginning of blanking period Write '1' clear.	RW	0
28	HBE	HB interrupt enable	RW	0
27	AVSI	Active Video Display pending Asserted during active video display time for each line, Interrupt triggered at the beginning of active period for each line Write '1' clear.	RW	0
26	AVSE	AVS interrupt enable	RW	0
25	FEIP	Frame trans end interrupt pending Write '1' clear.	RW	0
24	FEIE	FEI enable	RW	0
23	-	Reserved	-	-
22:11	CX	Current scan pixel's x axis location (in pixels)	R	1
10:0	CY	Current scan pixel's y axis location (in pixels)	R	0

17.5.4 LCD0_TIM0

LCD0 RGB Timing0 register
Offset = 0x000C

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	PREL_EN	Pre_line enable 1:enable pre_line function 0:disable pre_line function	RW	0
12:8	PREL_CNT	Pre_line counter. if this counter set x, the LCDC will send a pre_line signal to DE when is has send [VSPW-x)] valid horizontal data pluse.	RW	0
7	VSYNC_INV	Vsync Output Polarity Inversion	RW	0
6	HSYNC_INV	Hsync Output Polarity Inversion	RW	0
5	DCLK_INV	DCLK Output Polarity Inversion	RW	0
5	-	Reserved	-	-
4	LDE_INV	LDE Output Polarity Inversion	RW	0
3:0	-	Reserved	-	-

Notes:
*When we define the timing parameters, it often refers to Tpclk (short for "pixel cycle period"). In parallel output mode, Tpclk = Tdclk; in serial mode, Tpclk = Tdclk * 3.*

17.5.5 LCD0_TIM1

LCD0 RGB Timing1 register

Offset = 0x0010

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:20	HSPW	Horizontal Sync Pulse Width (in pixels) Thspw = (HSPW+1) * Tpclk	RW	0
19:10	HFP	Horizontal Front Porch (in pixels) Thfp = (HFP +1) * Tpclk	RW	0
9:0	HBP	Horizontal Back Porch (in pixels) Thbp = (HBP +1) * Tpclk	RW	0

17.5.6 LCD0_TIM2

LCD0 RGB Timing2 register
Offset = 0x0014

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:20	VSPW	Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Thsync	RW	0
19:10	VFP	Vertical Front Porch (in lines) Tvfp = (VFP +1) * Thsync	RW	0
9:0	VBP	Vertical Back Porch (in lines) Tvbp = (VBP +1) * Thsync	RW	0

17.5.7 LCD0_COLOR

LCD0 Color register
Offset = 0x0018

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	R	panel's default color R	RW	0
15:8	G	panel's default color G	RW	0
7:0	B	panel's default color B	RW	0

17.5.8 LCD0_IMG_XPOS

LCD0 image x position in the screen
Offset = 0x002C

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	XSTART	At which line does the image begin	RW	0
15:12	-	Reserved	-	-
11:00	XEND	At which line does the image end	RW	0

17.5.9 LCD0_IMG_YPOS

LCD0 image y position in the screen
Offset = 0x0030

Bits	Name	Description	Access	Reset
31:27	-	Reserved	-	-

26:16	YSTART	At which column does the image begin	RW	0
15:11	-	Reserved	-	-
10:00	YEND	At which column does the image end	RW	0

17.5.10 LVDS_CTL

LVDS Control Register
Offset = 0x0000

Bits	Name	Description	Access	Reset
31:22	-	Reserved	R	0
21	L	RGB to LVDS clock polarity select 0:normal 1:inverse	RW	0
20	E_RSV	Even Port RSV Signal Select 0:Always '0' 1:Always '1'	RW	0
19:18	E_DE	Even Port DE Signal Select 00:Always '0' 01:Always '1' 1x:DE	RW	0
17:16	E_VS	Even Port VS Signal Select 00:Always '0' 01:Always '1' 1x:VS	RW	0
15:14	E_HS	Even Port HS Signal Select 00:Always '0' 01:Always '1' 1x:HS	RW	0
13	O_RSV	Odd Port RSV Signal Select 0:Always '0' 1:Always '1'	RW	0
12:11	O_DE	Odd Port DE Signal Select 00:Always '0' 01:Always '1' 1x:DE	RW	0
10:9	O_VS	Odd Port VS Signal Select 00:Always '0' 01:Always '1' 1x:VS	RW	0
8:7	O_HS	Odd Port HS Signal Select 00:Always '0' 01:Always '1' 1x:HS	RW	0
6	MIRROR	LVDS Mirror Select 0:Normal (TXE3+ TXE3- … TXO0+ TIO0-) 1:Mirror (TXO0+ TXO0- … TXE3+ TIE3-)	RW	0
5	CH_SWAP	LVDS Channel Swap Select 0:No Swap 1:Odd/Even Swap	RW	0
4:3	MAPPING	Output Mapping Select 00:Bit Mapping I 01:Bit Mapping II	RW	0

		Others:Reserved		
2	CHANNEL	Channel Select 0:Single Channel 1:Dual Channel	RW	0
1	FORMAT	Output Format 0:18-bit 1:24-bit	RW	0
0	EN	LVDS Interface Enable 0:Disable 1:Enable (LVDS & RSDS can't be both enabled)	RW	0

17.5.11 LVDS_ALG_CTL0

LVDS Analog Control Register 0
Offset = 0x0004

Bits	Name	Description	Access	Reset
31	IBPOWL	Bias current on&off	RW	0
30	PLLPOWL	PLL power on	RW	0
29:26	-	Reserved	R	0
25:24	SLVDSIL	Set LVDS Tx CMFB Circuit Bias Current 'IBLV<14:0>' (IBLV<14>, IBLV<13> not used) 20u*[1]+10u*[0]+60u	RW	0x2
23	-	Reserved	R	0
22:20	SVOCML	Set LVDS Tx common mode reference voltage 'vocm' 000:1.04V 001:1.08V 010:1.13V 011:1.18V 100:1.22V 101:1.27V 110:1.32V 111:1.37V	RW	0x4
19:18	-	Reserved	R	0
17:15	SPLLIL	Set PLL charge pump current 20u*[2]+10u*[1]+5u*[0]+5u	RW	0x3
14:13	SPLLRL	Set PLL LPF resistor 00:6k 01:8k 10:10k 11:12k	RW	1
12:11	WDMODEL	PLL watch dog mode 00:WD active 01:set vc=1.5 1x:Disable WD	RW	0
10	PLLPOLARL	PLL input clock delay 180°or not 0:not delay 1:delay	RW	0
9:7	-	Reserved	-	-
6	POLARL	LVDS/RSDS output signal polarity control 0:polarity not changed 1:polarity reversed (all ! P/N swap)	RW	0

5	ELVDSPOWL	EVEN PORT Output driver power on	RW	1
4	OLVDSPOWL	ODD PORT Output driver power on	RW	1
3	OCKPOLARL	Bring forward ODD PORT channel [D] Serializers clock 'CKOUT' 180°or not ('CKSEL' is also brought forward half period of 'CKOUT') 0:not 1:ahead 180°	RW	0
2	ECKPOLARL	Bring forward EVEN PORT channel [D] Serializers clock 'CKOUT' 180°or not ('CKSEL' is also brought forward half period of 'CKOUT') 0:not 1:ahead 180°	RW	0
1	ENVBPBL	Bring forward DUAL-PORT (except channel [D]) Serializes clock 'CKOUT' 180°or not ('CKSEL' is also brought forward half period of 'CKOUT') 0:not 1:ahead 180°	RW	0
0	LVDS_LOCK	LVDS PLL status	R	0

17.6 Application Note

18 MIPI DSI

18.1 Overview

MIPI DSI (Display Serial Interface) is the standard display interface that complies with MIPI Alliance. The DSI Host Controller deals with data transmitting and receiving. When transmitting data, DSI Host Controller may work in High-Speed mode or Low-power mode; when receiving data, DSI Host Controller works in Low-Power mode only. Features of MIPI DSI in S500 is listed below:

- Compliant with MIPI DSI Specification version 1.01 and the D-PHY specification version 0.9
- Display Resolutions up to 1080p
- Pixel Format:
  - Command Mode: RGB233, RGB444, RGB565, RGB666(Loosely), and RGB888
  - Video Mode: RGB565, RGB666 (Packed), RGB666(Loosely), and RGB888
- Command and Video mode support(type 1,2,3 and 4 display architecture)
- Low power and ultra low power support
- 75 Mbps to 1Gbps per lane
- Support 1-4 data lanes

18.2 Block Diagram

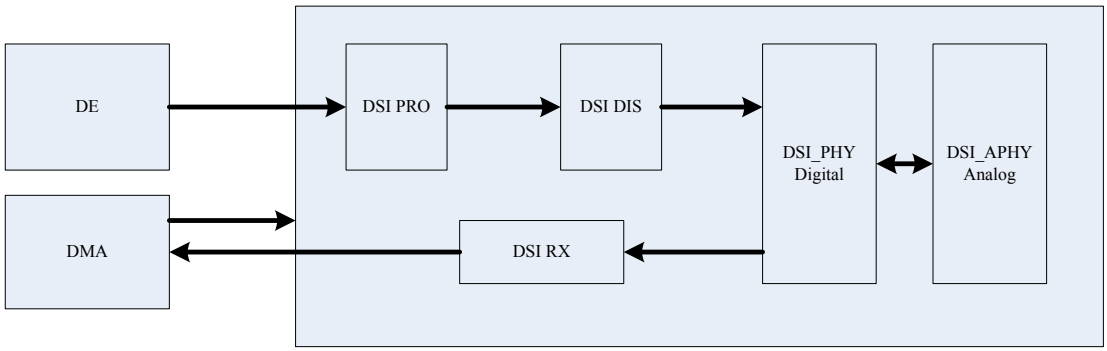


Figure 18-1 MIPI DSI Block Diagram

18.3 Function Description

DSI Host Controller supports two transmission modes: Command mode and Video Mode. When working in CMD Mode, the DSI Host Controller shall start a packet transfer by software; When working in Video Mode, the DSI Host Controller shall start the packet transmission automatically without software interfering.

DSI Host Controller fetches pixel data from DE, and packs the data into RGB packets, then sends the packet when transmitting data; when receiving data, DSI Host Controller receive the packet, unpack the packet and store the data into FIFO. BDMA may carry the data into LCD by FIFO.

Details about DSI, please refer to < *MIPI Alliance Standard for Display Serial Interface*>.

18.4 Register List

Table 18-1 MIPI DSI Host Controller Registers Address

Name	Physical Base Address
DSI	0xB0220000

Table 18-2 MIPI DSI Controller Registers

Offset	Register Name	Description
0x00	DSI_CTRL	DSI Control Register
0x04	DSI_SIZE	DSI Screen Size Register
0x08	DSI_COLOR	DSI Default Color Register
0x0C	DSI_VIDEO_CFG	DSI Video Configure Register
0x10	DSI_RGBHT0	DSI RGB Hsync Timing0 Register
0x14	DSI_RGBHT1	DSI RGB Hsync Timing1 Register
0x18	DSI_RGBVT0	DSI RGB Vsync Timing0 Register
0x1C	DSI_RGBVT1	DSI RGB Vsync Timing1 Register
0x20	DSI_TIMEOUT	DSI Time Out Register
0x24	DSI_TR_STA	DSI Transfer State Register
0x28	DSI_INT_EN	DSI Interrupt Enable Register
0x2C	DSI_ERROR_REPORT	DSI Error Report Register
0x30	DSI_FIFO_ODAT	DSI FIFO Output Data Register
0x34	DSI_FIFO_IDAT	DSI FIFO Input Data Register
0x38	DSI_IPACK	DSI Input Packet Information Register
0x40	DSI_PACK_CFG	DSI Packet Configure Register
0x44	DSI_PACK_HEADER	DSI Packet Header Register
0x48	DSI_TX_TRIGGER	DSI TX Trigger Register
0x4C	DSI_RX_TRIGGER	DSI RX Trigger Register
0x50	DSI_LANE_CTRL	DSI Lane Control Register
0x54	DSI_LANE_STA	DSI Lane State Register
0x60	DSI_PHY_T0	DSI PHY Timing0 Register
0x64	DSI_PHY_T1	DSI PHY Timing1 Register
0x68	DSI_PHY_T2	DSI PHY Timing2 Register
0x80	DSI_PHY_CTRL	PHY Control Register

18.5 Register Description

18.5.1 DSI_CTRL

DSI Control Register
Offset=0x00

Bit(s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	TR_MODE	0:Command Mode 1:Video Mode	RW	0
11:10	VC	Virtual channel number(also for Odd Field in Interlaced Video)	RW	0
09:08	DL_NUM	Data Lane Number 00:Data Lane 0 (1 Data Lane) 01:Data Lane 0 ~ 1 (2 Data Lanes) 10:Data Lane 0 ~ 2 (3 Data Lanes) 11:Data Lane 0 ~ 3 (4 Data Lanes)	RW	0
07	VOM	Video Output Mode	RW	0

		0:Drive the panel with video from DE 1:Drive the panel with default color		
06	CON_CLK	Continue Clock Lane 1:Continue Clock Lane 0:non-Continue Clock Lane	RW	0
05	RB_SWAP	Swap R, B in input data 0:R, B NO SWAP 1:R, B SWAP	RW	0
04	EOTP_EN	EOTP Enable 0:Disable 1:Enable *Note:Devices compliant to DSI spec v1.0 and earlier do not support EOTP*	RW	0
03	SOFT_RST	Soft Reset for RX FIFO and RX Logic when received error occurs. 0:no Reset 1:Reset	RW	0
02:00	-	Reserved	-	-

Note:This register is mainly used to configure the controller to fit the application.

18.5.2 DSI_SIZE

DSI Screen Size Register
Offset=0x04

Bit(s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	Y	Active lines per frame (Active lines per field for interlaced video) The actual value is Y	RW	0
15:00	-	Reserved	-	-

*Note:This register is used to configure the size of the active pixel per line and active lines per frame. Support up to 2048*2048.*

18.5.3 DSI_COLOR

DSI Default Color Register
Offset=0x08

Bit(s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	R	panel's default color R	RW	0
15:08	G	panel's default color G	RW	0
7:0	B	panel's default color B	RW	0

Note:This register specifies panel's default color.

18.5.4 DSI_VIDEO_CFG

DSI Video Configure Register
Offset=0x0C

Bit(s)	Name	Description	Access	Reset
30:15	-	Reserved	-	-

14	HSA_PS_EN	HSA period in Video mode Power-Saving Mode Enable (only active in Non-Burst Mode with Sync Pulses mode) 1:Enable 0:Disable	RW	0
13	HBP_PS_EN	HBP period in Video mode Power-Saving Mode Enable 1:Enable 0:Disable	RW	0
12	HFP_PS_EN	HFP period in Video mode Power-Saving Mode Enable 1:Enable 0:Disable	RW	0
11	-	Reserved	-	-
10:08	RGB_FM	RGB Color Format 000:16-bit Format(RGB565) 001:18-bit Packed Format(RGB666) 010:18-bit Loosely Packed Format(RGB666) 011:24-bit Format(RGB888) Others:Reserved	RW	0
07	-	Reserved	-	-
06:05	EVEN_VC	Virtual channel number For Even Filed (Only Active for Interlaced Video)	RW	0
04	SCAN_MODE	Video Scan Format Select 0:Progressive 1:Interlaced	RW	0
03	POWER_SAVE	Power-Saving Mode Enable 1:Enable 0:Disable	RW	0
02:01	VMS	Video Mode Select 00:Non-Burst Mode with Sync Pulses(Sync mode) 01:Non-Burst Mode with Sync Events(DE mode) 10:Burst Mode(time-compressed mode) 11:Reserved	RW	0
00	EN	Video Mode Start to process 1:Enable 0:Disable	RW	0

Note:This register is mainly used to configure the video mode. (Only for video mode)

18.5.5 DSI_RGBHT0

DSI RGB Hsync Timing0 Register
Offset=0x10

Bit(s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:20	HAS	Horizontal Sync Active Width T_{hsa} = (HAS+6) * T_{DSI_Clk} / DL_NUM	RW	0
19:10	HFP	Horizontal Front Porch T_{hfp} = (HFP +6) * T_{DSI_Clk} / DL_NUM	RW	0
9:0	HBP	Horizontal Back Porch T_{hbp} = (HBP +6) * T_{DSI_Clk} / DL_NUM	RW	0

Note:
This register specifies timing parameters of the horizontal sync signal.
The timing settings include Packet Header and Packet Foot.

18.5.6 DSI_RGBHT1

DSI RGB Hsync Timing1 Register
Offset=0x14

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:00	BLLP	Blanking or Low-Power Interval T_{BLLP} = (BLLP +6) * T_{DSI_Clk} / DL_NUM	RW	0

Note:
This register specifies timing parameters of the BLLP for burst mode.
The timing settings has include Packet Header and Packet Foot.

18.5.7 DSI_RGBVT0

DSI RGB Vsync Timing0 Register
Offset=0x18

Bit(s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:24	VFL	DSI_Vsync (to DE) Falling-edge to Active Line Distance 0x0:Reserved; 0x1:1 lines; 0x2:2lines; 0x3:3 lines; …… 0xc:12 lines; 0xd:13 lines; 0xe:14 lines; 0xF:15 lines	RW	0
23:20	PLS	DSI Preline Number Set (to DE) 0x0:1 line; 0x1:2 lines; … 0xE:15 lines; 0xF:16 lines	RW	0
19:13	VSA	Vertical Sync Active Width (in lines) T_{vsa} = VSA * T_{line}	RW	0
12:00	LTOTAL	Total Line in one frame (in lines) T_{ltotal} = LTOTAL * T_{line} *Note:1 field /1frame of Progressive; 2 fields/1 frame of Interlaced.*	RW	0

Note:This register specifies timing parameters of the vertical sync signal.

18.5.8 DSI_RGBVT1

DSI RGB Vsync Timing1 Register
Offset=0x1C

Bit(s)	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:16	LSEF	Active Line Start Position in Even field of Interlaced scan	RW	0
15:12	-	Reserved	-	-
11:00	LSOF	Active Line Start Position in Progressive scan or Odd field of Interlaced scan	RW	0

Note:This register specifies timing parameters of the vertical sync signal.

18.5.9 DSI_TIMEOUT

DSI Time Out Register
Offset=0x20

Bit(s)	Name	Description	Access	Reset

31:24	-	Reserved	-	-
23:00	BTA_TO	Time for BTA timeout Specify time out from Host initiate BTA request to bus grant turns over form DSI peripheral to DSI Host with respect to TX escape clock.	RW	0

Note:This register specifies the time of BTA time-out.

18.5.10 DSI_TR_STA

DSI Transfer State Register
Offset=0x24

Bit(s)	Name	Description	Access	Reset
31	VBI	Vertical Blanking Interrupt Pending(Video Mode) Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period. Write 1 to clear.	RW	0
30:20	-	Reserved	-	-
19	TCIP	Transfer Complete Interrupt Pending Bit(CMD Mode) 0:Transfer is not Complete 1:Transfer is Complete Write 1 to clear the bit *Note:After a command mode transfer or a trigger transfer finish, the bit is set to 1*	RW	0
18	BUS_TURNOVER	Indicates when Bus grant turns over from DSI Peripheral to DSI Host 0:Bus Turn over not finish 1:Bus grant turns over from DSI Peripheral to DSI Host Write 1 to clear the bit	RW	0
17	RX_DAT_DONE	Indicates when a LPDT packet (except for Ack and Error report packet) is received 0:no LPDT packet is received 1:a LPDT packet is received Write 1 to clear the bit	RW	0
16	RX_ACK_PACK	Indicates when an Ack and Error report packet is received. 0:no Ack and Error report packet is received 1:an Ack and Error report packet is received Write 1 to clear the bit	RW	0
15	RX_TRIGGER	Indicates when a RX Trigger is received. 0:no RX Trigger is received 1:a RX Trigger is received Write 1 to clear the bit	RW	0
14:11	-	Reserved	-	-
10	UDF	Output FIFO underflow pending bit Set when output FIFO is empty, hardware still detects the write pointer of FIFO move. 0:no error occurred 1:error occurred Write 1 to clear the bit	RW	0
09	OVF	Input FIFO overflow pending bit	RW	0

		Set when input FIFO is full, hardware still detects the write pointer of FIFO move. 0:no error occurred 1:error occurred Write 1 to clear the bit		
08	IFIFO_EMP	Input FIFO Empty Flag 0:Not Empty 1:Empty *Note:this bit is used to tell the host whether data is received, because the FIFO sending data do not need to know, the sending situation is for certain.*	R	-
07	ERR_BTA_TO	BTA Time Out Error occur 0:no error occurred 1:a BTA Time Out Error occurred when initiate a BTA request Write 1 to clear the bit	RW	0
06	ERR_RX_CRC	Receive CRC Error Bit in LPDR 0:no error occurred 1:a CRC Error occurred when receiving long packet Write 1 to clear the bit	RW	0
05	ERR_RX_ECC	Receive ECC Error Bit in LPDR 0:no error occurred or a single-bit error occurs and corrected 1:multi-bit errors occur Write 1 to clear the bit	RW	0
04	ERR_ESC	Escape Mode Entry Error Pending Bit 0:no error occurred 1:an unrecognized escape entry command is received. Write 1 to clear the bit *Note:an unknown Entry Command is received, the bit is also set to '1'.*	RW	0
03	ERR_SYNC_ESC	Low-Power Data Transmission Synchronization Error 0:no error occurred 1:the number of bits received during a LPDT is not a multiple of eight when the transmission ends. Write 1 to clear the bit	RW	0
02	ERR_CONTROL	False Control Error 0:no error occurred 1:an incorrect line state sequence is detected. For example, if a BTA request or escape mode request is immediately followed by a Stop state instead of the required Bridge state. Write 1 to clear the bit	RW	0
01	ERR_CON_LP1	LP1 Contention Error 0:no error occurred 1:the lane module detects a contention situation on a line while trying to drive the line high Write 1 to clear the bit	RW	0
00	ERR_CON_LP0	LP0 Contention Error 0:no error occurred 1:the lane module detects a contention situation on a line while trying to drive the line low	RW	0

		Write 1 to clear the bit		

Note:This register reflects the transfer status of the controller.

18.5.11 DSI_INT_EN

DSI Interrupt Enable Register
Offset=0x28

Bit(s)	Name	Description	Access	Reset
31	VBI_EN	VBI interrupt pending enable 0:Disable; 1:Enable	RW	0
30:20	-	Reserved	-	-
19	TCIP_EN	TCIP interrupt pending enable 0:Disable; 1:Enable	RW	0
18	BUS_TURNOVER_EN	BUS_TURNOVER interrupt pending enable 0:Disable; 1:Enable	RW	0
17	RX_DAT_DONE_EN	RX_DAT_DONE interrupt pending enable 0:Disable; 1:Enable	RW	0
16	RX_ACK_PACK_EN	RX_ACK_PACK interrupt pending enable 0:Disable; 1:Enable	RW	0
15	RX_TRIGGER_EN	RX_TRIGGER interrupt pending enable 0:Disable; 1:Enable	RW	0
14:11	-	Reserved	-	-
10	UDF_EN	UDF interrupt pending enable 0:Disable; 1:Enable	RW	0
09	OVF_EN	OVF interrupt pending enable 0:Disable; 1:Enable	RW	0
08	-	Reserved	-	-
07	ERR_BTA_TO_EN	ERR_BTA_TO interrupt pending enable 0:Disable; 1:Enable	RW	0
06	ERR_RX_CRC_EN	ERR_RX_CRC interrupt pending enable 0:Disable; 1:Enable	RW	0
05	ERR_RX_ECC_EN	ERR_RX_ECC interrupt pending enable 0:Disable; 1:Enable	RW	0
04	ERR_ESC_EN	ERR_ESC interrupt pending enable 0:Disable; 1:Enable	RW	0
03	ERR_SYNC_ESC_EN	ERR_SYNC_ESC interrupt pending enable 0:Disable; 1:Enable	RW	0
02	ERR_CONTROL_EN	ERR_CONTROL interrupt pending enable 0:Disable; 1:Enable	RW	0
01	ERR_CON_LP1_EN	ERR_CON_LP1 interrupt pending enable 0:Disable; 1:Enable	RW	0
00	ERR_CON_LP0_EN	ERR_CON_LP0 interrupt pending enable 0:Disable; 1:Enable	RW	0

Note:This register enable or mask the interrupt sources.

18.5.12 DSI_ERROR_REPORT

DSI Error Report Register
Offset=0x2C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-

15:00	REPORT	Error Reporting Bit (Detailed description see MIPI DSI Spec 1.0) Before a new transfer is started, software must clear the bits to 0x0000	RW	0

Note:This register stores the Error Reporting Packet received from the peripherals.

18.5.13 DSI_FIFO_ODAT

DSI FIFO Output Data Register
Offset=0x30

Bits	Name	Description	Access	Reset
31:00	DATA	FIFO DATA for Output	RW	0

Note:The byte sequence is arranged in little-endian format. The right side (LSB) of the word is sent first. The data stored in LCD is word-aligned, so DSI Host Controller must discard several bytes if the word counter of sending data is not word-aligned.

4th byte	3rd byte	2nd byte	1st byte

MSB LSB

18.5.14 DSI_FIFO_IDAT

DSI FIFO Input Data Register
Offset=0x34

Bits	Name	Description	Access	Reset
31:00	DATA	FIFO DATA for Input	RW	0

Note:The byte sequence is arranged in little-endian format. That is the first byte received is on the right side (LSB) of the word. When the last bytes received cannot compose a word, the bytes should be placed on the right side (LSB) of the word. And FIFO's other bytes must be filled with 0xFF in order to satisfy the word- aligned rule.

4th byte	3rd byte	2nd byte	1st byte

MSB LSB

18.5.15 DSI_IPACK

DSI Input Packet Information Register
Offset=0x38

Bits	Name	Description	Access	Reset
31:25	-	Reserved	-	-
24	IPACK_TYPE	Input Packet Type: 0:Short Packet; 0x1:Long Packet	R	0
23:16	IPACK_DI	Input Packet Data Identifier	R	0
15:0	IPACK_WC	Input Packet Word Count	R	0

18.5.16 DSI_PACK_CFG

DSI Packet Configure Register (used in command mode)

Offset=0x40

Bits	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19:18	PT	Packet Type 00:Short Packet without reading back data 01:Long Packet (Normal Data From FIFO) 10:Long Packet(Pixel Data From DE) Others:Reserved *Note:When PT set to 10, Pixel Data must be sent in a packet per line.*	RW	0
17	-	Reserved	-	-
16	CRC_CK_EN	CRC Check Enable 0:Disable 1:Enable when receiving data	RW	0
15	-	Reserved	-	-
14	TR_MODE	Transmission Mode Select 0:High-Speed 1:Low-Power *Note:High-Speed is preferred. If fetch data from DE, High-Speed mode is only allowed.*	RW	0
13:08	DT	Data Type	RW	0
07	-	Reserved	-	-
06:04	PTBM	Pixel To Byte Mapping 001:Eight bits per pixel format 010:Twelve bits per pixel format 011:Sixteen bits per pixel format 100:Eighteen bits per pixel format 101:Twenty-four bits per pixel format Others:Reserved	RW	0x3
03:02	-	Reserved	-	-
01	CCM	Command Continuous Mode (only in Pixel data from DE) 0:single Command Mode 0x1:Continuous Command Mode	RW	0
00	ST	Start a Packet transmission: Write a 1 to start a transmission action. when CCM==1, software should write 0 to stop Packet transmission; When CCM==0, hardware will clear this bit to 0 after Packet transmission.	RW	0

Note:When starting a short packet transmission, the data to be transmitted is from SP_DAT Reg. When starting a long packet transmission, the data to be transmitted is from DMA or from DE.
When in CMD Mode, only one packet per transmission is support.
When reading back data (Use LPDT), the host controller shall judge what type of packet the current transferring packet is. If the read-back packet is Acknowledge and Error Report, store the read-back data in ERR_REP (error report) register. If the read-back packet is other type, store the data in DSI_FIFO_DAT.

18.5.17 DSI_PACK_HEADER

DSI Packet Header Register
Offset=0x44

Bits	Name	Description	Access	Reset
31:16	NULL_PACKET_PH	The Null Packet Header of Transmit packet.	RW	0

		Note:active when Null_Packet_PH>0 and transmit after RGB Packet. [7:0] = Data0 (Word Count lower byte for long packet) [15:8] = Data1 (Word Count upper byte for long packet)		
15:00	PH	The Packet Header of Transmit packet. [7:0] = Data0 (Word Count lower byte for long packet) [15:8] = Data1 (Word Count upper byte for long packet)	RW	0

Note:This register defines the packet header to DSI packets.

18.5.18 DSI_TX_TRIGGER

DSI TX Trigger Register
Offset=0x48

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:08	TRIGGER	Entry Command Pattern	RW	0
07:01	-	Reserved	-	-
00	ST	Start a trigger transmit 0:do not operate 1:Start a trigger	RW	0

Note:This register is used to send trigger.

18.5.19 DSI_RX_TRIGGER

DSI RX Trigger Register
Offset=0x4C

Bits	Name	Description	Access	Reset
31:08	-	Reserved	-	-
07:00	TRIGGER	Entry Command Pattern	R	0

Note:This register stored the received trigger.
Only when a new trigger is received, the register is update. CPU can also write value to the register.

18.5.20 DSI_LANE_CTRL

DSI Lane Control Register
Offset=0x50

Bits	Name	Description	Access	Reset
31:07	-	Reserved	-	-
06	CLK_ULPS	Force Clock Lane Module to enter the Ultra-Low Power State. 0:No force; 1:Force *Note:the bit is auto-cleared after 1 AHB_clk.*	RW	0
05	CLK_ULPS_EXIT	Force Clock Lane Module to exit the Ultra-Low Power State. 0:No force; 1:Force *Note:the bit is auto-cleared after 1 AHB_clk.*	RW	0
04	CLK_TXSTOP	Force Clock Lane Module into Transmit mode /	RW	0

		(Generate Stop State) 0:No force; 1:Force *Note:the bit is auto-cleared after 1 AHB_clk.*		
03	DL_ULPS	Force DATA Lane Module to enter the Ultra-Low Power State. 0:No force; 1:Force *Note:the bit is auto-cleared after 1 AHB_clk.*	RW	0
02	DL_ULPS_EXIT	Force DATA Lane Module to exit the Ultra-Low Power State. 0:No force; 1:Force *Note:the bit is auto-cleared after 1 AHB_clk.*	RW	0
01	DL_TXSTOP	Force DATA Lane Module into Transmit mode / (Generate Stop State) 0:No force; 1:Force *Note:the bit is auto-cleared after 1 byte_clk. Whether D-PHY is in TX state or RX state, force TX state to STOP-State and direction go to 0.*	RW	0
00	DL0_BTA	Force Data Lane 0 Module Bus Turn Around (Only for Data Lane 0) 0:No force; 1:Force *Note:the bit is auto-cleared after 1 AHB_clk.*	RW	0

Note:This register is mainly used to control the lane state.
The setting for Data Lane Control is useful for both Data Lane 0 and Data Lane 1, except for DL_RXMODE and DL_BTA. The setting of DL_RXMODE and DL_BTA is useful only for Data Lane 0.

18.5.21 DSI_LANE_STA

DSI Lane State Register
Offset=0x54

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:12	DL_ST	Data Lane is in Stop State 0:Data Lane is not in Stop State 1:Data Lane is in Stop State *Note:Bit 15 for Data Lane 3, Bit 14 for Data Lane 2, Bit 13 for Data Lane 1, Bit 12 for Data Lane 0*	R	x
11:08	DL_ULPS	Data Lane is in Ultra-Low Power State 0:Data Lane is not in Ultra-Low Power State 1:Data Lane is in Ultra-Low Power State *Note:Bit 11 for Data Lane 3, Bit 10 for Data Lane 2, Bit 9 for Data Lane 1, Bit 8 for Data Lane 0*	R	x
07:06	-	Reserved	-	-
05	CLK_ST	Clk Lane is in Stop State 0:Clock Lane is not in Stop State 1:Clock Lane is in Stop State	R	x
04	CLK_ULPS	Clk Lane is in Ultra-Low Power State 0:Clock Lane is not in Ultra-Low Power State 1:Clock Lane is in Ultra-Low Power State	R	x
03:01	-	Reserved	-	-
00	DIR	Transmit/Receive Direction (Data Lane 0 Only) 0:The Lane is in transmitting mode. 1:The Lane is in receiving mode.	R	x

Note:This register reflects the status of the lane module.

18.5.22 DSI_PHY_T0

DSI PHY Operation Timing0 – For Clock Lane
Offset=0x60

Bit(s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13:11	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst. 000:2 * DSI_Clk 001:4 * DSI_Clk 010:6 * DSI_Clk 011:8 * DSI_Clk 100:12 * DSI_Clk 101:16 * DSI_Clk 110-111:Reserve	RW	0x3
10:08	$T_{CLK-POST}$	Timing that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode. 000:8 * DSI_Clk 001:12 * DSI_Clk 010:16 * DSI_Clk 011:20 * DSI_Clk 100:24 * DSI_Clk 101:28 * DSI_Clk 110:32 * DSI_Clk 111:36 * DSI_Clk	RW	0x3
07:06	$T_{CLK-PRE}$	Timing that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode. 00:1 * DSI_Clk 01:2 * DSI_Clk 10:3 * DSI_Clk 11:4 * DSI_Clk	RW	0x2
05:03	$T_{CLK-ZERO}$	Time for lead HS-0 drive period before starting Clock. 000:2 * DSI_Clk 001:4 * DSI_Clk 010:8 * DSI_Clk 011:16 * DSI_Clk 100:32 * DSI_Clk 101:64 * DSI_Clk 110:96 * DSI_Clk 111:128 * DSI_Clk	RW	0x3
02:00	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission 000:1 * DSI_Clk 001:2 * DSI_Clk 010:4 * DSI_Clk 011:8 * DSI_Clk 100:12 * DSI_Clk 101:16 * DSI_Clk 110-111:Reserved	RW	0x3

18.5.23 DSI_PHY_T1

D-PHY TX Operation Timing1 – For Data Lane
Offset=0x64

Bit(s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13:11	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst. 000:2 * DSI_Clk 001:4 * DSI_Clk 010:8 * DSI_Clk 011:16 * DSI_Clk 100:24 * DSI_Clk 101:32 * DSI_Clk 110:48 * DSI_Clk 111:64 * DSI_Clk	RW	0x3
10:08	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst. 000:2 * DSI_Clk 001:4 * DSI_Clk 010:6 * DSI_Clk 011:8 * DSI_Clk 100:12 * DSI_Clk 101:16 * DSI_Clk 110:20* DSI_Clk 110-111:Reserved	RW	0x3
07:06	-	Reserved	-	-
05:03	$T_{HS-ZERO}$	Time to drive HS-0 before the Sync sequence 000:2 * DSI_Clk 001:4 * DSI_Clk 010:8 * DSI_Clk 011:16 * DSI_Clk 100:24 * DSI_Clk 101:32 * DSI_Clk 110:48 * DSI_Clk 111:64 * DSI_Clk	RW	0x3
02:00	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission 000:1 * DSI_Clk 001:2 * DSI_Clk 010:4 * DSI_Clk 011:8 * DSI_Clk 100:12 * DSI_Clk 101:16 * DSI_Clk 110-111:Reserved	RW	0x3

18.5.24 DSI_PHY_T2

D-PHY TX Operation Timing2 – For LPClk
Offset=0x68

Bit(s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	INIT	Time for initial from PHY CAL Done T_{INIT} = (INIT * 256+1)* T_{LPX}	RW	0x10

		Note:The minimum requirement of T_{INT} is 100us, normally sets to 400us ~ 500us.		
15:08	WAKEUP	Time for wake up from ULPS. (Data Lane & Clock Lane) T_{WAKEUP} = (WAKEUP * 256 +1)* T_{LPX}	RW	0x3
07	TA_SURE	Time-out before new TX side starts driving $T_{TA-SURE}$ = (TA_SURE + 1) * T_{LPX}	RW	0
06:00	PRE_SCALAR	Low-Power Clock pre-scalar value T_{LPX} = (PRE_SCALAR + 1) * T_{DSI_Clk} $T_{LP\ CLK}$ = 2 * T_{LPX}	RW	0xF

18.5.25 DSI_PIN_MAP

DSI Function Test Control Register
Offset=0x7C

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:9	DLANE3_MAP	MIPI DSI Lane 3 Mapping: 0x0:Data 0 (both direction); 0x1:Data 1 (normally using tx direction); 0x2:Data 2 (normally using tx direction); 0x3:Data 3 (normally using tx direction); Others:Reserved	RW	0x3
8	-	Reserved	-	-
7:6	DLANE2_MAP	MIPI DSI Lane 2 Mapping: 0x0:Data 0 (both direction); 0x1:Data 1 (normally using tx direction); 0x2:Data 2 (normally using tx direction); 0x3:Data 3 (normally using tx direction); Others:Reserved	RW	0x2
5	-	Reserved	-	-
4:3	DLANE1_MAP	MIPI DSI Lane 1 Mapping: 0x0:Data 0 (both direction); 0x1:Data 1 (normally using tx direction); 0x2:Data 2 (normally using tx direction); 0x3:Data 3 (normally using tx direction); Others:Reserved	RW	0x1
2	-	Reserved	-	-
1:0	DLANE0_MAP	MIPI DSI Lane 0 Mapping: 0x0:Data 0 (both direction); 0x1:Data 1 (normally using tx direction); 0x2:Data 2 (normally using tx direction); 0x3:Data 3 (normally using tx direction); Others:Reserved	RW	0

18.5.26 DSI_PHY_CTRL

DSI PHY Control Register
Offset=0x80

Bits	Name	Description	Access	Reset
31	REGO_PHY_CLKSEL_DONE	1:calculate PHY_CLK phase done	R	0

30:29	REGO_PHY_CLKSEL_CAL	calculate PHY_CLK phase result 00:select PHY_CLK phase0 01:select PHY_CLK phase90 10:select PHY_CLK phase180 11:select PHY_CLK phase270	R	0
28	REG_PHY_CLKSEL_EN	0:Bypass(disable) PHY_CLK auto select circuit 1:enable PHY_CLK auto select circuit	RW	0
27:26	REG_PHY_CLKSEL	when REG_PHY_CLKSEL_EN=0, manual select which PHY_CLK phase sample 32bit HSDATA 00:select PHY_CLK phase0 01:select PHY_CLK phase90 10:select PHY_CLK phase180 11:select PHY_CLK phase270	RW	0
25	DSI_CALEN	Init and CAL the D-PHY Block 0:do not operate 1:CAL the D-PHY *Note:After D-PHY is powered on, software must initial the D-PHY. When D-PHY_INIT goes to low, Analog Phy completes the initialization process. And Digital Phy starts to work after that.*	RW	0
24	DSI_EN	D-PHY Block Enable 0:Disable (D-PHY is powered off) 1:Enable (D-PHY is powered on)	RW	0
23:22	-	Reserved	-	-
21:18	DPDN_SWAP	Direction of DSI datalane3,2,1,0 0:obverse 1:inverse	RW	0
17	CPCN_SWAP	Direction of DSI clklane 0:obverse 1:inverse	RW	0
16	SELECT_DSI_HSCLK	Select DSI_HSCLK/DSI_HSCLK90 phase 0:DSI_HSCLK is 0 degree phase clock, DSI_HSCLK90 is 90 degree phase clock; 1:DSI_HSCLK is 180 degree phase clock, DSI_hsclk90 is 270 degree phase clock;	RW	0
15:11	LANE_EN	Clk lane and four data lane enable signal Order is D3 D2 D1 D0 CK	RW	0
10:9	LP_DRIVER	LP Driver strength select	RW	1
8	OSRS	Lp tx Output slew rate select 0:normal 1:fast slew rate	RW	0
7	SHDS	Select hs data source 0:select inter data source 1:select digital data source	RW	1
6:4	TMDT	Tune DSI clk lane match delay time 000:about 105ps 001:about 105ps 010:about 174ps 011:about 209ps 100:about 243ps 101:about 278ps 110:about 312ps 111:about 347ps	RW	1

3:2	SELECT_ADJUST_CURRENT	Select output node adjust current 00: 8mA, 01:8.8mA, 10:9.6mA, 11:10.4mA	RW	1
1:0	TX_DRIVER	Tune DSI tx driver strength 00:level1 01:level2 10:level3 11:level4	RW	0

18.6 Application Note

Details about DSI, please refer to < *MIPI Alliance Standard for Display Serial Interface*>.

19 HDMI Interface

19.1 Overview

HDMI (High Definition Multimedia Interface) consists of HDMI Video interface and HDMI Audio interface and HDMI Transmitter core. The HDMI Transmitter Core is a full-function, single-link transmitter with high-bandwidth digital content protection (HDCP), which transmits studio-quality video and/or audio to any HDMI/DVI/HDCP-enabled digital receivers. Features of HDMI Interface module is listed below:

- Compatible with HDMI 1.4, HDCP1.1 and DVI 1.0
- Supports most video formats from 640*480i to 1920*1080p, including:
  - 640*480p@59.94/60Hz
  - 720*480p@59.94/60Hz
  - 720*576p@50Hz
  - 1280*720p@59.94/60Hz
  - 1280*720p@50Hz
  - 720(1440)*480i@59.94/60Hz
  - 720(1440)*576i@50Hz
  - 1440*480p@59.94/60Hz
  - 1440*576p@50Hz
  - 1920*1080i@59.94/60Hz
  - 1920*1080i@50Hz
  - 1920*1080p@24Hz
  - 1920*1080p@59.94/60Hz
  - 1920*1080p@50Hz
- Supports 24bit, 30bit, 36bit RGB/YCbCr 4:4:4 format (Deep Color)
- Supports xvYCC601, xvYCC709 Enhanced Colorimetry format
- Supports IEC60958 audio format up to 24bits
- Supports High-bitrate compressed audio formats
- Supports up to 8-channel Audio sample, supports 48/96/192/44.2/88.4/176.8kHz audio sample rate
- Supports Auto-Lipsync Correction feature
- Supports 3D Frame Packing Structure with 1080p@24Hz, 720p@50Hz, 720p@59.94/60Hz, etc.
- Supports 3D Side-by-Side (Half) Structure with 1080i@59.94/60Hz, 1080i@50Hz, etc.
- Supports 3D Top-and-Bottom Structure with 1080p@24Hz, 720p@50Hz, 720p@59.94/60Hz, etc.

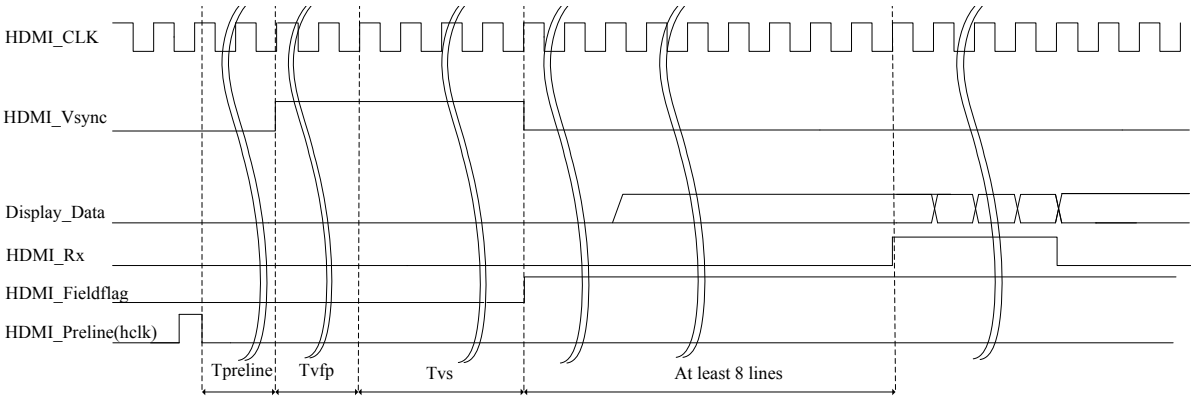
19.2 Function Description

19.2.1 HDMI Video Interface

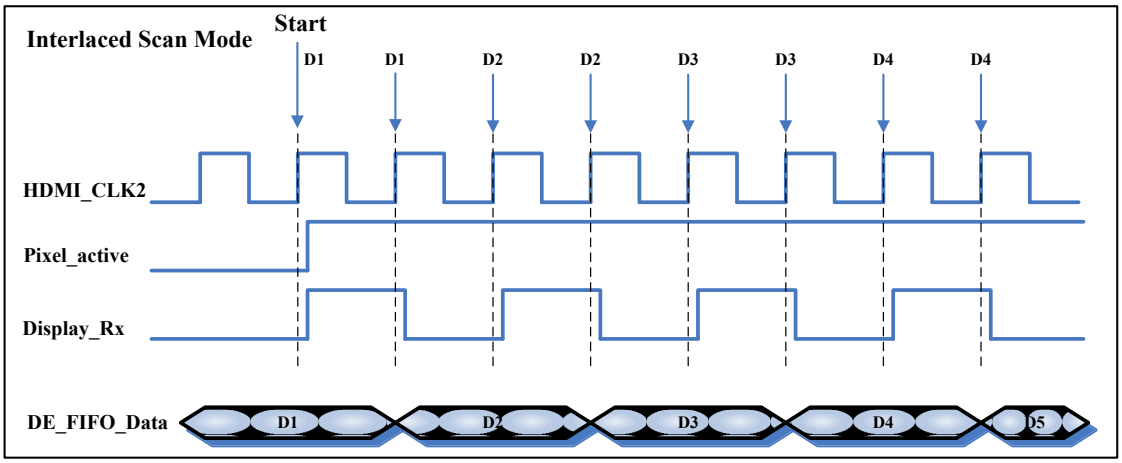
HDMI Video interface is used for transferring video data (such as RGB or YCbCr pixel data coming from DE) into data stream according to HDMI Video timing. Dis_Hsync, dis_Vsync, Pixel_Active and Line_Active signals are produced for controlling the HDMI output timing. HDMI_Vsync, HDMI_rx, HDMI_FieldFlag, HDMI_left_flag and HDMI_preline signals are produced for handshaking with DE. How to produce those signals is according to the video format that defined in the registers mentioned before.

HDMI_Vsync signal starts from the falling edge of Line_active, and ends by register settings which ensure at least 8 lines from the next Line_active rising edge.

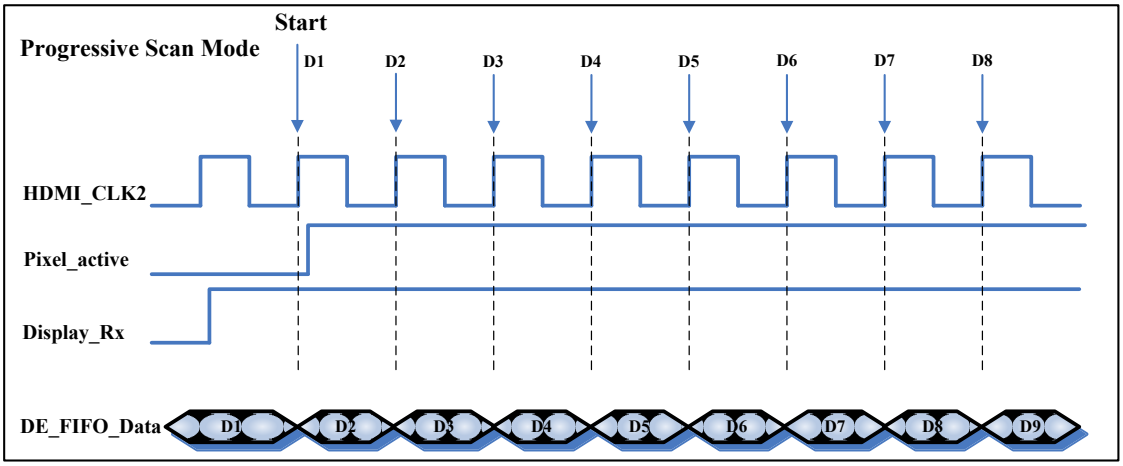
HDMI_preline signal active before HDMI_Vsync, and interval lines are setting by register.



(a) HDMI Timing



(b) Pdiv2 Mode



(c) Interlaced or Progressive Scan Mode

Figure 19-1 Handshake timing between HDMI and DE Module

Note:

(1) Vsync and Display_Rx signals must be with active high polarity supporting to DE for handshake. So, in the Video Interface, active high signals of Hsync, Vsync are made only working with DE. However, Hsync and Vsync signals that send to HDMI Transmitter Core are according to the polarity setting bits of HDMI_SCHCR Register.

(2) For 720x480i and 720x576i, we must set to both Interlaced and Pdiv2 mode, and for 1080i, only set to interlaced mode.

(3) DISPLAY_Preline is a signal for DE, which must be active before the end of one frame; its position can be set by Tpreline, from 1 to 16. Especially for HDMI Frame 3D, one frame must be the whole 3D frame which includes left eye and right eye information.

19.2.2 HDMI Audio Interface

HDMI Audio interface is used for transferring Audio Samples into data stream according to HDMI Audio timing. Audio Interface supports up to 8 channels, 24bits audio input.

Audio Interface timing in HDMI is showed in Figure below. Ch_wen signal is used to control when audio data send. Sample_en signal is used to indicate one audio sample ends and next one starts. Frame_en signal is used to indicate one audio frame ends and next one starts (one audio frame includes 192 audio samples).

Each audio sample just indicated one bit of channel status information, that displayed by ch_status signal. Total 192bits channel status is described by the registers from HDMI_AICHSTAByte0to3 to HDMI_AICHSTAByte20to23 and HDMI_AICHSTASCN.

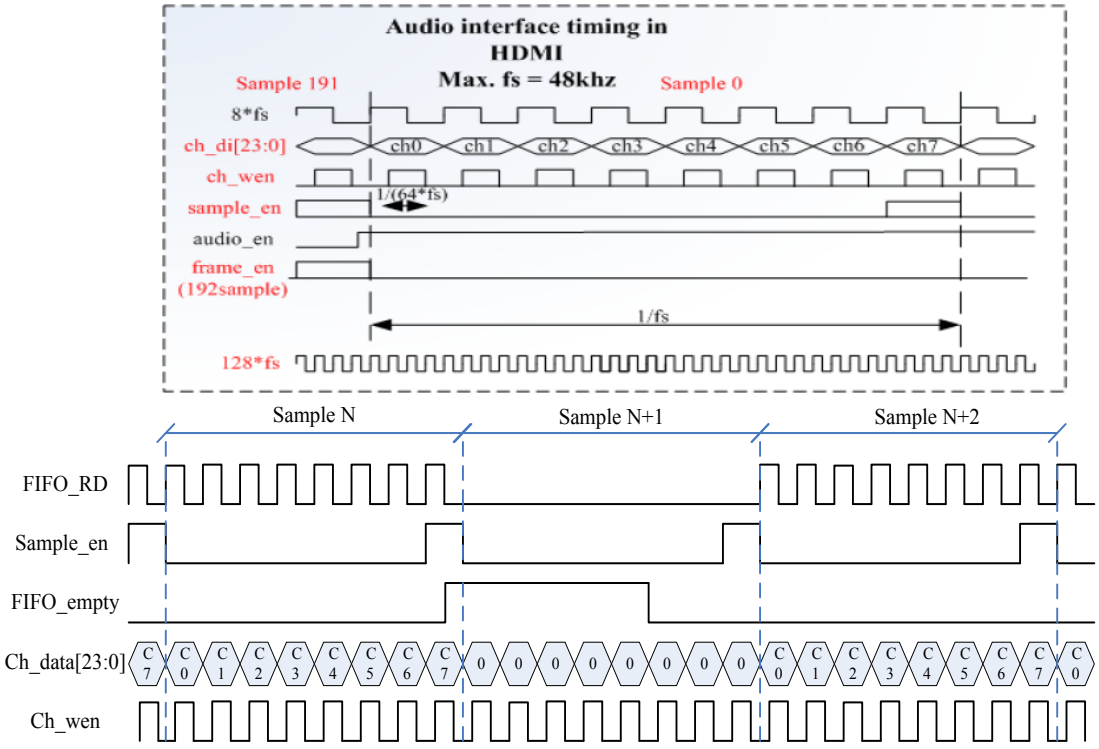


Figure 19-2 Audio Interface Timing

Note:

1) *Active (high) period of ch_wen signal is about 1/(64fs). Ch_wen signal should be worked with the audio channel mask bits that described in the HDMI_ASPCR Register to produce FIFO_RD signal that read Audio data from DAC FIFO.*
2) *Each channel has its own 192bit channel status. However, most bits are same that defined in HDMI_AICHSTAByte**to** registers, besides few is different that defined in HDMI_AICHSTASCN register.*
3) *The function of auto transfer all zero audio sample packets has been added when DAC FIFO_empty signal been set. At this time, FIFO_RD signal would be cleared and audio sample data that written into internal audio FIFO would be set to zero. To insure the right audio channel order, FIFO_RD signal will be active again only after both the FIFO_empty signal cleared and the next sample_en signal active.*

19.3 Application Note

20 HDCP2 Tx

20.1 Overview

A HDCP Transmitter (Tx) and Receiver (Rx) pair performs authentication before it transfers AV data. Authentication involves a series of control messages to be exchanged among transmitter and receiver. After receiver is authentic and a secret key that will be used for encrypting AV data, Encrypted datum begin to transfer between a HDCP pair.

Hardware and Software together play a role in authentication process. Software detects receiver when it is connected and directs the Hardware to start authentication. Hardware generates control message and associated data for authentication, writes the data to registers and inform Software to let it transfer messages to receiver. Control messages received from the other end are written to register set by Software thereby Hardware reads and performs authentication checks.

When successfully finishing authentication, Software started PES payload Encryption after setting raw and encryption datum information, then Hardware would auto got plaintext datum from InputRFIFO, encrypted 128-bit block of payload, put encrypted 128-bit block into OutputEFIFO. Hardware could output Encrypted datum with format of no TS Packet, Blu-ray TS Packet or MPEG2 TS Packet.

S500 is compliant to HDCP revision 2.1 and 2.0, and features of HDCP2 Tx are listed below:

- Uses industry-standard public-key RSA authentication and AES-128 encryption
- Compliant to HDCP revision 2.1 and 2.0
- Supports repeaters
- Inside Random Number Generator compliant to NIST-SP 800 90
- Inside HMAC-SHA256 block
- Inside Input and Output FIFO for raw and Encryption datum
- Inside TS packet compliant to Blu-ray and MPEG2 format
- Supports PES portion Encryption mode

20.2 Block Diagram

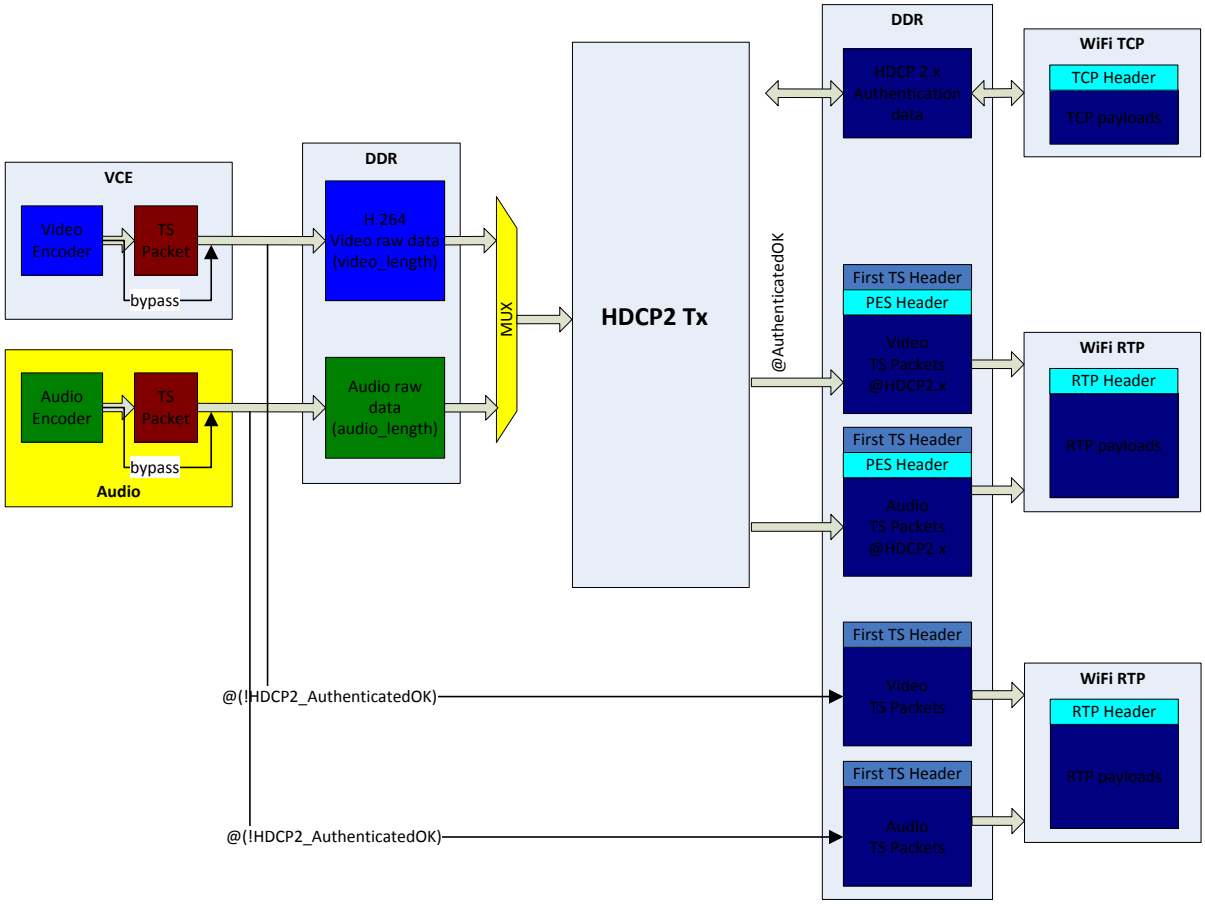


Figure 20-1 HDCP2 Tx General Block Diagram

20.3 Function Description

A HDCP2 Transmitter (Tx) and Receiver (Rx) pair performs authentication before it does AV data transfer. Authentication involves AKE, Pairing, Locality Check, SKE, and authentication with Repeater.

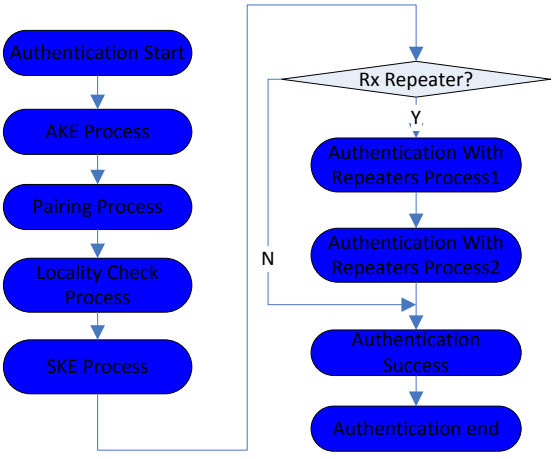


Figure 20-2 HDCP2 Tx Authentication Process

Detailed information on HDCP2, please refer to document: *<High-bandwidth Digital Content Protection System>*.

20.4 Register List

Table 20-1 HDCP2 Tx Registers Address

Name	Physical Base Address
HDCP2TX_REGISTER	0xB0250000

20.5 Application Note

Detailed information on HDCP2, please refer to document: <*High-bandwidth Digital Content Protection System*>.

21 TVOUT

21.1 Overview

TVOUT is interface of TV display, it support digital interface of CVBS and BT.656. It integrated a 12-bit high speed ADC for analog to digital signal transforming. Features of TVOUT are listed below.

- Support NTSC and PAL format for CVBS output
- Support Standard 8bit BT.656 Output for 625-line and 525-line
- Four 12-bit video DAC outputs sample rate up to 300MHz

21.2 Block Diagram

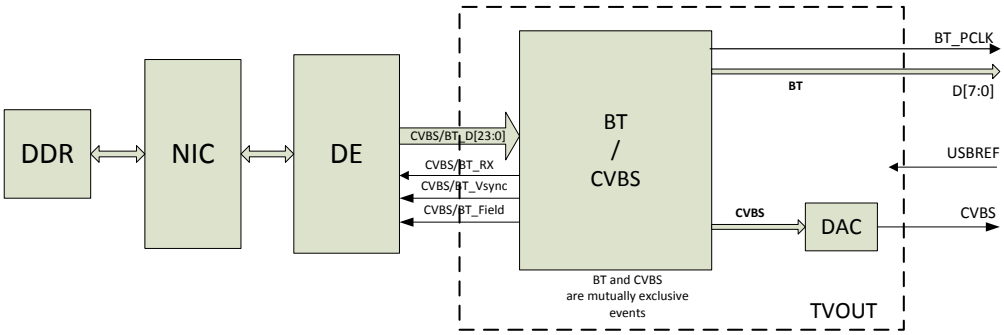


Figure 21-1 TVOUT System Diagram

21.3 Function Description

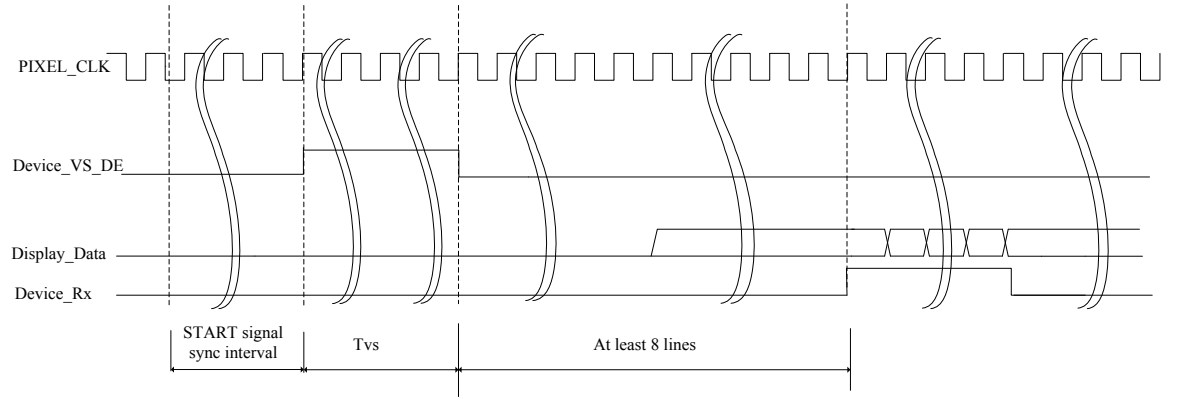
21.3.1 DE and TVOUT Interface Timing

CVBS and BT are sharing one interface to interactive with DE. The clock is from CMU, and the data format is 24-bit YCbCr.

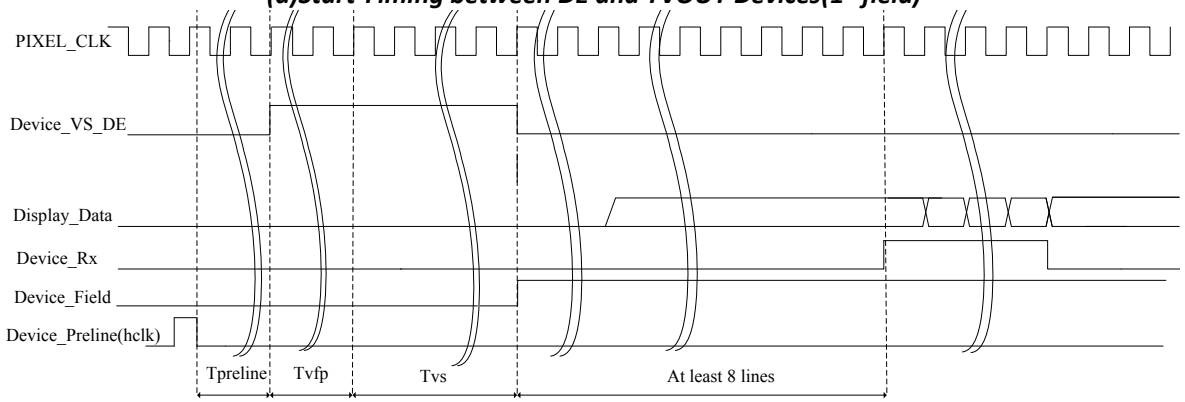
VS_DE signal is sent by display device, the rising edge representing the former valid line is terminated, i.e. field/frame blanking interval started. The falling edge indicates new field/frame is to coming, reminding DE to prepare data. The period from Vsync falling edge to the valid data start should be at lease 8 lines.

Device_Rx signal is the Display device requesting data from DE.

Device_Field signal is the signal of interlaced equipment, used to indicate the present field of odd or even field for DE. When field is odd field, the signal is low level; when field is even field, the signal is high level. The toggle edge is aligned with Vsync falling edge.



(a)Start Timing between DE and TVOUT Devices(1st field)



(b)Timing between DE and TVOUT Device(2nd field and afterwards)

Figure 21-2 Handshake Timing between DE and TVOUT Devices

Format of 24-bit YUV data sent from DE to TVOUT module is shown in the figure below:

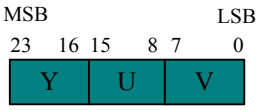


Figure 21-3 DE data format

21.4 Register List

Table 21-1 TVOUT Controller Registers Address

Name	Physical Base Address
TVOUT	0xB02B0000

Table 21-2 TVOUT Controller Registers

Offset	Register Name	Description
0x0000	TVOUT_EN	TVOUT Enable Register
0x0004	TVOUT_OCR	TVOUT Output Control Register
0x0008	TVOUT_STA	TVOUT STATUS Register
0x000C	TVOUT_CCR	TVOUT Output Contrast Control Register
0x0010	TVOUT_BCR	TVOUT Output Brightness Control Register
0x0014	TVOUT_CSCR	TVOUT Output Color Saturation Control Register
0x0018	TVOUT_PRL	TVOUT Preline Number Set Register
0x001C	TVOUT_VFALD	TVOUT Vsync(for DE) Falling-edge to Active Line Distance Set Register
0x0020	CVBS_MSR	CVBS Output Mode Select Register
0x0024	CVBS_AL_SEPO	CVBS Output Active Line Start and End Position (Odd Field)

		Register
0x0028	CVBS_AL_SEPE	CVBS Output Active Line Start and End Position (Even Field) Register
0x002C	CVBS_AD_SEP	CVBS Output Active Data In Every Line Start and End Position Register
0x0030	CVBS_HUECR	CVBS Output Hue Control Register
0x0034	CVBS_SCPCR	CVBS Output Sub-Carrier Phase Control Register
0x0038	CVBS_SCFCR	CVBS Output Sub-Carrier Frequency Control Register
0x003C	CVBS_CBACR	CVBS Output Color Burst Amplitude Control Register
0x0040	CVBS_SACR	CVBS Output Sync Amplitude Control Register
0x0100	BT_MSR0	BT Mode Select Register0
0x0104	BT_MSR1	BT Mode Select Register1
0x0108	BT_AL_SEPO	BT Active Line Start and End Position (Odd Field or ISP) Register
0x010C	BT_AL_SEPE	BT Active Line Start and End Position (Even Field) Register
0x0110	BT_AP_SEP	BT Active Pixels In Every Line Start and End Position Register

21.5 Register Description

21.5.1 TVOUT_EN

TVOUT Enable Register
Offset = 0x00

Bit(s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	CVBS_EN	CVBS Output Enable 0: Disable 1: Enable	RW	0

21.5.2 TVOUT_OCR

TVOUT Output Control Register
Offset = 0x04

Bit(s)	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:24	INRSET	HDAC Internal 75ohm Set 01111: 75 ohm Only active when Internal 75ohm Setup is selected	RW	0F
23	INCALSET	HDAC Internal 75ohm Set Selection: 0: 75ohm Auto Calibration 1: 75ohm Setup	RW	0
22:13	-	Reserved	-	-
12	PI_IRQEN	HDAC PlugIn Line IRQ Enable. 0: Disable 1: Enable	RW	0
11	PO_IRQEN	HDAC PlugOut Line IRQ Enable. 0: Disable 1: Enable	RW	0

10	CVINACEN	CVBS Internal 75ohm Auto Calibration Enable 0: Disable 1: Enable Only active when Internal 75ohm is enable.	RW	0
9	CVPO_ADEN	CVBS PlugOut Line Auto Detect Enable 0: Disable 1: Enable	RW	0
8	CVPI_ADEN	CVBS PlugIn Line Auto Detect Enable 0: Disable 1: Enable Only active when using internal 75ohm in circuit.	RW	0
7	CVINREN	CVBS Internal 75ohm Enable 0: Disable 1: Enable	RW	0
6:5	-	Reserved	-	-
4	DACOUT	HDAC Output Color Bar Enable. 0: Disable 1: Enable	RW	0
3	DAC3	HDAC_CVBS enable 0: Disable 1: Enable	RW	0
2:0	-	Reserved	-	-

21.5.3 TVOUT_STA

TVOUT Status Register
Offset = 0x08

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	DAC3DLS	HDAC_CVBS PlugOut Pending. 0: No Line PlugOut 1: TV Line PlugOut	RW	0x0
6:4	-	Reserved	-	-
3	DAC3ILS	HDAC_CVBS PlugIn Pending. 0: No Line PlugIn 1: TV Line PlugIn	RW	0x0
2:0	-	Reserved	-	-

21.5.4 TVOUT_CCR

TVOUT Output Contrast Control Register
Offset = 0x0C

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	COTCTL	Contrast control. 0000: 75% ... 0111: 100% ... 1110: 125% 1111: Reserve	RW	0x7

Note:

1. *Contrast Control Register[3:0]=(X-0.75)×28; X is 75% to 125%.*

21.5.5 TVOUT_BCR

TVOUT Output Brightness Control Register
Offset = 0x10

Bit(s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	BRGCTL	Brightness control. 0x000:-512LSB … 0x1FF:1LSB 0x200:0LSB 0x201:1LSB … 0x3FF:511LSB	RW	0x200

Note:

1. *The MSB of Brightness Control Register[9:0] is sign bit. The unit is LSB of DAC. The value is calculated with 2-complement.*

21.5.6 TVOUT_CSCR

TVOUT Output Color Saturation Control Register
Offset = 0x14

Bit(s)	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5:0	CSATCTL	Color Saturation control. 000000:50% … 000111:100% … 111111:150%	RW	0x7

Note:

1. *Color Saturation Control Register[3:0]=(X-0.5)×14, X<100%; =(X-1) ×112+7, X>100%*

21.5.7 TVOUT_PRL

TVOUT Preline Number Set Register
Offset = 0x18

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:8	CPN	CVBS Preline Number Set 0000: 1 line 0001: 2 lines … 1110: 15 lines 1111: 16 lines	RW	0xF
7:0	-	Reserved	-	-

Note:

1. *The register is used to set Preline Number.*

21.5.8 TVOUT_VFALD

TVOUT Vsync(for DE) Falling-edge to Active Line Distance Set Register
Offset = 0x1C

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:8	CVAD	CVBS Vsync Falling-edge to Active Line Distance 0000~0111: Reserved 1000: 8 lines 1001: 9 lines … 1110: 14 lines 1111: 15 lines	RW	0x8
7:0	-	Reserved	-	-

21.5.9 CVBS_MSR

CVBS Output Mode Select Register
Offset = 0x20

Bit(s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	SCEN	CVBS output 108M sample clk for DAC Enable 0: Disable 1: Enable	RW	0x0
5	APNS	Active pixel number Mode Select 0: 714 Pixel---BT.470 standard 1: 720 Pixel---BT.656 standard	RW	0x0
4	CVCKS	CVBS Clock mode Select 0: 27MHzPLL+24MHz 1: 27MHzPLL	RW	0x0
3:0	CVBS	CVBS TV system Select. 0000: NTSC-M 0001: NTSC-J 0010: PAL-Nc 0011: PAL-B,G,H 0100: PAL-D 0101: PAL-I 0110: PAL-M 0111: PAL-N Others: Reserved	RW	0x4

Note:

1. CVBS output to TV system parameters is listed below:

TV System	*Line Rate (Line/Frame)*	*Frame Rate (per second)*	*Fsc (MHz)*	*Y Channel 3dB Bandwidth (MHz)*	*Difference between Black and Blanking level (IRE)*
NTSC-M	*525*	*29.97*	*3.579545*	*4.2*	*7.5*
NTSC-J	*525*	*29.97*	*3.579545*	*4.2*	*0*
PAL-Nc	*625*	*25*	*3.582056*	*4.2*	*0*
PAL-B,G,H	*625*	*25*	*4.43361875*	*5.0*	*0*
PAL-D	*625*	*25*	*4.43361875*	*6.0*	*0*
PAL-I	*625*	*25*	*4.43361875*	*5.5*	*0*

PAL-M	*525*	*29.97*	*3.575611*	*4.2*	*7.5*
PAL-N	*625*	*25*	*4.43361875*	*4.2*	*7.5*

21.5.10 CVBS_AL_SEPO

CVBS Output Active Line Start and End Position Register(Odd Field)
Offset = 0x24

Bit(s)	Name	Description	Access	Reset
31:26	-	Reserved	-	-
25:16	ALEP	Active Line End Position in odd field or one frame	RW	0x0
15:10	-	Reserved	-	-
9:0	ALSP	Active Line Start Position in odd field or one frame	RW	0x0

21.5.11 CVBS_AL_SEPE

CVBS Output Active Line Start and End Position Register(Even Field)
Offset = 0x28

Bit(s)	Name	Description	Access	Reset
31:26	-	Reserved	-	-
25:16	ALEPEF	Active Line End Position in Even field	RW	0x0
15:10	-	Reserved	-	-
9:0	ALSPEF	Active Line Start Position in Even field	RW	0x0

21.5.12 CVBS_AD_SEP

CVBS Output Active Data In Every Line Start and End Position Register
Address = 0x2C

Bit(s)	Name	Description	Access	Reset
31:26	-	Reserved	-	-
25:16	ADEP	Active Data End Position in each line(in pixel)	RW	0x0
15:10	-	Reserved	-	-
9:0	ADSP	Active Data Start Position in each line(in pixel)	RW	0x0

21.5.13 CVBS_HUECR

CVBS Output HUE Control Register
Offset=0x30

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	HUECTL	The HUE control. 00H: -22.5 Degree … 80H: 0 Degree … FFH: 22.32421875 Degree	RW	0x80

Note:
The HUE Control Register[7:0]=X/0.17578125+128; Xis -22.5 to 22.32421875.

21.5.14 CVBS_SCPCR

CVBS Output Sub-Carrier Phase Control Register
Offset = 0x34

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	SCPC	The Phase of Sub-Carrier Phase Compensate. 00H: 0 Degree … FFFH: 359.912 Degree	RW	0x0

Note:
The register value of the phase of sub-carrier phase compensate is X×4096/360. X is the wanted phase of color burst phase compensate

21.5.15 CVBS_SCFCR

CVBS Output Sub-Carrier Frequency Control Register
Offset=0x38

Bit(s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8:0	SCFCR	Sub-Carrier Frequency Control. 000H: -1280ppm … 0FFH: -5ppm 100H: 0ppm 101H: 5ppm … 1FFH: 1275ppm	RW	0x100

Note: 1.Step is 5ppm.

21.5.16 CVBS_CBACR

CVBS Output Color Burst Amplitude Control Register
Offset = 0x3C

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	CBURAM	CBUR Amplitude Level 0000: 30% … 0111: 100% … 1111: 180%	RW	0x7

Note:
The register is used to adjust the amplitude of color burst. 100% means the real amplitude level of color burst when connect with different TV. Every step change ±10%.

21.5.17 CVBS_SACR

CVBS Output Sync Amplitude Control Register
Offset = 0x40

Bit(s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	SYNCAM	SYNC Pedestal Level Amplitude. 00H: 0LSB … 7FH: 127LSB	RW	0x0

21.5.18 BT_MSR0

BT Mode Select Register0
Offset = 0x100

Bit(s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	BTEN	BT IF Enable 0: Disable 1: Enable	RW	0x0

21.5.19 BT_MSR1

BT Mode Select Register1
Offset = 0x104

Bit(s)	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	PAES	Pclk Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	RW	0x0
1	PNMS	PAL/NTSC Mode Select 0: PAL --625 line, 50 field/s 1: NTSC--525 line, 59.94 field/s	RW	0x0
0	-	Reserved	-	-

21.5.20 BT_AL_SEPO

BT Active Line Start and End Position (Odd Field) Register
Offset = 0x108

Bit(s)	Name	Description	Access	Reset
31:25	-	Reserved	-	-
24:16	LEPO	Active Line End Position in Odd field	RW	0x0
15:8	-	Reserved	-	-
7:0	LSPO	Active Line Start Position in Odd field	RW	0x0

Note:

1. *Active line start position must be counted from the 1st line.*

21.5.21 BT_AL_SEPE

BT Active Line Start and End Position (Even Field) Register
Offset = 0x10C

Bit(s)	Name	Description	Access	Reset
31:26	-	Reserved	-	-

25:16	LEPE	Active Line End Position in Even field	RW	0x0
15:10	-	Reserved	-	-
9:0	LSPE	Active Line Start Position in Even field	RW	0x0

Note:

1. Active line start position must be counted from the 1st line

21.5.22 BT_AP_SEP

BT Active Pixels In Every Line Start and End Position Register
Address = 0x110

Bit(s)	Name	Description	Access	Reset
31:26	-	Reserved	-	-
25:16	ADEP	Active Data Pixels End Position in each line	RW	0x0
15:10	-	Reserved	-	-
9:0	ADSP	Active Data Pixels Start Position in each line	RW	0x0

Note: *Active Pixels start position must be counter from EAV, Max value is 720 Pixels, Min Value is 0. The value of (ADEP-ADSP) must be even number.*

21.6 Application Note

22 USB3

USB3 interface support host function that compliant with USB 2.0 Specification. Features of USB3 port is listed below.

- Host and Device mode is supported
- Fully compliant with USB Specification 2.0
- Device mode Supports High Speed (480Mb/s) and Full Speed (12Mb/s)
- Host mode Supports High Speed, Full Speed and Low Speed
- Supports Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Interface UTMI+(level3)
- Up to 31 devices are supports by the Host
- Supports USB remote wake-up feature
- Host mode is compliant with XHCI architecture
- Downstream hub function is supported

23 USB2

23.1 Overview

There are two USB2 interfaces both support OTG functionality, and one of which support USB HSIC (Hi-Speed Inter-Chip) standard. HSIC is the low power edition of USB 2.0 standard, which reduce the PHY size and power consumption. Features of USB2 HSIC interface is listed below:

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- HSIC Interface for an option.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) with USB2.0.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (one series downstream HUB supported).
- Supports full-speed or high-speed in peripheral mode.
- Supports 15 IN endpoints and 15 OUT endpoints besides Control endpoint0.
- Supports high-speed high-bandwidth Isochronous transfer and Interrupt transfer.
- Integrated 15KB single port RAM as IN, OUT endpoint buffer. Partially configurable endpoint buffer size, endpoint type with single, double, triple or quad buffering.
- Supports suspend, resume and power managements function.
- Support remote wakeup.
- An optional HSIC interface for USBH1 controller.
- One OTG function and the other working as either Device or Host
- 32 bit AHB bus interface to uP for debug use
- Master access to DDR with 32bit UDMA bus

23.2 Block Diagram

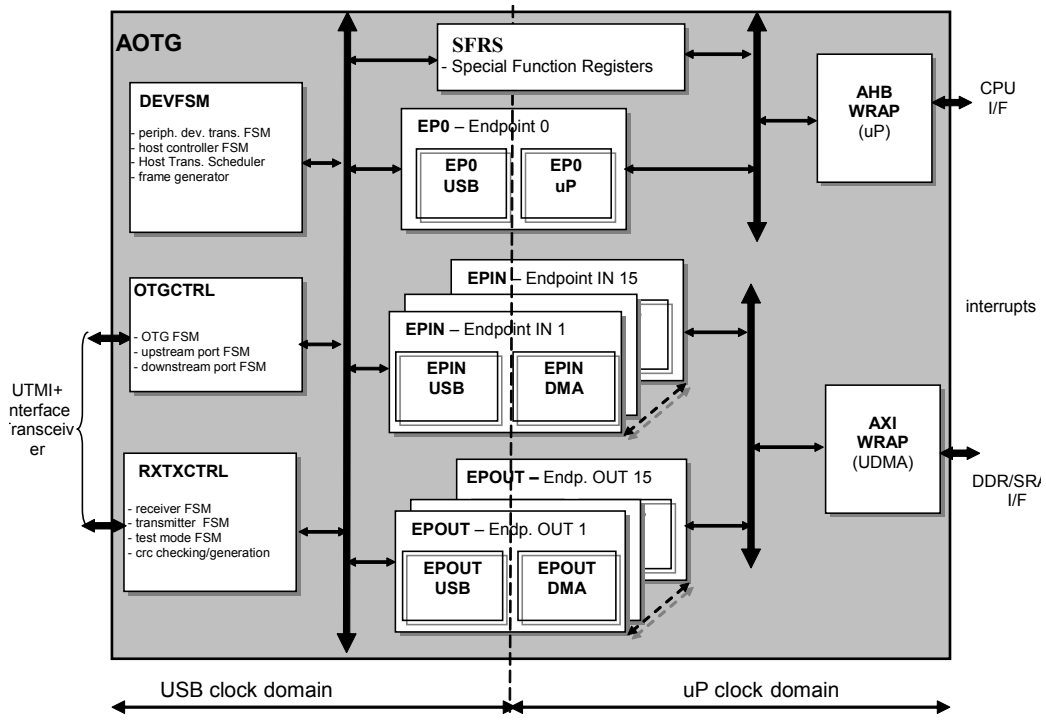


Figure 23-1 AOTG Controller block diagram

23.3 Function Description

The Actions OTG (AOTG) controller is designed to support all tasks specified in the OTG Supplement. Either AOTG module is composed of AOTG controller and UTMI+ transceiver. AOTG supports hardware implementation of the Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). Special Function Registers are provided to control the HNP and SRP.

Either AOTG can be used as a dual-role device and can act as a USB host or a USB peripheral device. Each of the ID input pins controls the default role of the relative controller. If the ID=1, it means that the mini-B plug is connected and the AOTG becomes a B-device. When the ID=0 it means that a mini-A plug is connected and the AOTG becomes an A-device.

For details, see *<On-The-Go Supplement to the USB2.0 Specification Rev. 1.0a>*.

23.4 Application Note

For details, see *<On-The-Go Supplement to the USB2.0 Specification Rev. 1.0a>*.

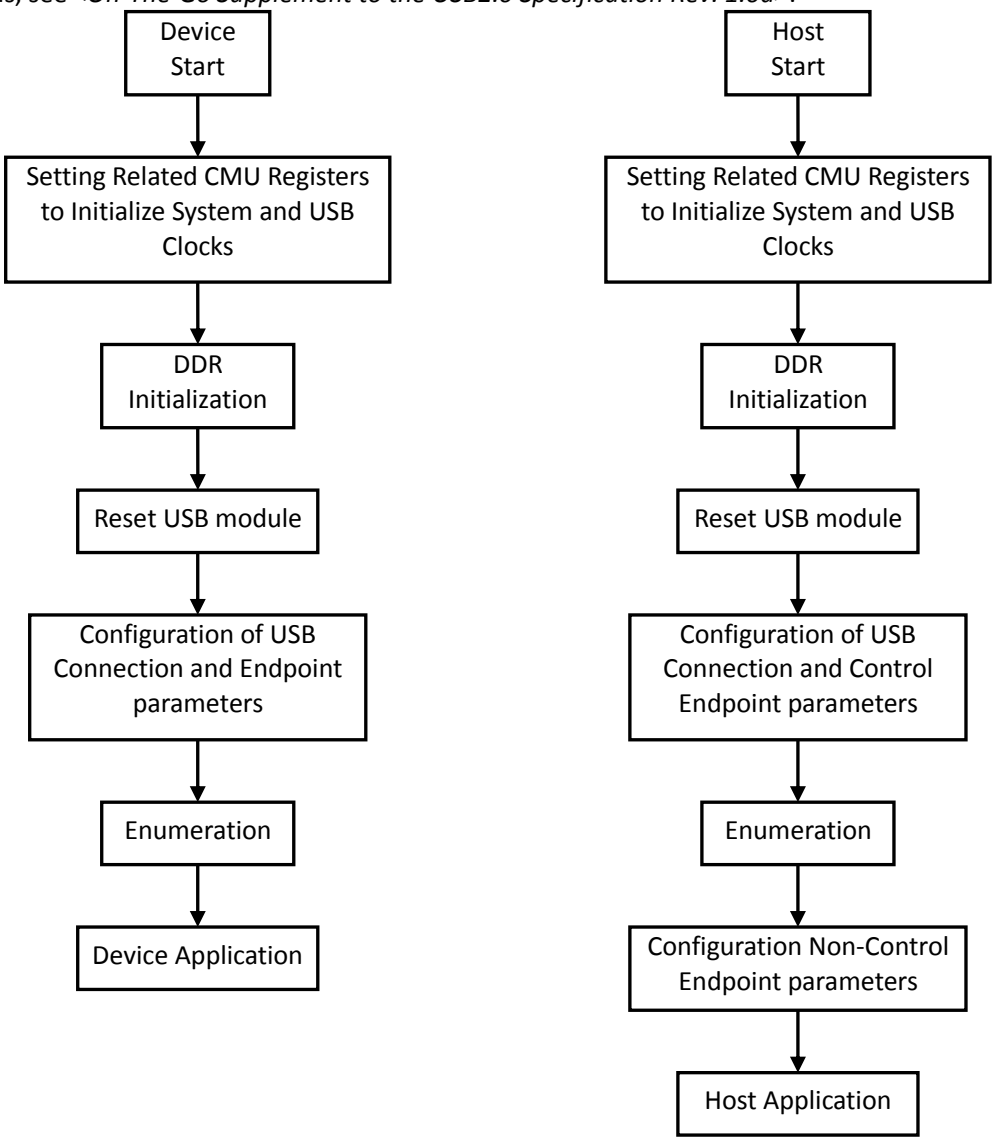


Fig 12 Software Control Procedure

Details about USB2.0 please refer to documents on *Universal Serial Bus 2.0 Specification*.

24 Audio In/Out Interface

24.1 Overview

I2S and SPDIF interface are supported by S500 for audio IN/OUT. I2S is also known as Inter-IC Sound, it is and electrical serial bus interface for digital audio signals, used to communicate PCM audio data between IC and devices. SPDIF is a transmitter interface for digital audio devices, data transmitted is also PCM encoded audio signals. Features of Audio interface are listed below:

- Support I2S, SPDIF, HDMI audio transmiting simultaneously.
- Support mix voice from I2S receiver with HDMI audio, SPDIF, I2S transmitter directly in digital domain for karaoke.

I2S

- Supports 2.0-channel I2S transmitter and receiver
- Supports 7.1-channel and 5.1-channel through I2S transmitter with ext.8-channel and 6-channel DAC or with ATC260X, by TDM (time-division multiplexed) Mode.
- Supports 4-channel through I2S receiver with ATC260X, by TDM Mode for 4-channel record.
- Support stereo DMIC in ATC260X, and data received by I2S receiver of S500.
- I2S can only work as Master Mode.
- I2S supports sample rate 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/176.4k/44.1k/22.05k/11.025k
- I2S transmitter has 24bit*32level FIFO, and I2S receiver has 24bit*16level FIFO.

SPDIF

- SPDIF supports transmitter mode only.
- SPDIF supports sample rate 96k/48k/44.1k/32k.

24.2 Block Diagram

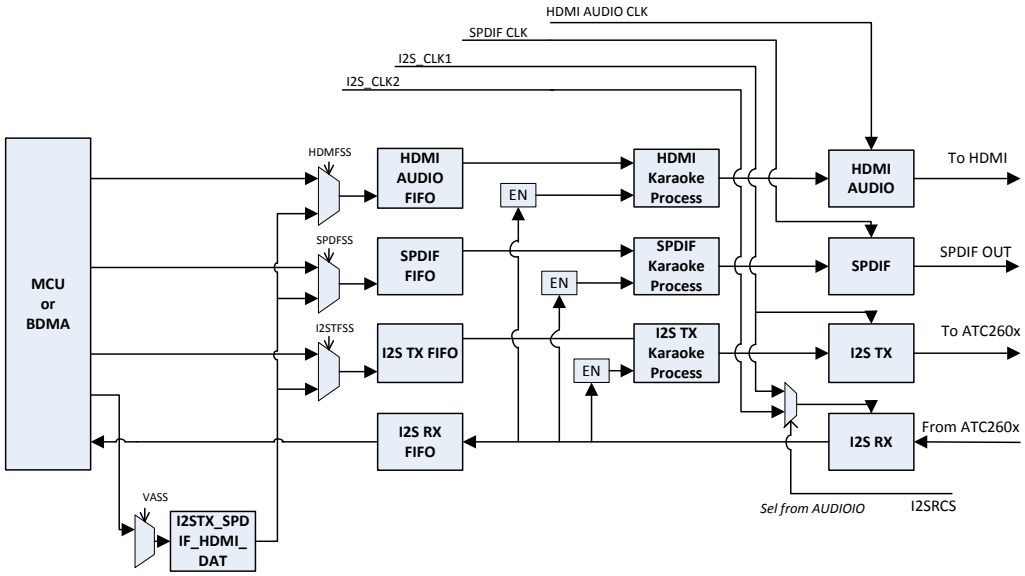


Figure 24-1 Audio In/Out Main Block Diagram

The Audio In/Out Interface support transmiting audio through I2S, SPDIF, HDMI audio interfaces simultaneously. The I2S interface is the communication channel between S500 and Audio Codec of ATC260x.

24.3 Function Description

24.3.1 I2S Interface

I2S mode supports sample rate 192K/96K/88.2K/48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. I2S Module can work as I2S Receiver (I2S RX) and I2S Transmitter (I2S TX), only work as Master Mode. I2S TX Supports 5.1-channel and 7.1-channel with ext.6-channel/8-channel DAC by TDM Mode. It also supports 2.0-Channel Mode. Clock and Data are sent through 4 pins: BCLK, LRCLK, DOUT, MCLK.

TDM Mode A with ext.6-channel/8-channel DAC:
In TDM Mode A, the MSB of channel 1 left data is sampled by outside multi-channel DAC on the second rising edge on BCLK following a LRCLK rising edge. Channel 1 right and channel 2/…/N (here N=3 or 4) data follow channel 1 left data.

In TDM Mode A, it also supports DOUT data sample by outside multi-channel DAC on falling edge of BCLK. The following picture shows data sampled on rising edge of BCLK.

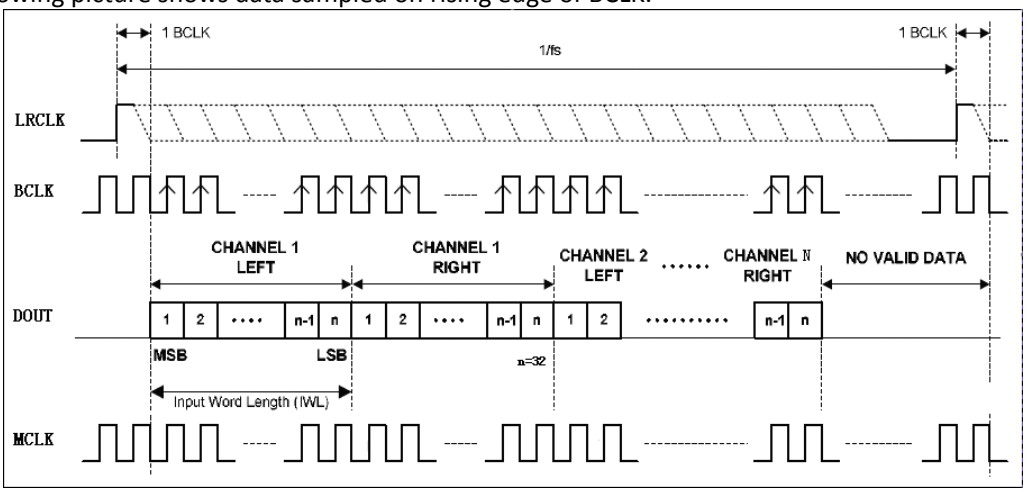


Figure 24-2 TDM Mode A

TDM Mode B with ext.6-channel/8-channel DAC:
In TDM Mode B, the MSB of channel 1 left data is sampled by outside multi-channel DAC on the first rising edge on BCLK following a LRCLK rising edge. Channel 1 right and channel 2/…/N (here N=3 or 4) data follow channel 1 left data.

In TDM Mode B, it also supports DOUT data sample by outside multi-channel DAC on falling edge of BCLK. The following picture shows data sampled on rising edge of BCLK.

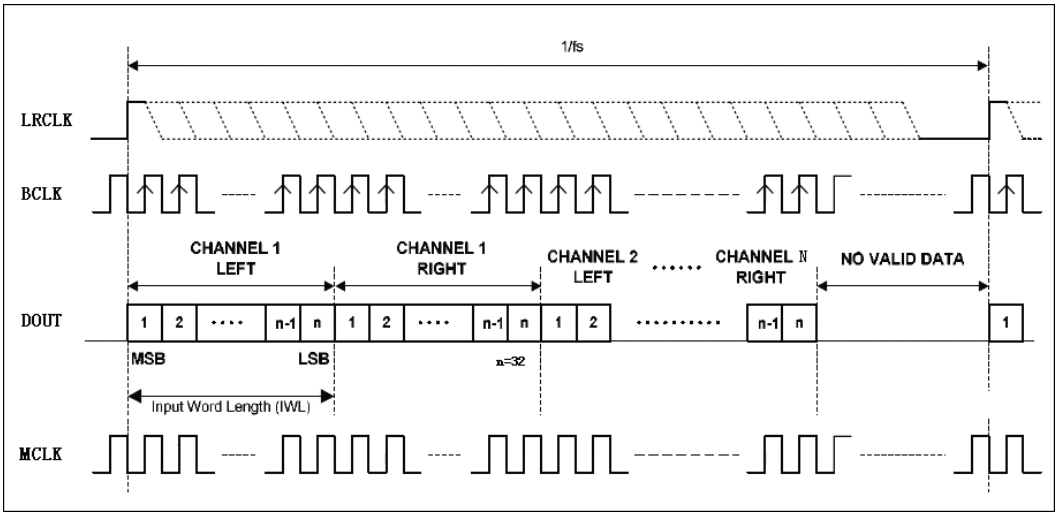


Figure 24-3 TDM Mode B

I2S RX Supports 2.0-channel and 4-channel with ext.multi-channel ADC by TDM Mode. Only supports TDM Mode A/B rising (rising edge samples data). Clock and Data are sent through 4 pins: BCLK, LRCLK, DIN, MCLK.

24.3.2 SPDIF Interface

S/PDIF is used to transmit digital signals of a number of formats, the most common being the 48 kHz sample rate format used in DAT and the 44.1 kHz format used in CD audio. Instead the data is sent using Biphase mark code, which has either one or two transitions for every bit, allowing the original sample clock to be extracted from the signal itself.

S/PDIF is used for transmitting 20 bit audio data streams plus other related information. To transmit sources with less than 20 bits of sample accuracy, the superfluous bits will be set to zero. S/PDIF can also transport 24 bit samples by way of four extra bits, but not all equipment supports this, and might ignore these extra bits.

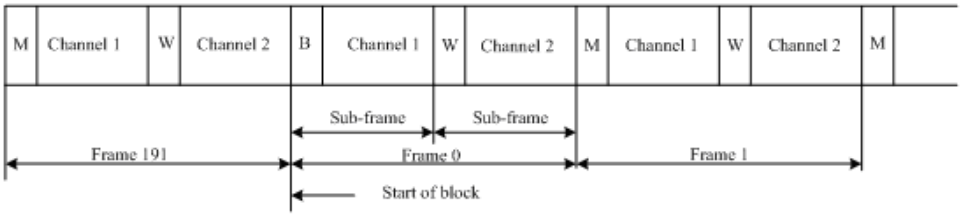


Figure 24-4 Frame format

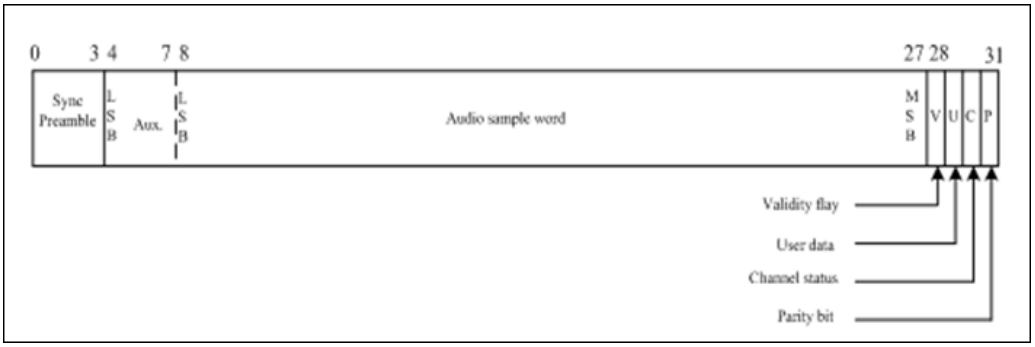


Figure 24-5 Sub-frame format

24.4 Register List

Table 24-1 I2S_SPDIF Controller Registers Address

Name	Physical Base Address
I2S_SPDIF	0xB0100000

Table 24-2 I2S/SPDIF Controller Registers

Offset	Register Name	Description
0x0000	I2S_CTL	I2S Control Register
0x0004	I2S_FIFOCTL	I2S FIFO Control Register
0x0008	I2STX_DAT	I2S TX FIFO Data Register
0x000c	I2SRX_DAT	I2S RX FIFO Data Register
0x0010	SPDIF_HDMI_CTL	SPDIF and HDMI FIFO Control Register
0x0014	SPDIF_DAT	SPDIF FIFO Data Register
0x0018	SPDIF_CLSTAT	SPDIF TX Channel Low Statue Register
0x001c	SPDIF_CHSTAT	SPDIF TX Channel High Statue Register
0x0020	HDMI_DAT	HDMI FIFO Data Register
0x002c	I2STX_SPDIF_HDMI_CTL	I2S TX, SPDIF, HDMI FIFO Virtual Address Control Register
0x0030	I2STX_SPDIF_HDMI_DAT	I2S TX, SPDIF, HDMI FIFO Data Register

24.5 Register Description

24.5.1 I2S_CTL

I2S Control Register
Offset = 0x00

Bit(s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:11	I2SPM	I2S PINS MODE: 00: 3-wire 01: 4-wire 10: 6-wire 11: reserved	RW	0x0
10	I2SRCS	I2S RX Clock Select: 0: from I2S_CLK2 1: from I2S_CLK1 (used by I2S TX)	RW	0x0
9:8	I2SRXM	I2S RX MODE: 00: 2.0-Channel Mode 01: 4-Channel TDM Mode A 1x: 4-Channel TDM Mode B	RW	0x0
7	-	Reserved	-	-
6:4	I2STXM	I2S TX MODE: 000: 2.0-Channel Mode 001: 5.1-Channel TDM Mode A 010: 5.1-Channel TDM Mode B 011: 7.1-Channel TDM Mode A 1xx: 7.1-Channel TDM Mode B	RW	0x0

3	I2STTDMRF	I2S TX TDM Mode data sample edge: 0: BCLK rising edge sample 1: BCLK falling edge sample	RW	0x0
2	I2STOWL	I2S TX output word length: 0: 32bit 1: Reserved	RW	0x0
1	I2SREN	I2S RX Enable. 0: Disable 1: Enable	RW	0x0
0	I2STEN	I2S TX Enable. 0: Disable 1: Enable	RW	0x0

Note:

1） I2S TX output word length 24bit can only be supported by 7.1-channel Mode, and can not be supported by 2.0-channel Mode/5.1-channel Mode.

2） I2SPM should be configed according to application when transmit I2S uses 3-wire, 4-wire or 6-wire.

3） When use I2SPM 3-wire, I2S TX and RX can not be enable at the same time.

4） When use I2SPM 4-wire, I2S RX should be enable at the same time.

5） Bit10:I2SRCS. In 3-wire Mode or 4-wire Mode, it can only be configure to 1

24.5.2 I2S_FIFOCTL

I2S FIFO Control Register

Offset = 0x04

Bit	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:19	KMCMMI2ST	Karaoke Multi-Channel Mix Mode. (not valid in Stereo Mix Mode) I2S RX Data Mix to I2S TX Data : 00: mix to all channels 01: mix to FL,FR 10: mix to FL,FR,C 11: mix to C	RW	0x0
18	I2STFSS	I2S TX Fifo Source Select: 0: APB 1: I2STX_SPDIF_HDMI_DAT	RW	0x0
17	I2SRFEF	I2S RX FIFO Empty Flag. 0: Not Empty 1: Empty	R	0x1
16	-	Reserved	-	-
15	I2STXKA	I2S TX Data Mix With I2S RX Data for Karaoke: 0: Disable 1: Enable	RW	0x0
14:13	-	Reserved	-	-
12	I2SRFIP	I2S RX FIFO Full IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0x0
11	I2SRFIEN	I2S RX FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0x0
10	I2SRFDEN	I2S RX FIFO Full DRQ Enable.	RW	0x0

		0: Disable 1: Enable		
9	I2SRFR	I2S RX FIFO Reset. 0: Reset FIFO 1: Enable FIFO	RW	0x0
8	I2STFFF	I2S TX FIFO Full Flag. 0: Not Full 1: Full	R	0x0
7:4	-	Reserved	-	-
3	I2STFIP	I2S TX FIFO Empty IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0x0
2	I2STFIEN	I2S TX FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	I2STFDEN	I2S TX FIFO Empty DRQ Enable. 0: Disable 1: Enable	RW	0x0
0	I2STFR	I2S TX FIFO Reset. It Controls Virtual Address Fifo and Actual Address Fifo. 0: Reset FIFO 1: Enable FIFO	RW	0x0

24.5.3 I2STX_DAT

I2S TX FIFO Data Register
Offset = 0x08

Bit	Name	Description	Access	Reset
31:8	I2STFDA	I2STX FIFO Data.	W	x
7:0	Reserved	-	R	0

24.5.4 I2SRX_DAT

I2S RX FIFO Data Register
Offset = 0x0C

Bit	Name	Description	Access	Reset
31:8	I2SRFDA	I2S RX FIFO Data.	R	x
7:0	Reserved	-	R	0

24.5.5 SPDIF_HDMI_CTL

SPDIF and HDMI Control Register
Offset = 0x010

Bit	Name	Description	Access	Reset
31:17	Reserved	-	R	x
16:15	KMCMMHDM	Karaoke Multi-Channel Mix Mode. (not valid in Stereo Mix Mode) I2S RX Data Mix to HDMI Data : 00: mix to all channels	RW	0x0

		01: mix to FL,FR 10: mix to FL,FR,C 11: mix to C		
14	HDMFSS	HDMI Fifo Source Select: 0: APB 1: I2STX_SPDIF_HDMI_DAT	RW	0x0
13	SPDFSS	SPDIF Fifo Source Select: 0: APB 1: I2STX_SPDIF_HDMI_DAT	RW	0x0
12	HDMKA	HDMI Data Mix With I2S RX Data for Karaoke: 0: Disable 1: Enable	RW	0x0
11	SPDKA	SPDIF Data Mix With I2S RX Data for Karaoke: 0: Disable 1: Enable	RW	0x0
10	SPDEN	SPDIF Enable. 0: Disable (will reset TX state machine) 1: Enable	RW	0x0
9	HDMFIEN	HDMI FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
8	HDMFDEN	HDMI FIFO Empty (16 level left) DRQ Enable. 0: Disable 1: Enable	RW	0x0
7	HDMFFF	HDMI FIFO FULL Flag. 0: Not Full 1: Full	R	0x0
6	HDMFIP	HDMI FIFO Empty IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0x0
5	SPDFIEN	SPDIF FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
4	SPDFDEN	SPDIF FIFO Empty (16 level) DRQ Enable. 0: Disable 1: Enable	RW	0x0
3	SPDFFF	SPDIF FIFO FULL Flag. 0: Not Full 1: Full	R	0x0
2	SPDFIP	SPDIF FIFO Empty IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0x0
1	HDMFR	HDMI FIFO Reset. It Controls Virtual Address Fifo and Actual Address Fifo. 0: Reset FIFO 1: Enable FIFO	RW	0x0
0	SPDFR	SPDIF FIFO Reset. It Controls Virtual Address Fifo and Actual Address Fifo. 0: Reset FIFO 1: Enable FIFO	RW	0x0

24.5.6 SPDIF_DAT

SPDIF FIFO Data Register
Offset = 0x14

Bit	Name	Description	Access	Reset
31:8	SPDFDA	SPDIF FIFO Data.	W	x
7:0	-	Reserved	R	0

24.5.7 SPDIF_CLSTAT

SPDIF TX Channel Low Statue Register
Offset = 0x18

Bit	Name	Description	Access	Reset
31:0	SPDCLSTAT	SPDIF TX Channel Low Status. (Channel status bit31 to bit0.)	RW	x

24.5.8 SPDIF_CHSTAT

SPDIF TX Channel High Statue Register
Offset = 0x1C

Bit	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	SPDCHSTAT	SPDIF TX Channel High Status. (Channel status bit47 to bit32.)	RW	x

24.5.9 HDMI_DAT

HDMI FIFO Data Register
Offset = 0x20

Bit	Name	Description	Access	Reset
31:8	HDMFDA	HDMI FIFO Data.	W	x
7:0	-	Reserved	R	0

24.5.10 I2STX_SPDIF_HDMI_CTL

I2S TX, SPDIF, HDMI FIFO Virtual Address Control Register
Offset = 0x2C

Bit	Name	Description	Access	Reset
31:2	Reserved	-	R	0
1	VADEN	Virtual Address DRQ Enable: 0: disable 1: enable	RW	0x0
0	VASS	Virtual Address Source Select: 0: Reserved 1: from APB	RW	0x0

24.5.11 I2STX_SPDIF_HDMI_DAT

I2S TX, SPDIF, HDMI FIFO Data Register
Offset = 0x30

Bit	Name	Description	Access	Reset
31:8	ISHFDA	I2S TX, SPDIF, HDMI FIFO Data. When writing to this address, data will be sent to I2STFDA, SPDFDA and HDMFDA correspondingly if I2STFSS , SPDFSS ,HDMFSS are enable.	W	x
7:0	Reserved	-	R	0

24.6 Application Note

24.6.1 I2S TX operation

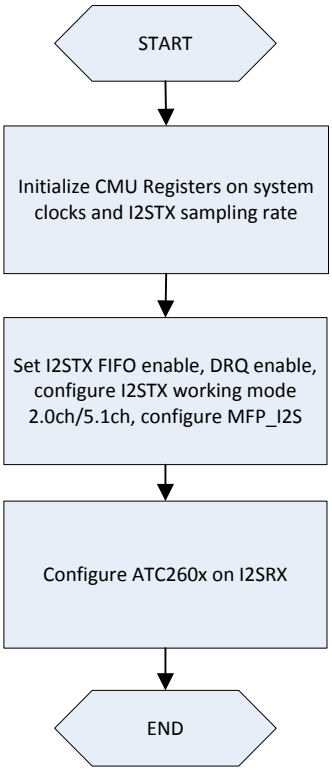


Figure 24-6 I2S TX works with ATC260x Control Flow

24.6.2 I2S RX operation

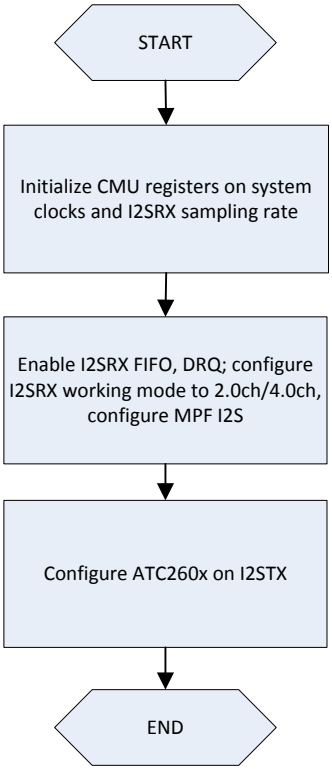


Figure 24-7 I2SRX works with ATC260x Control Flow

24.6.3 Karaoke operation

S500 supports voice from ATC260x to mix to HDMI FIFO, SPDIF FIFO, I2STX FIFO directly in digital domain by hardware, which each access has an enable bit. Karaoke mix include Stereo Mix Mode and Multi-Channel Mix Mode (5.1-channel and 7.1-channel). When background music sent to FIFO is stereo, Karaoke Multi-Channel Mix Mode should be configured to 00, which mix to all channels. When the background music sent to FIFO from 5.1-channel or 7.1-channel, Karaoke Multi-Channel Mix Mode has 4 configure choices, which can be configure to mix to all channels, mix to FL,FR, mix to FL,FR, mix to FL,FR,C, mix to C. And background music data sent to FIFO should according to this sequence, FL,FR,SW,C,BL,BR (,SBL,SBR). Otherwise it may not mix to the correct channels.

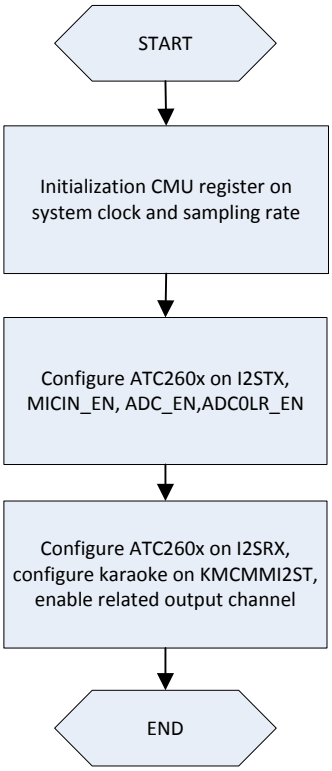


Figure 24-8 Karaoke with ATC260x Control Flow

ATC260x is configure to 1 or 2 microphone OP enable, ADC enable, ADC0LR enable for add ADC left channel and right channel data which then the two channels send the same data to ADC digital and send out by I2S TX. S500 will receive from I2S RX and mix data to I2S TX, HDMI audio or SPDIF when corresponding I2STXKA, HDMKA or SPDKA is enable.

25 PCM (Pulse Code Modulation)

25.1 Overview

Pulse Code Modulation (PCM) is the method of encoding an audio signal in digital format. Features of PCM are listed below.

- Include 2 PCM Modules, PCM0 and PCM1
- Include PCM TX and PCM RX, both can work as Master Mode or Slave Mode
- Linear PCM (13-16bit), u-Law (8bit), A-Law (8bit)
- PCM clock in Master Mode 2.048MHz, in Slave Mode up to 2.048MHz
- Long Frame Sync and Short Frame Sync

25.2 Block Diagram

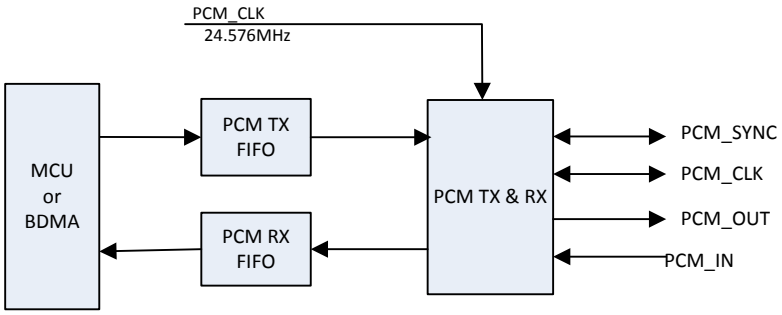


Figure 25-1 Main Block

25.3 Function Description

PCM data can be linear PCM (13-16bit), u-Law (8bit) or A-Law (8bit). The interface can be programmed as Master or as Slave.

PCM clock and data are in master mode available at 2.048MHz to allow interfacing to standard CODEC.

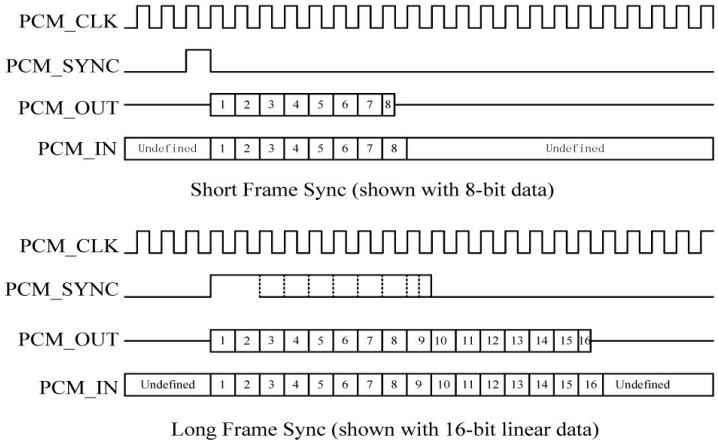


Figure 25-2 PCM Timing

25.4 Register List

Table 25-1 PCMx Controller Registers Address

Name	Physical Base Address
PCM0	0xB0110000
PCM1	0xB0118000

Table 25-2 PCMx Controller Registers

Offset	Register Name	Description
0x0000	PCMx_CTL	PCM Control Register
0x0004	PCMx_STAT	PCM Status Register
0x0008	PCMx_RXDAT	PCM Receive FIFO Data Register
0x000C	PCMx_TXDAT	PCM Transmit FIFO Data Register

Note: x=0,1

25.5 Register Description

25.5.1 PCMx_CTL

PCMx Control Register
Offset = 0x00+x*0x8000, x=0,1

Bit(s)	Name	Description	Access	Reset
31:20	-	Reserved	R	0
19	EN	PCM Enable. 0: Disable 1: Enable	RW	0
18	SEN	Sign Extension Enable(only when 16bit slots are used). 0: Select zeros padding or audio gain. 1: Select sign extension. When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit companded sample. When writing the bit is 1, the unused bits are both sign extension.	RW	0
17	SAMF	Sample Format 0: 8bit sample with 8 cycle slot duration 1: 8bit sample with 16 cycle slot duraton	RW	0
16	IVEN	Inversion Enable. 0: Disable 1: Enable. When inversion enables, inversion is performed for A-Law even bit andd for u-Law all bit.	RW	0
15	MS	PCM Master/Slave Select. 0: Master 1: Slave	RW	0
14	FRMS	PCM Frame Mode Select 0: Short Frame Sync Mode 1: Long Frame Sync Mode	RW	0
13	FINS	PCM FIFO Input Source Select. 0: Data from APB The data will be send out through PCM_OUT pin	RW	0
12	LBEN	Loop Back Enable.	RW	0

		Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable		
11:10	RWC	RW control 00 read and write 01 read only 10 write only 11 reversed	RW	0
9	LMFR	LSB or MSB First. 0: MSB first 1: LSB first when transmitting and receiving voice samples.	RW	0
8	SSOE	SYNC Suppress Output Enable. 0: Enable SYNC output 1: Disable SYNC output when keeping PCM_CLK running when in master mode. Some CODEC utilize the mode to enter a low power mode.	RW	0
7	TXIE	PCM TX IRQ Enable. 0: Disable 1: Enable	RW	0
6	RXIE	PCM RX IRQ Enable. 0: Disable 1: Enable	RW	0
5	TXDE	PCM TX DRQ Enable 0: Disable 1: Enable	RW	0
4	RXDE	PCM RX DRQ Enable 0: Disable 1: Enable	RW	0
3	DATO	PCM Data Output Mode. 0: Normal Output 1: Forces PCM_OUT to ouput 0	RW	0
2:0	DATM	PCM Data Mode Select 000: u-Law(8bit) 001: A-Law(8bit) 010: linear PCM(13bit) 011: linear PCM(14bit) 100: linear PCM(15bit) 101: linear PCM(16bit)	RW	0

25.5.2 PCMx_STAT

PCMx Status Register
Offset = 0x04+x*0x8000, x=0,1

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7	TFES	TX FIFO empty Status 1: empty 0: no empty	R	1

6	RFFS	RX FIFO full Status 0: no full 1: full	R	0
5	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
4	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
3	TFEP	TX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to the bit will clear it or reset FIFO clear it.	RW	0
2	RFEP	RX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to the bit will clear it or reset FIFO clear it.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear the bit.	RW	1
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0

25.5.3 PCMx_RXDAT

PCMx RX FIFO Data Register
Offset = 0x08+x*0x8000, x=0,1

Bit(s)	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	RXDAT	PCM RX FIFO Data. The depth of FIFO is 16bit x 16 levels.	R	x

25.5.4 PCMx_TXDAT

PCMx TX FIFO Data Register
Offset = 0x0C+x*0x8000, x=0,1

Bit(s)	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	TXDAT	PCM TX FIFO Data. The depth of FIFO is 16bit x 16 levels.	W	x

25.6 Application Note

25.6.1 Control Flow

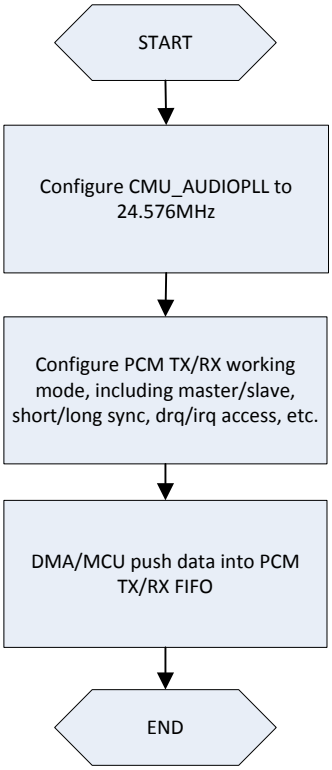


Figure 25-3 PCM TX/RX Control Flow

26 Ethernet MAC

26.1 Overview

The Ethernet MAC Controller provides interface for Ethernet signal from application processor to RMII/SMII interface. It is compliant with the IEEE 802.3 standard for Media Access Control (MAC) over the 10Mbps and 100Mbps Ethernet. Features of Ethernet MAC are listed below:

- Supports 10/100 Mb/s data transfer rate
- Supports RMII/SMII interface
- Meets the IEEE 802.3 CSMA/CD standard
- Full or half duplex operation
- Flexible address filtering
- Up to 16 physical addresses
- 512-bit hash table for multicast addresses
- Scatter/gather capabilities
- Descriptor "ring" or "chain" structures
- Automatic descriptor list polling
- Clock switching supported
- Operates as internal configurable FIFOs
- Programmable transmit threshold levels

26.2 Block Diagram

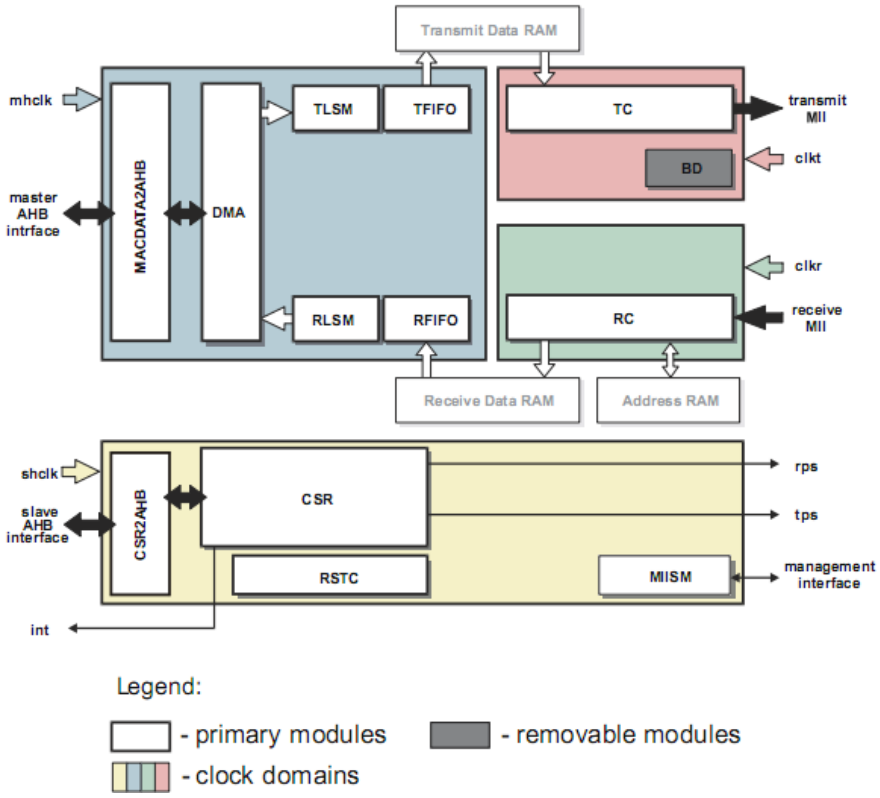


Figure 26-1 Block Diagram

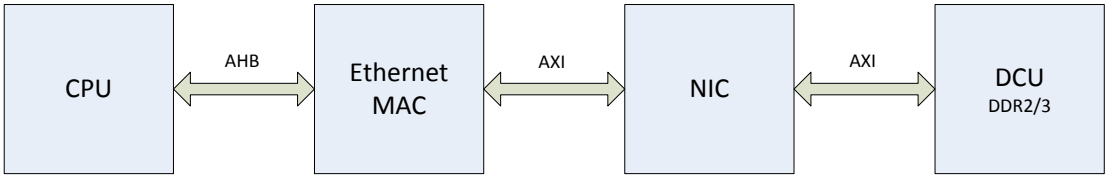


Figure 26-2 Bus interface

26.3 Function Description

Communication with an external host is implemented via a set of Control and Status Registers and the DMA controller for external shared RAM memory. For data transfers the MAC AHB operates as a DMA master. It automatically fetches from transmit data buffers and stores receive data buffers into external RAM with minimum CPU intervention. The linked list management enables the use of various memory allocation schemes. There is an interface for external dual port RAMs serving as configurable FIFO memories and there are separate memories for transmit and receive processes. Using the FIFOs additionally isolates the MAC AHB from an external host and provides resolution in case of latency of an external bus.

TC – Transmit Controller

The transmit controller implements the 802.3 transmit operation. From the network side it uses the standard 802.3 MII interface for an external PHY device. The transmit controller operates synchronously with the clkt clock from the module

BD – Backoff/Deferring

The backoff/deferring controller implements the 802.3 half duplex operation. It operates synchronously with the clkt clock from the module. The backoff/deferring controller can be optionally removed for lower gate count if the half duplex operation is not required

RC – Receive Controller

The receive controller implements the 802.3 receive operation. From the network side it uses the standard 802.3 MII interface for an external PHY device. The receive controller operates synchronously with the clkr clock from the module.

TFIFO – Transmit FIFO Controller

The transmit FIFO controller is used for buffering data prepared for transmission by the MAC AHB. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core. The TFIFODEPTH parameter defines the total FIFO size. The FIFO size is equal to 2TFIFODEPTH -1. The TCDEPTH parameter defines the maximum number of frames that can reside in the transmit FIFO at the moment. The actual number is equal to 2TCDEPTH -1. The transmit FIFO controller operates synchronously with the mhclk clock from the host interface

RFIFO – Receive FIFO Controller

The receive FIFO controller is used for buffering data received by the MAC AHB. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core. The RFIFODEPTH parameter defines the total FIFO size. The FIFO size is equal to 2RFIFODEPTH -1. The RCDEPTH parameter defines the maximum number of frames that can reside in the receive FIFO at the moment. The actual number is equal to 2RCDEPTH -1. The receive FIFO controller operates synchronously with the mhclk clock from the host interface.

TLSM – Transmit linked List State Machin

The transmit linked list state machine implements the descriptor / buffer architecture of the MAC AHB. It manages the transmit descriptor list, and fetches the data prepared for transmission from the data buffers

into the transmit FIFO. The transmit linked list state machine controller operates synchronously with the mhclk clock from the host interface.

RLSM – Receive linked List State Machine

The receive linked list state machine implements the descriptor/ buffer architecture of the MAC AHB. It manages the receive descriptor list, and moves the data the receive FIFO into the data buffers. The receive linked list state machine controller operates synchronously with the mhclk clock from the host interface.

DMA – Direct Memory Access controller

The direct memory access controller implements the host Data interface. It services both the receive and the transmit channels. The direct memory access controller operates synchronously with the mhclk clock from the host interface.

MACDATA2AHB – AHB master wrapper

The MAC data to AHB interface wrapper. It translates MAC data access operations to AHB control, address and data signals. The AHB wrapper component operates synchronously with the mhclk clock from the host AHB master interface

CSR – Control and Status Registers

The CSR component is used to control the MAC AHB operation by the host. It implements the register set, the interrupt controller, and the power management functionality of the MAC AHB. It also provides an interface for the host. The CSR component operates synchronously with the shclk clock from the host interface.

MACCSR2AHB – AHB slave wrapper

The MAC CSR to AHB slave interface wrapper. It translates host read or write AHB operations into MAC CSR interface operations. The APB wrapper component operates synchronously with the shclk clock from the host AHB slave interface.

RSTC – Reset Controller

The reset controller is used to reset all components of the MAC AHB. It generates a reset signal synchronous to all clock domains in the design from the single external reset line.

Receive data RAM

Synchronous dual port RAM working as the receive FIFO.

Transmit data RAM

Synchronous dual port RAM working as the transmit FIFO.

Address RAM

Synchronous dual port RAM working as the addresses memory.

26.4 Register List

Table 26-1 Ethernet Base Address

Name	Physical Base Address
Ethernet	0xB0310000

Table 26-2 Ethernet Register List

Offset	Register Name	Description
0x0000	MAC_CSR0	Bus mode register

0x0008	MAC_CSR1	Transmit poll demand register
0x0010	MAC_CSR2	Receive poll demand register
0x0018	MAC_CSR3	Receive descriptor list base address register
0x0020	MAC_CSR4	Transmit descriptor list base address register
0x0028	MAC_CSR5	Status register
0x0030	MAC_CSR6	Operation mode register
0x0038	MAC_CSR7	Interrupt enable register
0x0040	MAC_CSR8	Missed frames and overflow counter register
0x0048	MAC_CSR9	MII management and serial ROM register
0x0050	MAC_CSR10	MII serial management*
0x0058	MAC_CSR11	General-purpose timer and interrupt mitigation control register
0x0080	MAC_CSR16	MAC address low*
0x0088	MAC_CSR17	MAC address high*
0x0090	MAC_CSR18	Pause time & cache thresholds*
0x0098	MAC_CSR19	Pause control FIFO thresholds*
0x00A0	MAC_CSR20	Flow control setup & status*
0x0200~0x03F8	SC0~126	Statistical Counters* (0x0200 - 0x3F8)
0x00B0	MAC_CTRL	MAC control register

26.5 Register Description

26.5.1 MAC_CSR0

Bus Mode Register
Offset = 0x0000

Bit	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20	DBO	Descriptor byte ordering mode. 1 – big endian mode used for data descriptors. 0 – little endian mode used for data descriptors. DBO can be written only when both the receive and the transmit processes are stopped. Note that the big endian setting can only be used in OCP version of the core (it is not available on AMBA AHB™).	RW	0
19:17	TAP	Transmit automatic polling. If the TAP is written with a nonzero value, the MAC-1G/MAC performs an automatic transmit descriptor polling when operating in suspended state. When the descriptor is available, the transmit process goes into the running state. When the descriptor is marked as owned by the host, the transmit process remains suspended. The poll is always performed at the current transmit descriptor list position. The time interval between two consecutive polls is shown in table 7. The actual interval is based on the network side MII clock source. It is calculated by dividing clkt clock. This produces different absolute time values for each	RW	0

		operating mode (10/100). TAP can be written only when the transmit processes is stopped.		
16:8	-	Reserved	-	-
7	BLE	Big/Little endian. Selects the byte-ordering mode used by the data buffers. 1 – big endian mode used for the data buffers. 0 – little endian mode used for the data buffers. BLE can be written only when both the receive and transmit processes are stopped. Note that the big endian setting can only be used in OCP version of the core (it is not available on AMBA AHB).	RW	0
6:2	DSL	Descriptors skip length. Specifies the number of 128-bit words between two consecutive unchained descriptors. For example, when the DSL=0 then consecutive descriptors are read from following addresses 0x***00, 0x***10, 0x***20, etc; when the DSL=1 then consecutive descriptors are read from following addresses 0x***00, 0x***20, 0x***40, etc; DSL can be written only when both the receive and the transmit processes are stopped.	RW	0
1	BAR	Bus arbitration mode. 0 – means that the Rx process has priority over Tx process. When both Rx and Tx processes request the bus, than the sequence of transfers on the DMA bus looks like: Rx->Rx->Tx->Rx->Rx->Tx… In other words, single Tx access is placed between every two consecutive Rx accesses. Using this mode helps to prevent Rx FIFO from overflow. 1 – means that Rx and Tx processes share equal priority for DMA access. Round Robin arbitration is used in which the sequence of transfers on the DMA bus looks like: Rx->Tx->Rx->Tx->Rx…	RW	0
0	SWR	Software reset. Setting this bit resets all internal flip-flops except external PHY interface wrappers and AHB interface wrappers. SWR will be cleared automatically when the reset operation is complete.	RW	0

Table 26-3 Transmit automatic polling intervals

CSR0(19:17)	Time	10Mb/s	100Mb/s
000	TAP disabled	TAP disabled	TAP disabled
001	(g)mii_period * 2048	819.2 us	81.92 us
010	(g)mii_period * 4096	1.638 ms	163.8 us
011	(g)mii_period * 8192	3.276 ms	327.6 us
100	(g)mii_period * 128	51.2 us	5.12 us
101	(g)mii_period * 256	102.4 us	10.24 us
110	(g)mii_period * 512	204.8 us	20.48 us
111	(g)mii_period * 1024	409.6 us	40.96 us

26.5.2 MAC_CSR1

Transmit poll demand register
Offset = 0x0008

Bit	Name	Description	Access	Reset
31:0	TPD	Writing this field with any value instructs the MAC AHB to check for frames to be transmitted. This operation is valid only when the transmit process is suspended. If no descriptor is available the transmit process remains suspended. When the descriptor is available the transmit process enters the running state. This is write only register, reading always returns 0x00000000 value.	RW	0x0

26.5.3 MAC_CSR2

Receive poll demand register
Offset = 0x0010

Bit	Name	Description	Access	Reset
31:0	RPD	Writing this field with any value instructs the MAC AHB to check for receive descriptors to be acquired. This operation is valid only when the receive process is suspended. If no descriptor is available the receive process remains suspended. When the descriptor is available the receive process enters the running state. This is write only register, reading always returns 0x00000000 value.	RW	0x0

26.5.4 MAC_CSR3

Receive descriptor list base address register
Offset = 0x0018

Bit	Name	Description	Access	Reset
31:0	RLA	Start of the receive list address. Contains the address of the first descriptor in a receive descriptor list. This address should be longword aligned (RLA(1:0)=00).	RW	0x0

26.5.5 MAC_CSR4

Transmit descriptor list base address register
Offset = 0x0020

Bit	Name	Description	Access	Reset
31:0	TLA	Start of the transmit list address. Contains the address of the first descriptor in a transmit descriptor list. This address should be long-word aligned (TLA(1:0)=00).	RW	0x0

26.5.6 MAC_CSR5

Status register
Offset = 0x0028

Bit	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22:20	TS	Transmit process state (Read only). Indicates the current state of a transmit process: 000 - Stopped, RESET or STOP TRANSMIT command issued 001 - Running, fetching transmit descriptor. 010 - Running, waiting for end of transmission. 011 - Running, transferring data buffer from host memory to FIFO. 100 - Reserved. 101 - Running, setup packet. 110 - Suspended, FIFO underflow or unavailable descriptor. 111 – Running, closing transmit descriptor.	R	0
19:17	RS	Receive process state (Read only). Indicates the current state of a receive process: 000 - Stopped, RESET or STOP RECEIVE command issued. 001 - Running, fetching receive descriptor. 010 - Running, waiting for the end of receive packet before prefetch of next descriptor. 011 - Running, waiting for receive packet. 100 - Suspended, unavailable receive buffer. 101 - Running, closing receive descriptor. 110 - Not used 111 – Running, transferring data from FIFO to host memory.	R	0
16	NIS	Normal interrupt summary. This bit is logical or on the following bits: CSR5.0 - Transmit interrupt CSR5.2 - Transmit buffer unavailable CSR5.6 - Receive interrupt CSR5.11 - General purpose timer overflow CSR5.14 – Early receive interrupt Only the unmasked bits affect the normal interrupt summary bit. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
15	AIS	Abnormal interrupt summary. This bit is logical or on the following bits: CSR5.1 - Transmit process stopped CSR5.5 - Transmit underflow CSR5.7 - Receive buffer unavailable CSR5.8 - Receive process stopped CSR5.10 – Early transmit interrupt Only the unmasked bits affect the abnormal interrupt summary bit. the user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0

14	ERI	Early receive interrupt. Set when the MAC AHB fills the data buffers of the first descriptor. Cleared by the MAC AHB after the receive interrupt (CSR5.6). The user can clear this bit by writing 1. Writing 0 has no effect.	RW	0
11	GTE	General-purpose timer expiration. Set when the general-purpose timer reaches a value of zero. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
10	ETI	Early transmit interrupt. Indicates that the packet to be transmitted was fully transferred into the FIFO. This bit is cleared by the MAC AHB after the transmit interrupt (CSR5.0). The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
8	RPS	Receive process stopped. RPS is set when a receive process enters a stopped state. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
7	RU	Receive buffer unavailable. When set, indicates that the next receive descriptor is owned by the host and is unavailable for the MAC AHB . When RU becomes set, the MAC AHB enters a suspended state,and returns to receive descriptor processing when the host changes ownership of the descriptor and either a receive poll demand command is issued or a new frame is recognized by the MAC AHB . The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
6	RI	Receive interrupt. Indicates the end of a frame receive. The complete frame has been transferred into the receive buffers. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
5	UNF	Transmit underflow. Indicates that the transmit FIFO was empty during a transmission. The transmit process goes into a suspended state. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
4:3	-	Reserved	R	0
2	TU	Transmit buffer unavailable. When set, TU indicates that the host owns the next descriptor on the transmit descriptor list therefore it cannot be used by the MAC AHB . When the TU becomes set, the transmit process goes into a suspended state and can resume normal descriptor processing when the host changes ownership of the	RW	0

		descriptor and either a transmit poll demand command is issued or transmit automatic polling is enabled. The user can clear this bit by writing a '1'. Writing a '0' has no effect.		
1	TPS	Transmit process stopped. TPS is set when the transmit process goes into a stopped state. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0
0	TI	Transmit interrupt. Indicates the end of a frame transmission process. The user can clear this bit by writing a '1'. Writing a '0' has no effect.	RW	0

26.5.7 MAC_CSR6

Operation mode register
Offset = 0x0030

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>31</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>30</td><td>RA</td><td>Receive all.
When set, all incoming frames are received regardless of their destination address. an address check is performed and the result of the check is written into the receive descriptor (RDES0.30).
RA can be changed only when the receive process is in a stopped state.</td><td>RW</td><td>0</td></tr>
<tr><td>29:23</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>22</td><td>TTM</td><td>Transmit threshold mode.
0 – transmit threshold mode appropriate for 100 Mb/s mode.
1 – transmit threshold mode appropriate for 10 Mb/s mode.
Changing this bit is allowed only when the transmitter process is in the stopped state.</td><td>RW</td><td>0</td></tr>
<tr><td>21</td><td>SF</td><td>Store and forward.
When set, the transmission starts after a full packet is written into the transmit
FIFO, regardless of the current FIFO threshold level.
Changing this bit is allowed only when the transmitter process is in the stopped
state.</td><td>RW</td><td>0</td></tr>
<tr><td>20:18</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>17:16</td><td>SPEED</td><td>Ethernet Speed Selection.
The value in this field is used to drive the external speed pin used to
configure external components as defined below.
<table>
<tr><td>CSR6.17</td><td>CSR6.16</td><td>Ethernet speed mode</td><td>speed signal [1:0]</td></tr>
<tr><td>1</td><td>0</td><td>10Mbps</td><td>00</td></tr>
</table></td><td>RW</td><td>0</td></tr>
</table>

		0 | 0 | 100Mbps | 01 SPEED bits can be changed only when both the transmit and the receive processes are in the stopped state.		
15:14	TR	Threshold control bits. This bit, together with the TTM and the SF, control the threshold level for the transmit FIFO. Changing this bit is allowed only when the transmitter process is in the stopped state.	RW	0
13	ST	Start/stop transmit command. Setting this bit when the transmit process is in a stopped state causes transition into a running state. In the running state the MAC AHB checks the transmit descriptor at a current descriptor list position. If the MAC AHB owns the descriptor then the data starts to transfer from memory into the internal transmit FIFO. When the host owns the descriptor, the MAC AHB enters a suspended state. Clearing this bit when the transmit process is in a running or a suspended state instructs the MAC AHB to enter the stopped state.	RW	0
12:11	-	Reserved	-	-
10	LP	Loopback mode. 0 – normal operation 1 – internal loopback. When working in the internal loopback mode, the transmitted frames are routed back to the receiver inside the core. The external loopback pin should be used to switch the receive clock externally, on the chip-level. The system designer should provide the receive clock synchronous to the transmit clock when working in the loopback. Standard receive clock recovered from the PHY cannot be used in the loopback mode.	RW	0
9	FD	Full duplex mode. 0 – half duplex mode. 1 – forcing full duplex mode. Changing this bit is allowed only when both the transmitter and receiver processes are in the stopped state.	RW	0
8	-	Reserved	-	-
7	PM	Pass all multicast. When set, all the frames with the multicast destination addresses will be received regardlessof the address check result. of the address check result. PM can be changed only when the receive process is in a stopped state.	RW	0
6	PR	Promiscuous mode. When set all the frames will be received regardless of the address check result. an address check is not performed.	RW	1

		PR can be changed only when the receive process is in a stopped state.		
5	-	Reserved	-	-
4	IF	Inverse filtering (Read only). If this bit is set when working in a perfect filtering mode, the receiver performs an inverse filtering during the address check process. The "filtering type" bits of the setup frame determine a state of this bit.	R	0
3	PB	Pass bad frames. When set, the MAC AHB transfers all frames into the data buffers, regardless of the receive errors. This allows the runt frames, collided fragments and truncated frames to be received. PB can be changed only when the receive process is in a stopped state.	RW	0
2	HO	Hash only filtering mode (Read only). When set, the MAC AHB performs an imperfect filtering over both the multicast and the physical addresses. The "filtering type" bits of the setup frame determine the state of this bit.	R	0
1	SR	Start/stop receive command. Setting this bit when the receive process is in a stopped state causes the transition into a running state. In the running state the MAC AHB checks the receive descriptor at the current descriptor list position. If the MAC AHB owns the descriptor, then it can process an incoming frame. When the host owns the descriptor, the receiver enters a suspended state and also sets the CSR5.7 (receive buffer unavailable) bit. Clearing this bit when the receive process is in running or suspended state instructs the MAC AHB to enter a stopped state after receiving the current frame.	RW	0
0	HP	Hash/perfect receive filtering mode (Read only). 0 – perfect filtering of the incoming frames is performed according to the physical addresses specified in a setup frame. 1 – imperfect filtering over the frames with the multicast addresses is performed according to the hash table specified in a setup frame. A physical addresses check is performed according to the CSR6.2 (HO - Hash only) bit. When the HO and HP are both set, an imperfect filtering is performed on all of the addresses. The "filtering type" bits of the setup frame determine the state of this bit.	R	0

All the possible combinations of the address filtering bits are listed in Table below. The actual values of the IF, HO, and HP bits are determined by the filtering type (FT1:FT0) bits in the setup frame. The IF, HO and HP bits are read-only

PM CSR 6.7	PR CSR 6.6	IF CSR 6.4	HO CSR 6.2	HP CSR 6.0	Current Filtering mode
0	0	0	0	0	16 physical addresses – perfect filtering mode

0	0	0	0	1	1 physical address for physical addresses and 512-bit hash table for multicast addresses
0	0	0	1	1	512-bit hash table for both physical and multicast addresses
0	0	1	0	0	Inverse filtering
*	1	0	0	*	Promiscuous mode
0	1	0	1	1	Promiscuous mode
1	0	0	0	*	Pass all multicast frames
1	0	0	1	1	Pass all multicast frames

Table 26-4 Transmit FIFO threshold levels (bytes)

CSR6.21	CSR6.(15:14)	CSR6.22=1	CSR6.22=0
0	00	64	128
0	01	128	256
0	10	128	512
0	11	256	1024
1	xx	Store and Forward	Store and Forward

26.5.8 MAC_CSR7

Interrupt enable register
Offset = 0x0038

Bit	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	NIE	Normal interrupt summary enable. When set, normal interrupts are enabled. Normal interrupts are listed below: CSR5.0 – Transmit interrupt CSR5.2 – Transmit buffer unavailable CSR5.6 – Receive interrupt CSR5.11 – General-purpose timer expired CSR5.14 – Early receive interrupt	RW	0
15	AIE	Abnormal interrupt summary enable. When set, abnormal interrupts are enabled. Abnormal interrupts are listed below: CSR5.1 – Transmit process stopped CSR5.5 – Transmit underflow CSR5.7 – Receive buffer unavailable CSR5.8 – Receive process stopped CSR5.10 – Early transmit interrupt	RW	0
14	ERE	Early receive interrupt enable. When both the ERE and normal interrupt enable bits are set, early receive interrupt is enabled.	RW	0
13:12	-	Reserved	-	-
11	GTE	General-purpose timer overflow enable. When both the GTE and normal interrupt summary enable bits are set, the general-purpose timer overflow interrupt is enabled	RW	0
10	ETE	Early transmit interrupt enable. When both the ETE and abnormal interrupt summary enable bits are set, the early transmit interrupt is enabled.	RW	0

9	-	Reserved	-	-
8	RSE	Receive stopped enable. When both the RSE and abnormal interrupt summary enable bits are set, the receive stopped interrupt is enabled.	RW	0
7	RUE	Receive buffer unavailable enable. When both the RUE and abnormal interrupt summary enable bits are set, the receive buffer unavailable is enabled.	RW	0
6	RIE	Receive interrupt enable. When both the RIE and normal interrupt summary enable bits are set, the receive interrupt is enabled.	RW	0
5	UNE	Underflow interrupt enable. When both the UNE and abnormal interrupt summary enable bits are set, the transmit underflow interrupt is enabled.	RW	0
4:3	-	Reserved	-	-
2	TUE	Transmit buffer unavailable enable. When both the TUE and normal interrupt summary enable bits are set, the transmit buffer unavailable interrupt is enabled.	RW	0
1	TSE	Transmit stopped enable. When both the TSE and abnormal interrupt summary enable bits are set, the transmit process stopped interrupt is enabled.	RW	0
0	TIE	Transmit interrupt enable. When both the TIE and normal interrupt summary enable bits are set, the transmit interrupt is enabled.	RW	0

26.5.9 MAC_CSR8

Missed frames and overflow counter register
Offset = 0x0040

Bit	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28	OCO	Overflow counter overflow (read only). Gets set when the FIFO overflow counter overflows. Reset when read.	R	0
27:17	FOC	FIFO overflow counter (read only). Counts the number of frames not accepted due to the receive FIFO overflow. The counter resets when read.	R	0
16	MFO	Missed frame overflow counter (read only). Set when a missed frame counter overflows. Reset when read.	R	0
15:0	MFC	Missed frame counter (read only). Counts the number of frames not accepted due to the unavailability f the receive descriptor. The counter resets when read.	R	0

26.5.10 MAC_CSR9

MII management and serial ROM register
Offset = 0x0048

Bit	Name	Description	Access	Reset

31:20	-	Reserved	-	-
19	MDI	MII management data in signal (read only). This bit reflects the sample on the MDI pin during the read operation on the MII management interface.	R	0
18	MII	MII management operation mode. 1 – indicates that the MAC reads the MII PHY registers. 0 – indicates that the MAC writes to the MII PHY registers.	RW	0
17	MDO	MII management write data. The value of this bit drives the MDO pin when a write operation is performed.	RW	0
16	MDC	MII management clock. The value of this bit drives the MDC pin.	RW	0
15:4	-	Reserved	R	0
3	SDO	Serial ROM data output. The value of this bit drives the sdo pin of the MAC.	RW	0
2	SDI	Serial ROM data input. This bit reflects the sdi pin of the MAC.	R	0
1	SCLK	Serial ROM clock. The value of this bit drives the sclk pin of the MAC	RW	0
0	SCS	Serial ROM chip select. The value of this bit drives the scs pin of the MAC.	RW	0

26.5.11 MAC_CSR10

The MII serial management register
Offset = 0x0050

Bit	Name	Description	Access	Reset
31	SB (START/ BUSY)	Writing this bit with "1" starts management data transfer or applying MIISM settings respectively to used opcode. When read as "1" indicates that data transition / setting applying process is in progress; When read as "0" indicates data transition / setting applying process completion.	RW	0
30:28	CLKDIV	When register is read this field contains actual MIISM clock divider settings Writing register with new CLKDIV value simultaneously with OPCODE set to "11" and START bit set, applying new clock divider settings on next rising edge of MDCLK signal. Clock divider settings: "000" - MDC = clk / 8 "001" - MDC = clk / 16 "010" - MDC = clk / 32 "011" - MDC = clk / 64 "100" - MDC = clk / 128 "101" - MDC = clk / 256 "110" - MDC = clk / 512 "111" - MDC = clk / 1024 The default value is "011" and the management clock generation is disabled after reset.	RW	0x3
27:26	OPCODE	MIISM operation code:	RW	0

		"00" – disable clock generation, "01" - register write command, "10" - register read command, "11" - clock divider set. Applying commands "00" disables the management clock generation while applying any other command enables the management clock generation.		
25:21	PHYADD	Physical layer address for current transfer	RW	0
20:16	REGADD	Register address for the current transfer.	RW	0
15:0	DATA	Register data. When write operation is selected (OPCODE="10"), the data from this filed will be written to selected register. When register read code is used (OPCODE="01"), the field will be overwritten by the data from selected register.	RW	0

26.5.12 MAC_CSR11

General-purpose timer and interrupt mitigation control register
0x0058

Bit	Name	Description	Access	Reset
31	CS	Cycle size. Controls the time units for the transmit and receive timers according to the following table: 1 – MII 100Mb mode – 5.12us, MII 10Mb mode – 51.2us 0 – MII 100Mb mode – 81.92us, MII 10Mb mode – 819.2us	RW	0
30:27	TT	Transmit timer. Controls the maximum time that must elapse between the end of a transmit operation and and setting the CSR5.TI (Transmit Interrupt) bit. This time is equal to TT * (16*CS). The transmit timer is enabled when written with nonzero value. After each frame transmission the timer starts to count down if it has not already started. It is reloaded after every frame transmitted. Writing '0' to this field disables the timer effect on the transmit interrupt mitigation mechanism. Reading this field gives the actual count value of the timer.	R	0
26:24	NTP	Number of transmit packets. Controls the maximum number of the frames transmitted before setting the CSR5.TI (Transmit Interrupt) bit. The transmit counter is enabled when written with nonzero value. It is decremented after every frame transmitted. It is reloaded after setting the CSR5.TI (Transmit Interrupt) bit Writing '0' to this field disables the counter effect on the transmit interrupt mitigation mechanism. Reading this field gives the actual count value of the counter.	R	0
23:20	RT	Receive timer.	RW	0

		Controls the maximum time that must elapse between the end of a receive operation and setting the CSR5.RI (Receive Interrupt) bit. This time is equal to RT * CS. The receive timer is enabled when written with nonzero value. After each frame reception the timer starts to count down if it has not already started. It is reloaded after every frame received. Writing '0' to this field disables the timer effect on the receive interrupt mitigation mechanism. Reading this field gives the actual count value of the timer.		
19:17	NRP	Number of receive packets. Controls the maximum number of the received frames before setting the CSR5.RI (Receive Interrupt) bit. The receive counter is enabled when written with nonzero value. It is decremented after every frame received. It is reloaded after setting the CSR5.RI (Receive Interrupt) bit. Writing '0' to this field disables the timer effect on the receive interrupt mitigation mechanism. Reading this field gives the actual count value of the counter.	R	0
16	CON	Continuous mode. 1 – general-purpose timer works in continuous mode 0 – general-purpose timer works in one-shot mode	R	0
15:0	TIM	Timer value. Contains the number of iterations of the general-purpose timer. Each iteration duration is MII 100Mb mode – 81.92us MII 10Mb mode – 819.2us	RW	0

26.5.13 MAC_CSR16

MAC address low register CSR16*
Offset = 0x0080
Note: The CSR16 is optional register and is implemented only in the version of MAC-1G/MAC core that supports flow control.

Bit	Name	Description	Access	Reset
31:24	MAL1	MAC address low 4th bytes. This field contains the bytes of the MAC hardware address (MAL(31:24) = MAC(31:24)). This field is used to fill the source hardware address field of pause frames generated by host.	R	0xFD
23:0	MAL0	MAC address low three bytes. This field contains 3 lowest bytes of the MAC hardware address (MAL(23:0) = MAC(23:0)). This field is used to fill the source hardware address field of pause frames generated by host.	RW	0x0

26.5.14 MAC_CSR17

MAC address high register CSR17*
Offset = 0x0088
Note: The CSR17 is optional register and is implemented only in the version of MAC-1G/MAC core that supports flow control.

Bit	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	MAH	MAC address high bytes. This field contains 2 highest bytes of the MAC hardware address (MAH(15:0) = MAC(47:32)). This field is used to fill the source hardware address field of pause frames generated by host.	R	0xF44E

26.5.15 MAC_CSR18

Pause time & cache thresholds register CSR18*
Offset = 0x0090
Note: The CSR18 is optional register and is implemented only in the version of MAC-1G/MAC core that supports flow control.

Bit	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:24	CPTL	Cache pause threshold level. The filed contains unsigned value indicating the minimum number of frames stored in the receive FIFO when the flow control mechanism starts to transmit pause frames. The actual width of the field depends of RCACHE_DEPTH parameter and a maximum value is RCACHE_DEPTH-1 (the significant bits are from 24 to 23+RCACHE_DEPTH). Writing a value less than in a CRTL field or 0 disables the flow control reactions on frame cash overflow:	RW	0
23:21	-	Reserved	-	-
20:16	CRTL	Cache restart threshold level. The filed contains unsigned value indicating the maximum number of frames stored in the receive FIFO below which the flow control mechanism stops to transmit pause frames. The actual width of the field depends of RCACHE_DEPTH parameter and a maximum value is RCACHE_DEPTH-1 (the significant bits are from 16 to 15+RCACHE_DEPTH). Writing a value larger than in a CPTL field or 0 disables the flow control reactions on frame cash overflow.	RW	0
15:0	PQT	Flow control pause quanta time. This field is used to fill the pause_time field of outgoing flow-control pause frames. The PQT contains 2-octet long unsigned integer indicating the length of time for which the receiving station	RW	0

		will be requested to inhibit next data frame transmission The pause_time is measured in units of pause_quanta, equal to 512 bit times of the particular implementation (10/100/1000(*1G only). Mbit/s) The range of possible pause_time is 0 to 65535 pause_quanta. Writing a value of 0 disables the flow control protocol.		

26.5.16 MAC_CSR19

FIFO thresholds register CSR19*
Offset = 0x0098
Note: The CSR19 is optional register and is implemented only in the version of MAC-1G/MAC core that supports flow control.

Bit	Name	Description	Access	Reset
31:16	FPTL	FIFO pause threshold level. The filed contains unsigned value indicating the minimum number of bytes stored in the receive FIFO when the flow control mechanism starts to transmit pause frames. The actual width of the field depends of RFIFO_DEPTH parameter and a maximum value is RFIFO_DEPTH-1 (the significant bits are from 16 to 15+RFIFO_DEPTH). Writing a value less than in a FRTL field or 0 disables the flow control reactions on FIFO overflow.	RW	0
15:0	FRTL	FIFO restart threshold level. The filed contains unsigned value indicating the maximum number of bytes stored in the receive FIFO below which the flow control mechanism stops to transmit pause frames. The actual width of the field depends of RFIFO_DEPTH parameter and a maximum value is RFIFO_DEPTH -1 (the significant bits are from 0 to RFIFO_DEPTH-1). Writing a value larger than in a FPTL field or 0 disables the flow control reactions on frame cash overflow.	RW	0

26.5.17 MAC_CSR20

Flow control setup & status CSR20*
Offset = 0x00A0
Note: The CSR20 is optional register and is implemented only in the version of MAC-1G/MAC core that supports flow control.

Bit	Name	Description	Access	Reset
31	FCE	Flow Control Enable Writing this bit with 1 enables all full and half-duplex flow control modules. The functionality of full-duplex flow control can be configured with TUE, TPE and RPE bits. The functionality of half-duplex flow control (back pressure) can be	RW	0

		configured with BPE bit.		
30	TUE	Transmit Un-pause frames Enable Writing this bit with 1 enables the transmission of pause frames with 0 pause time when the FIFO is almost empty (below the programmable threshold levels).	RW	0
29	TPE	Transmit Pause frames Enable Writing this field with 1 enables the transmission of pause frames with when the FIFO is near overflow (above the programmable threshold levels).	RW	1
28	RPE	Receive Pause frames Enable. Setting this bit with 1 enables the reception of pause frames and delaying the transmissions.	RW	1
27	BPE	Back pressure (half-duplex flow control) enable.	RW	0
26:2	-	Reserved	-	-
1	PRS	Pause Request Sent (Read only). When read as “1” indicates that the MAC-1G/MAC has sent a pause frame; otherwise read as “0”.	R	0
0	HTP	Host Transmission Paused (Read only). When read as “1” indicates that the MAC-1G/MAC is now delaying the transmission of the next frame according to the received pause frame; otherwise read as “0”.	R	0

26.5.18 SC0~126

Note: The statistical counters are optional registers and are implemented only in the version of MAC-1G/MAC core that supports statistical counters.
Statistical counters relieve the host and software drivers of the responsibility of maintaining statistics for managed Ethernet port. They are wrap-around counters, so after reaching maximum value of 2^{32} they wrap to 0 and continue counting. It is important for the software to read the statistical counters frequently enough to avoid missing the counter overflow. When read, the counter value resets to 0. The counters are physically implemented inside on-chip DP-RAM. They are undefined after hardware reset. This means that the software should read every counter after power-up, before starting the receive and the transmit processes, in order to clear every counter.
Receive descriptor buffer address 2 fields.
Offset = 0x0200

Bit	Name	Description	Access	Reset
31:0	SC	Statistical Couter	RW	0x0

Offset = 0x0200~0x2F8
The receive statistical counters (SC00-SC31)

Symbol	Name	Address	Function
SC00	Rx64	0x200	Counter incremented for each received frame which contains exactly 64 octets.
SC01	Rx65to127	0x208	Counter incremented for each received frame which contains 65 to 127 octets.
SC02	Rx128to255	0x210	Counter incremented for each received frame which contains 128 to 255 octets.
SC03	Rx256to511	0x218	Counter incremented for each received frame which contains 256 to 511 octets.
SC04	Rx512to1023	0x220	Counter incremented for each received frame which contains 512 to 1023 octets.

SC05	Rx1024to1518	0x228	Counter incremented for each received frame which contains 1024 to 1518 octets.
SC06	RXTooLong	0x230	Counter incremented for each received frame which contains more than 1518 octets.
SC07	-	0x238	-
SC08	RxOctOK	0x240	This counter is incremented by the number of octets received after each successfully received frame. The frame byte count includes addresses, type, data and FCS field.
SC09	RxUniOK	0x248	This counter is incremented for each unicast frame successfully received.
SC10	RxMultiOK	0x250	Counter incremented for each successfully received packet with multicast address that is not broadcast address.
SC11	RxBroadOK	0x258	This counter is incremented for each broadcast frame successfully received.
SC12	RxPauseOK	0x260	This counter is incremented for each successfully received MAC control PAUSE frame.
SC13	RxAlignErr	0x268	Counter incremented for each frame that contains non integral number of octets (dribbling bit) and does not pass the FCS check.
SC14	RxFCSErr	0x270	Counter incremented for each frame that contains an integral number of octets and does not pass the FCS check.
SC15	RxMIIErr	0x278	Counter incremented for each frame that experienced an MII error during reception (RXER asserted on GMII**(*1G only)**/MII).
SC16-SC31	-	0x280-0x2F8	Unimplemented. Reserved for future use.

Offset = 0x0300~0x3F8

The transmit statistical counters (SC32-SC63)

Symbol	Name	Address	Function
SC32	Tx64	0x300	Counter incremented for each frame which contains exactly 64 octets.
SC33	Tx65to127	0x308	Counter incremented for each transmitted frame which contains 65 to 127 octets.
SC34	Tx128to255	0x310	Counter incremented for each transmitted frame which contains 128 to 255 octets.
SC35	Tx256to511	0x318	Counter incremented for each transmitted frame which contains 256 to 511 octets.
SC36	Tx512to1023	0x320	Counter incremented for each transmitted frame which contains 512 to 1023 octets.
SC37	Tx1024to1518	0x328	Counter incremented for each transmitted frame which contains 1024 to 1518 octets.
SC38	-	0x330	-
SC39	-	0x338	-

SC40	TxOctOK	0x340	This counter is incremented by the number of octets transmitted after each successfully transmitted frame. The frame byte count includes addresses, type, data and FCS field.
SC41	TxUniOK	0x348	This counter is incremented for each unicast frame successfully transmitted.
SC42	TxMultiOK	0x350	Counter incremented for each successfully transmitted packet with multicast address that is not broadcast address.
SC43	TxBroadOK	0x358	This counter is incremented for each broadcast frame successfully transmitted.
SC44	TxPauseOK	0x360	This counter is incremented for each successfully transmitted MAC control PAUSE frame.
SC45	TXColl0	0x368	The number of frames successfully transmitted which experienced no collision.
SC46	TXColl1	0x370	The number of frames successfully transmitted which experienced single collision.
SC47	TXCollMulti	0x378	The number of frames successfully transmitted which experienced multiple (2-15) collisions.
SC48	TxDefer	0x380	This counter is incremented for each successfully transmitted frame with no collision, which is experienced delay because of medium busy state.
SC49	TxExColl	0x388	This counter is incremented for each transmission aborted after experiencing 16 in-window collisions.
SC50	TxLCErr	0x390	This counter is incremented for each frame which experienced a late collision.
SC51	TxCSErr	0x398	This counter is incremented for each frame, which experienced no carrier sense or dropped carrier sense during transmission.
SC52	TxMACErr	0x3A0	This counter is incremented for each frame aborted due to the FIFO underrun condition. If this counter is incremented, none of the remaining error counters is incremented.
SC53-SC63	-	0x3A8-0x3F8	Unimplemented. Reserved for future use.

26.5.19 MAC_CTRL

Receive descriptor buffer address 2 field
Offset = 0x00B0

Bit	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	RRSB	RMII_REFCLK select bit 0: use internal 125M/50M clock and RMII_REFCLK output this clock to PHY 1: use external 125M/50M clock, RMII_REFCLK is input	RW	0x0
7:4	SSDC	SMII SYNC delay cycle 0000: no delay 0001: 1 half cycle 0010: 2 half cycle 0011: 3 half cycle	RW	0x0

		0100: 4 half cycle 0101: 5 half cycle 0110: 6 half cycle 0111: 7 half cycle 1000: 8 half cycle 1001~1111: Reserved		
3:2	-	Reserved	-	-
1	RCPS	REF_CLK phase select 0: normal phase 1: inverter phase	RW	0x0
0	RSIS	RMII or SMII interface select bit 0: RMII 1: SMII	RW	0x0

26.5.20 Receive Decriptors

Each receive descriptor consist of 4 32-bit fields named RDES0, RDES1, RDES2 and RDES3 .The receive descriptor fields are described below. The BASE address is the position of the descriptor in receive descriptor list

Field Name	Offset	Description
RDES0	0x0000	Receive descriptor status field
RDES1	0x0004	Receive descriptor control and count field
RDES2	0x0008	Receive descriptor buffer address 1 field
RDES3	0x000c	Receive descriptor buffer address 2 field

26.5.21 RDES0

Receive descriptor status field
Offset = 0x0000

Bits	Name	Description	Access	Reset
RDES0.31	OWN	Ownership bit. 1 – the MAC AHB owns the descriptor. 0 – the host owns the descriptor. The MAC AHB will clear this bit when it completes a current frame reception, or when the data buffers associated with a given descriptor are already full.	RW	X
RDES0.30	FF	Filtering fail. When set, indicates that a received frame did not pass the address recognition process. This bit is valid only for the last descriptor of the frame (RDES0.8 set), when the CSR6.30 (receive all) bit is set, and the frame is at least 64 bytes long.	RW	X
RDES0.(29:16).	FL	Frame length. Indicates the length, in bytes, of the data transferred into a host memory for a given frame. This bit is valid only when the RDES0.8 (last descriptor) is set and RDES0.14 (descriptor error) is cleared.	RW	X

RDES0.15	ES	Error summary. This bit is logical or over following bits: RDES0.1 – CRC error. RDES0.6 – Collision seen. RDES0.7 – Frame too long. RDES0.11 – Runt frame. RDES0.14 – Descriptor error. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.14	DE	Descriptor error. Set by the MAC AHB when no receive buffer was available when trying to store the received data. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.11	RF	Runt frame. When set, indicates that the frame is damaged by a collision or by a premature termination before the end of a collision window. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.10	MF	Multicast frame. When set, indicates that the frame has a multicast address. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.9	FS	First descriptor. When set, indicates that this is the first descriptor of a frame.	RW	X
RDES0.8	LS	Last descriptor. When set, indicates that this is the last descriptor of a frame.	RW	X
RDES0.7	TL	Frame too long. When set, indicates that a current frame is longer than the maximum size of 1518 bytes, as specified by 802.3. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.6	CS	Collision seen. When set, indicates that a late collision was seen (collision after 64 bytes following SFD). This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.5	FT	Frame type. When set, indicates that the frame has the length field greater then 1500 (Ethernet type frame). When cleared, indicates the 802.3 type frame. This bit is valid only when the RDES0.8 (last descriptor) is set. Additionally, the FT is invalid for the runt frames of a length shorter then 14 bytes.	RW	X
RDES0.3	RE	Report on MII error. When set, indicates that an error has been detected by a physical layer chip connected through the MII interface. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X

RDES0.2	DB	Dribbling bit. When set, indicates that the frame was not byte aligned. This bit is valid only when the RDES0.8 (last descriptor) is set.	RW	X
RDES0.1	CE	CRC error. When set, indicates that the CRC error has occurred in the received frame. This bit is valid only when the RDES0.8 (last descriptor) is set. Additionally, the CE is not valid when the received frame is a runt frame.	RW	X
RDES0.0	ZERO	This bit is reset for the frames with the legal length.	RW	x

26.5.22 RDES1

Receive descriptor control and count field
Offset = 0x0004

Bits	Name	Description	Access	Reset
RDES1.25	RER	Receive end of ring. When set, indicates that this is the last descriptor in the receive descriptor ring. The MAC AHB returns to the first descriptor in the ring, as specified by the CSR3 (Start of receive list address).	RW	X
RDES1.24	RCH	Second address chained. When set, indicates that the second buffer's address points to the next descriptor and not to the data buffer. Note that the RER takes precedence over the RCH.	RW	X
RDES1.(21:11)	RBS2	Buffer 2 size. Indicates size, in bytes, of memory space used by the second data buffer. This number must be a multiple of 4. If it is 0, then the MAC AHB ignores the second data buffer and fetches the next data descriptor. This number is valid only when the RDES1.24 (Second address chained) is cleared.	RW	X
RDES1.(10:0)	RBS1	Buffer 1 size. Indicates the size, in bytes, of memory space used by the first data buffer. This number must be a multiple of 4. If it is 0, then the MAC AHB ignores the first data buffer and uses the second data buffer.	RW	x

26.5.23 RDES2

Receive descriptor buffer address 1 field
Offset = 0x0008

Bits	Name	Description	Access	Reset

RDES2.(31:0)	RBA1	Receive buffer 1 address. It Indicates the address of memory allocated for the first receive buffer. This number must be longword aligned (RDES2.1:0 = 00).	RW	x

26.5.24 RDES3

Receive descriptor buffer address 2 fields
Offset = 0x000c

Bits	Name	Description	Access	Reset
RDES2.(31:0)	RBA1	Receive buffer 1 address. It Indicates the address of memory allocated for the first receive buffer. This number must be longword aligned (RDES2.1:0 = 00).	RW	x

26.5.25 Transmit descriptors

Each transmit descriptor consist of 4 32-bit fields named TDES0, TDES1, TDES2 and TDES3 .The receive descriptor fields are described below. The BASE address is the position of the descriptor in transmit descriptor list

Field Name	Offset	Description
TDES0	0x0000	Transmit descriptor status field
TDES1	0x0004	Transmit Transmit descriptor control and count field
TDES2	0x0008	Transmit descriptor buffer address 1 field
TDES3	0x000c	Transmit descriptor buffer address 2 field

26.5.26 TDES0

Transmit descriptor status field
Offset = 0x0000

Bits	Name	Description	Access	Reset
TDES0.31	OWN	Ownership bit. 1 – the MAC AHB owns the descriptor. 0 – the host owns the descriptor. The MAC AHB will clear this bit when it completes a current frame transmission or when the data buffers associated with a given descriptor are empty.	RW	x
TDES0.15	ES	Error summary. This bit is a logical or of the following bits: TDES0.1 – Underflow error. TDES0.8 – Excessive collision error. TDES0.9 – Late collision. TDES0.10 – No carrier. TDES0.11 – Loss of carrier. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X
TDES0.11	LO	Loss of carrier. When set, indicates a loss of the carrier during a	RW	X

		transmission. This bit is valid only when TDES1.30 (last descriptor) is set.		
TDES0.10	NC	No carrier. When set, indicates that the carrier was not asserted by an external transceiver during the transmission. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X
TDES0.9	LC	Late collision. When set, indicates that a collision was detected after transmitting 64 bytes. This bit is not valid when TDES0.1 (underflow error) is set. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X
TDES0.8	EC	Excessive collisions. When set, indicates that the transmission was aborted after 16 retries. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X
TDES0.(6:3)	CC	Collision count. This field indicates the number of collisions that occurred before the end of a frame transmission. This value is not valid when TDES0.8 (Excessive collisions bit) is set. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X
TDES0.1	UF	Underflow error. When set, indicates that the FIFO was empty during the frame transmission. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X
TDES0.0	DE	Deferred. When set, indicates that the frame was deferred before transmission. Deferring occurs if the carrier is detected when the transmission is ready to start. This bit is valid only when TDES1.30 (last descriptor) is set.	RW	X

26.5.27 TDES1

Transmit Transmit descriptor control and count field
Offset = 0x0004

Bits	Name	Description	Access	Reset
TDES1.31	IC	Interrupt on completion. Setting this flag instructs the MAC AHB to set CSR5.0 (transmit interrupt) immediately after processing a current frame. This bit is valid when TDES1.30 (last descriptor) is set, or for a setup packet.	RW	X
TDES1.30	LS	Last descriptor. When set, indicates the last descriptor of the frame.	RW	X
TDES1.29	FS	First descriptor. When set, indicates the first descriptor of the frame.	RW	X
TDES1.28	FT1	Filtering type.	RW	X

		This bit together with TDES1.22 (FT0) controls a current filtering mode. This bit is valid only for the setup frames.		
TDES1.27	SET	Setup packet. When set, indicates that this is a setup frame descriptor.	RW	X
TDES1.26	AC	Add CRC disable. When set, the MAC AHB does not append the CRC value at the end of the frame. The exception is when the frame is shorter than 64 bytes and automatic byte padding is enabled. In that case the CRC field is added despite the state of the AC flag.	RW	X
TDES1.25	TER	Transmit end of ring. When set, indicates the last descriptor in the descriptors ring.	RW	X
TDES1.24	TCH	Second address chained. When set, indicates that the second descriptor's address points to the next descriptor and not to the data buffer. This bit is valid only when TDES1.25 (transmit end of ring) is reset.	RW	X
TDES1.23	DPD	Disabled padding. When set, automatic byte padding is disabled. The MAC AHB normally appends the PAD field after the INFO field when the size of a frame is less then 64 bytes. After padding bytes, the CRC field is also inserted regardless of the state of the AC flag. When the DPD is set, no padding bytes are appended.	RW	X
TDES1.22	FT0	Filtering type. This bit together with TDES1.28 (FT1), controls the current filtering mode. This bit is valid only when TDES1.27 (SET) bit is set.	RW	X
TDES1.(21:11)	TBS2	Buffer 2 size. Indicates the size, in bytes, of memory space used by the second data buffer. If it is zero, the MAC AHB ignores the second data buffer and fetches the next data descriptor. This bit is valid only when TDES1.24 (second address chained) is cleared.	RW	X
TDES1.(10:0)	TBS1	Buffer 1 size. Indicates the size, in bytes, of memory space used by the first data buffer. If it is 0, the MAC AHB ignores the first data buffer and uses the second data buffer.	RW	X

26.5.28 TDES2

Transmit descriptor buffer address 1 field
Offset = 0x0008

Bits	Name	Description	Access	Reset

TDES2.(31:0)	TBA1	Transmit buffer 1 address. Contains the address of the first data buffer. For the setup frame this address must be longword aligned (TDES3.1:0 = 00). In all other cases there are no restrictions on buffer alignment.	RW	X

26.5.29 TDES3

Transmit descriptor buffer address 2 field Offset = 0x000c

Bits	Name	Description	Access	Reset
TDES3.(31:0)	TBA2	Transmit buffer 2 address. Contains the address of the second data buffer. There are no restrictions on buffer alignment.	RW	X

26.6 Application Note

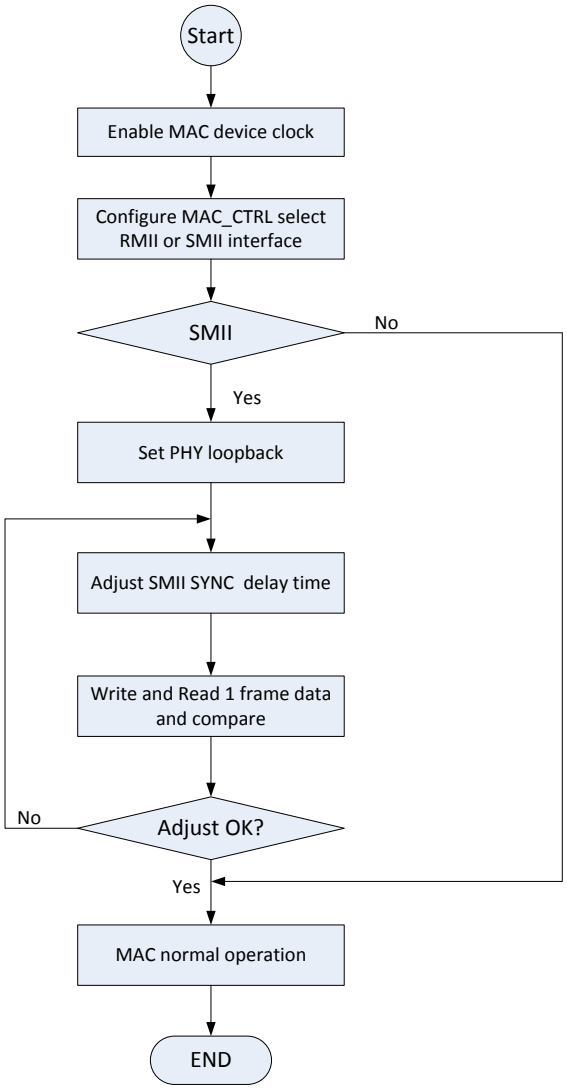


Figure 26-3 MAC and PHY Software initiate operation flow

27 SPI (Serial Peripheral Interface)

27.1 Overview

SPI (Serial Peripheral Interface) is a four wire, master-slave, full-duplex serial communication protocol. S500 integrated 4 SPI modules, the 4 channels can be configured as either a master or slave device. Features of SPI interface are listed below.

- Support master mode and slave mode. The speed of master mode up to 60Mbps, and slaver up to 20Mbps.
- Support dual I/O write and read mode while use as master
- Support single data rate mode and double data rate(DDR mode) while use as master
- Support two wire mode, only use SCLK and MOSI signal
- Support IRQ and DMA mode to transmit data
- Support system program boot from SPI nor-flash
- 4 SPI modules

27.2 Bclock Diagram

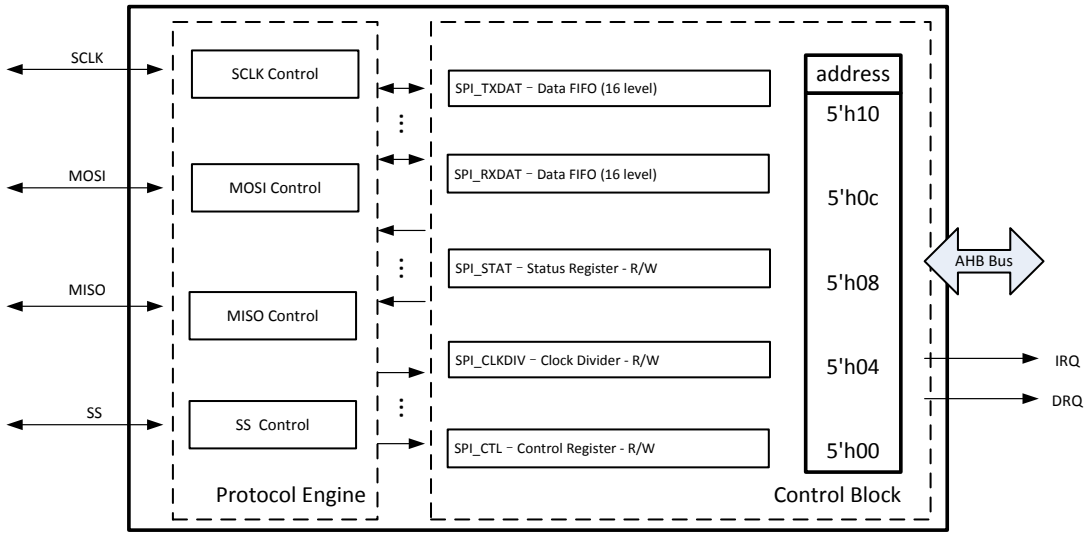


Figure 27-1 SPI Block Diagram

27.3 Function Description

S500 SPI module has 4 channels, which can be configured as either a master or slave device.
SPI uses a couple parameters called clock polarity (CPOL) and clock phase (CPHA) to determine when data is valid with respect to the clock signal. These must be set on the Master and all the Slaves in order for communication to work. CPOL determines whether the leading edge is defined to be the rising or falling edge of the clock (and vice versa for the trailing edge). CPHA determines whether the leading edge is used for setup or sample (and vice versa for the trailing edge).
This allows the data sufficient hold time. When CKHA = 0, data should become valid when the Slave Select (SS) line goes active. Note that most devices require the SS line to be used when CPHA = 0 to allow proper timing, while SS may be optional when CPHA = 1.
The following table summarizes the standard various settings:

Table 27-1 Standard various settings

CPOL/CPHA	Leading Edge	Trailing Edge	SPI Mode
0/0	Sample, rising	Setup, falling	0
0/1	Setup, rising	Sample, falling	1
1/0	Sample, falling	Setup, rising	2
1/1	Setup, falling	Sample, rising	3

27.4 Timing Diagram

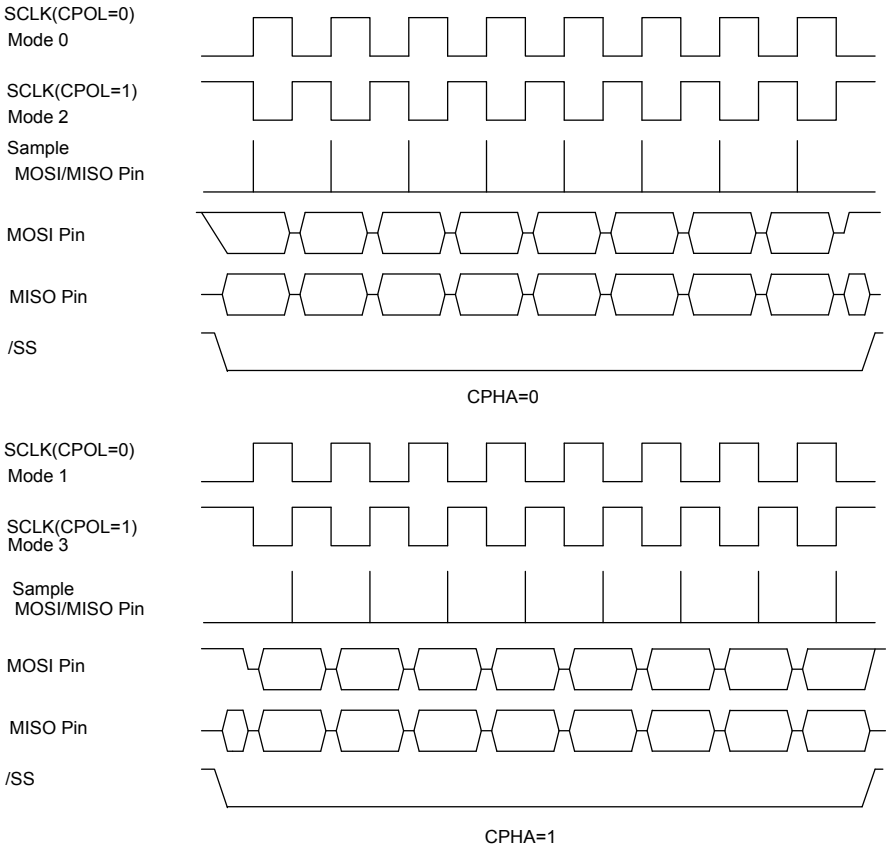


Figure 27-2 SPI working mode timing

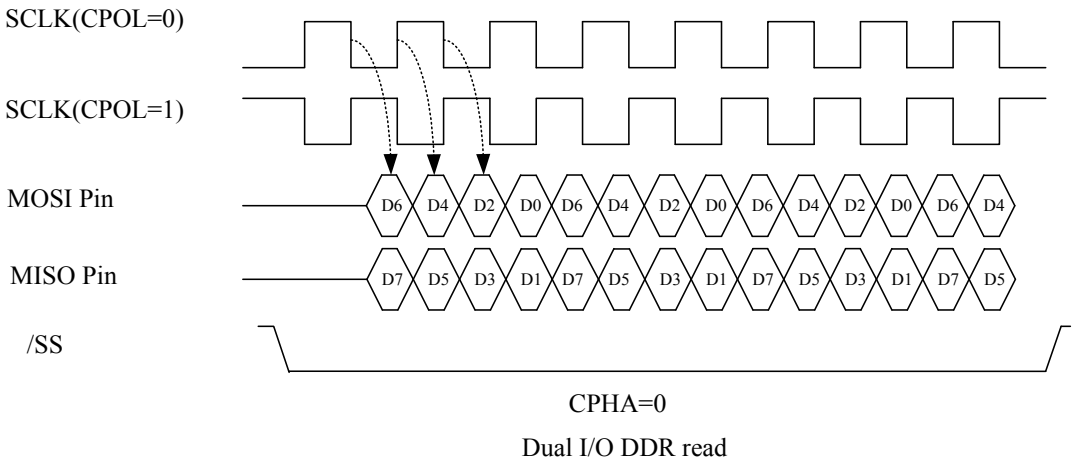


Figure 27-3 Dual I/O DDR read mode

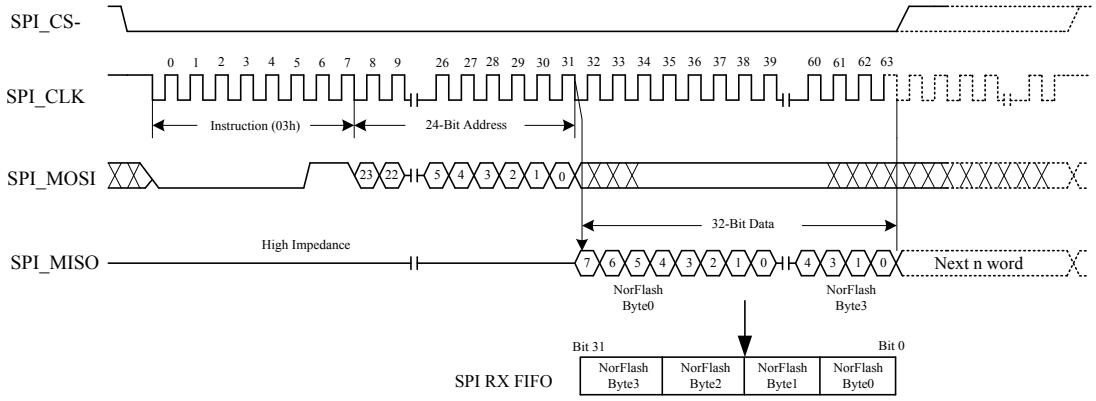


Figure 27-4 SPI NORflash Boot up mode read data timing

After read a word of the SNOR address "Addr", keep SPI_CS low and read continue if the next word address is "Addr+4".

27.5 Register List

Table 27-2 SPI Registers Block Base Address

Name	Physical Base Address
SPI0	0xB0200000
SPI1	0xB0204000
SPI2	0xB0208000
SPI3	0xB020C000

Table 27-3 SPI Registers Offset Address

Offset	Register Name	Description
0x0000	SPIx_CTL	SPI Control Register
0x0004	SPIx_CLKDIV	SPI Clock Divide Register
0x0008	SPIx_STAT	SPI Status Register
0x000C	SPIx_RXDAT	SPI Receive FIFO Data Register
0x0010	SPIx_TXDAT	SPI Transmit FIFO Data Register
0x0014	SPIx_TCNT	SPI Transmit counter for readonly
0x0018	SPIx_SEED	SPI Randomizer seed
0x001C	SPIx_TXCR	SPI TX DMA counter Register
0x0020	SPIx_RXCR	SPI RX DMA counter Register

27.6 Register Description

27.6.1 SPIx_CTL

SPIx Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:29	SDT	Sample delay time 000:No delay 001:Delay 1 HCLK cycle time 010:2 HCLK cycle time 011:3 HCLK cycle time 100:4 HCLK cycle time	RW	0

		101:5 HCLK cycle time 110~111:Reserved		
28	BM	Boot mode, read only. The function is set in srami module. The default value is defined by the status of CE0S pin. 0:normal mode 1:boot mode, the SPI mode is set to MODE3 and the SPI_CLKDIV is set to 0x02 by hardware automatically. Only SPI0 support this function.	R	x
27	GM	GPS mode 0:normal mode 1:GPS mode When select GPS mode, 3 wires and don't care the SPI SS pin.	RW	0
26	CEB	Convert Endian bit 0:not convert Endian 0x76543210 ->0x76543210 1:convert Endian 16bit mode: 0x3210->0x1032 32bit mode: 0x76543210 ->0x10325476 MSB or LSB first shift in or out	RW	0
25	-	Reserved	-	-
24	RANEN	Randomizer enable bit 0:normal (randomizer bypass) 1:randomizer enable Only SPI0 and SPI1 support this function.	RW	0
23:22	RDIC	RX DRQ/IRQ Control. 00:Set when at least one byte received in IRQ mode. 01:Set when 8 level received in IRQ/DRQ mode 10:Set when 16 level received in IRQ/DRQ mode 11:Set when 24 level received in IRQ/DRQ mode In DMA mode, DO not set 00, 01, because at lease 8 level necessary.	RW	0
21:20	TDIC	TX DRQ/IRQ Control. 00:Set when TX FIFO is 1 level empty in IRQ mode. 01:Set when TX FIFO is 8 level empty in IRQ/DRQ mode. 10:Set when TX FIFO is 16 level empty in IRQ/DRQ mode. 11:Set when TX FIFO is 24 level empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01, because at lease 8 level necessary.	RW	0
19	TWME	Two wire mode enable bit 0:Normal 4 wire mode 1:Two wire mode, use two pin, SPI_CLK and SPI_MOSI	RW	0
18	EN	Enable. 0:Disable 1:Enable	RW	0
17:16	RWC	RW control 00:Write and read 01:Write only 10:Read only 11:Reserved	RW	0
15	DTS	Read Start Control Write 1 to start Read clock while use DMA to read data,	RW	0

		available only in master read only mode. When transfer is finished, this bit will be auto cleared		
14	SSATEN	SPI_SS active automatically enable when in mode 0 and mode 2 (CPHA=0), only use in standard mode, except dual and DDR mode. 0:Disable 1:Enable	RW	0
13:12	DM	Dual mode and Double data rate Dual mode:Two data wire to read or write Double data rate:DDR 00:Single data wire and single data rate read or write 01:Dual and single data rate mode 10:Single data wire and DDR mode 11:Dual and DDR mode	RW	0
11	-	Reserved	-	-
10	MS	Master/Slave Select. 0:Master 1:Slave	RW	0
9:8	DAWS	Data/Address Width. Select 00:8 bit data and address, low 8 bit 01:16 bit data and address, low 16bit 10:32 bit data and address 11:Reserved	RW	0
7:6	CPOS	Clock Polarity Select. CPOL CPHA 00:Mode 0 01:Mode 1 10:Mode 2 11:Mode 3	RW	0x3
5	LMFS	LSB/MSB First Select. 0:Transmit and receive MSB first 1:Transmit and receive LSB first	RW	0
4	SSCO	SPI_SS Control Output (only for master mode). 1:Output high 0:Output low.	RW	1
3	TIEN	TX IRQ Enable. 0:Disable 1:Enable	RW	0
2	RIEN	RX IRQ Enable. 0:Disable 1:Enable	RW	0
1	TDEN	TX DRQ Enable. 0:Disable 1:Enable	RW	0
0	RDEN	RX DRQ Enable. 0:Disable 1:Enable	RW	0

27.6.2 SPIx_CLKDIV

SPIx Clock Divide Control Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	CLKDIV	In master mode: SPICLK=HCLK/(CLKDIV*2) While CLKDIV is set to 1, the divide is 2. The SPI clock rate up to 60MHz. In slave mode: Need not to set this register. Supporting SPI clock rate up to 20MHz. When use, this register can not be set to 0	RW	0

27.6.3 SPIx_STAT

SPIx Status Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9	TFEM	TX FIFO Empty. 1:Empty 0:Not Empty	R	1
8	RFFU	RX FIFO Full. 1:Full 0:Not Full	R	0
7	TFFU	TX FIFO Full. 1:Full 0:Not Full	R	0
6	RFEM	RX FIFO Empty. 1:Empty 0:Not Empty	R	1
5	TFER	TX FIFO Error. When overflow, the bit is set to 1. Write 1 to the bit will clear the bit and reset the FIFO.	RW	0
4	RFER	RX FIFO Error. When overflow, the bit is set to 1. Write 1 to the bit will clear the bit and reset the FIFO.	RW	0
3	BEB	Bus error bit. Write 1 to the bit will clear the bit 0:No error 1:Bus error	RW	0
2	TCOM	Transfer Complete Bit. DMA mode:This bit will be set to 1 when all the data sent out or receive over, that the SCK has not clock. CPU mode:This bit will be set to 1 when every byte data sent out or receive over, that the SCK has not clock. Write 1 will clear to zero	RW	0
1	TIP	TX IRQ Pending Bit. 0:No IRQ 1:IRQ Write 1 to the bit will clear it.	RW	0
0	PIP	RX IRQ Pending Bit. 0:No IRQ 1:IRQ Write 1 to this bit will clear it.	RW	0

27.6.4 SPIx_RXDAT

SPIx RXData Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:0	RXDAT	Receive Data. The depth of RXFIFO is 32bit×32 levels.	R	x

27.6.5 SPIx_TXDAT

SPIx TXData Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:0	TXDAT	Transmit Data. The depth of RXFIFO is 32bit×32 levels.	W	x

27.6.6 SPIx_TCNT

SPI transmit counter Register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	TCNT	Transmit counter, use to count the clock that sent out to read data in master mode. In read only mode, must first set this counter to determine how much clocks need to send out. The units of the count depend on the data width set by SPI_CTL. For example, if SPI is set 8bit mode, then each byte count 1. If SPI is set 32bit mode, then each word count 1. This counter only use in read only mode, include CPU and DMA receive	RW	0

27.6.7 SPIx_SEED

SPI Randomizer seed Register
Offset=0x0018

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:0	RS	Randomizer seed	RW	0

27.6.8 SPIx_TXCR

SPI TX DMA counter Register
Offset=0x001C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	TDWC	TX DMA word counter, use to count data Sent by DMA	RW	0

27.6.9 SPIx_RXCR

SPI RX DMA counter Register
Offset=0x0020

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	RDWC	RX DMA word counter, use to count data Received by DMA	RW	0

27.7 Application Note

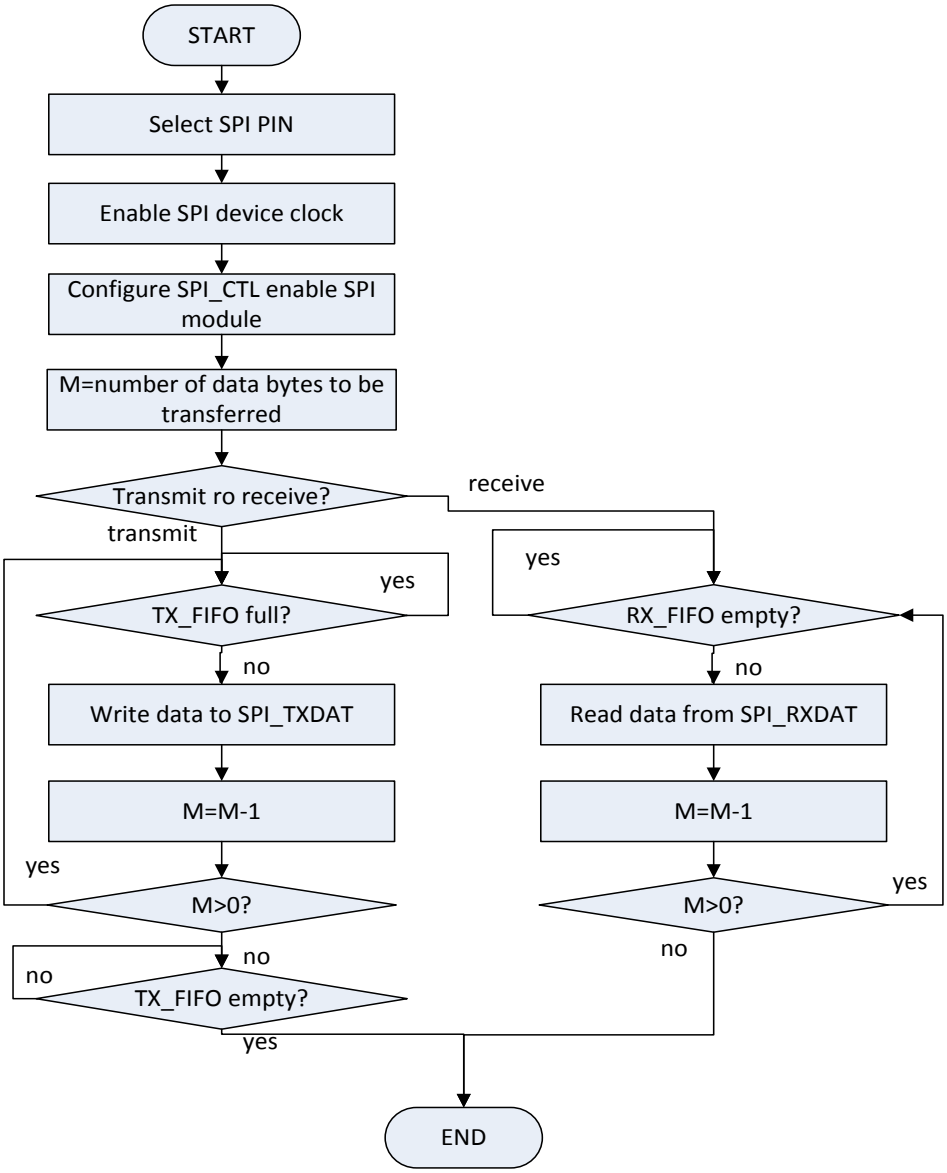


Figure 27-5 SPI writing/reading operating flow

28 UART and IRC

28.1 Overview

This module includes seven UART (Universal Asynchronous Receiver/Transmitter) interfaces. The UART0 interface can be multiplexed for IRC (Infrared Remote Controller), so the IRC has the same IRQ signal as UART0.

Features of UART module is listed below

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 levels Transmit FIFO and 32 levels Receive FIFO
- Capable of speeds up to 3Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data.
- Only UART2\3 support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system

IRC:

- Only UART0 support IRC Inputs
  - Support RC6\RC5\9012\NEC(8bit) protocol.
  - Need to connect an IR receiver when use.
- Support IR Paddle

28.2 Block Diagram

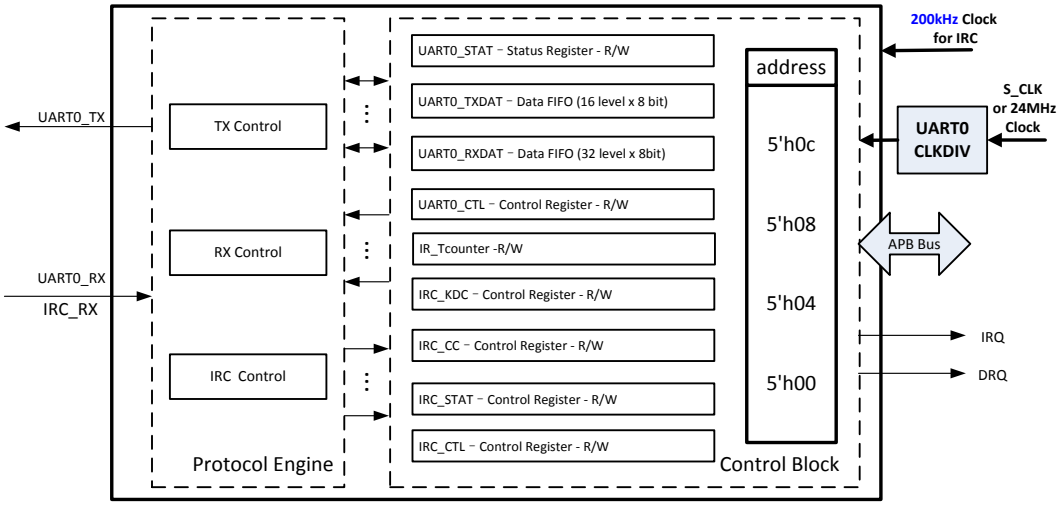


Figure 28-1 UART0 & IR Block Diagram

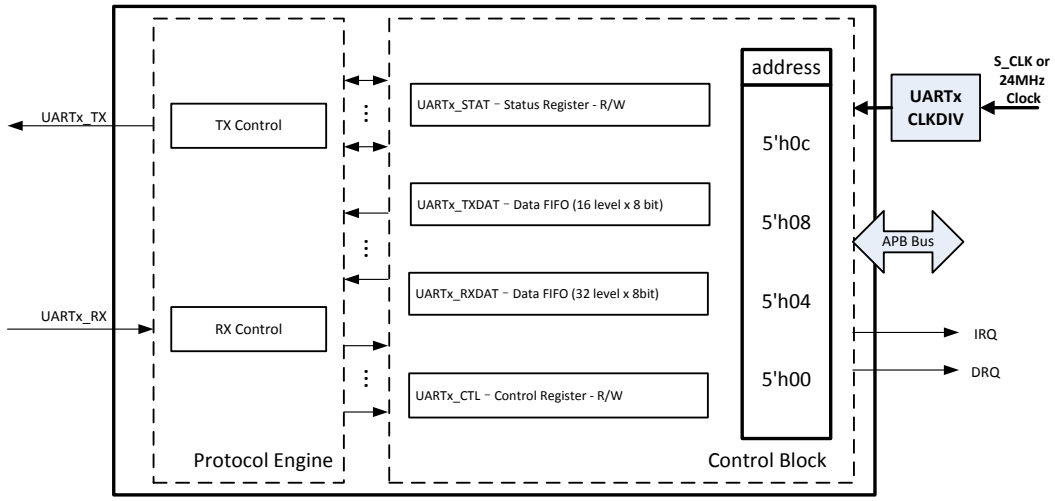


Figure 28-2 UART1\UART4\UART5\UART6 Block Diagram

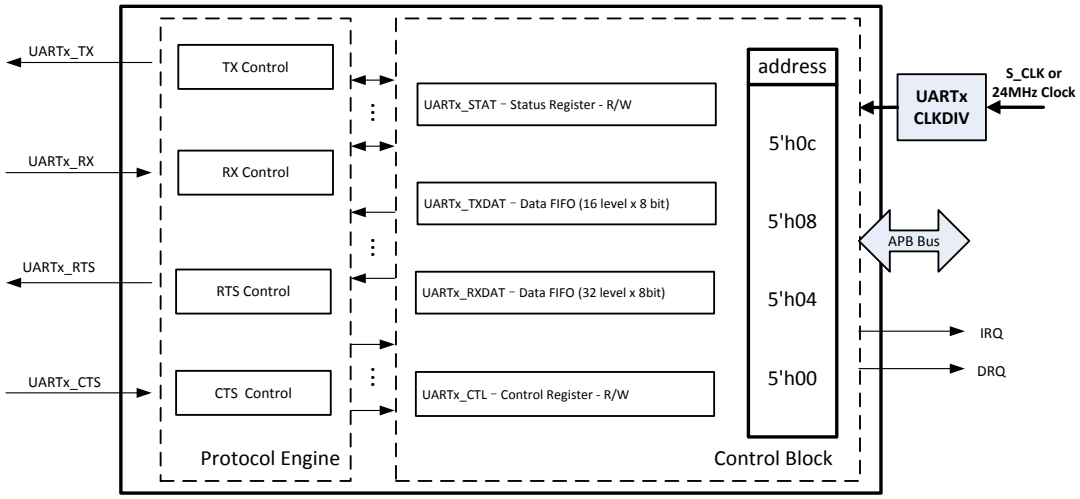


Figure 28-3 UART2\UART3 Block Diagram

28.3 Function Description

28.3.1 Clock Description

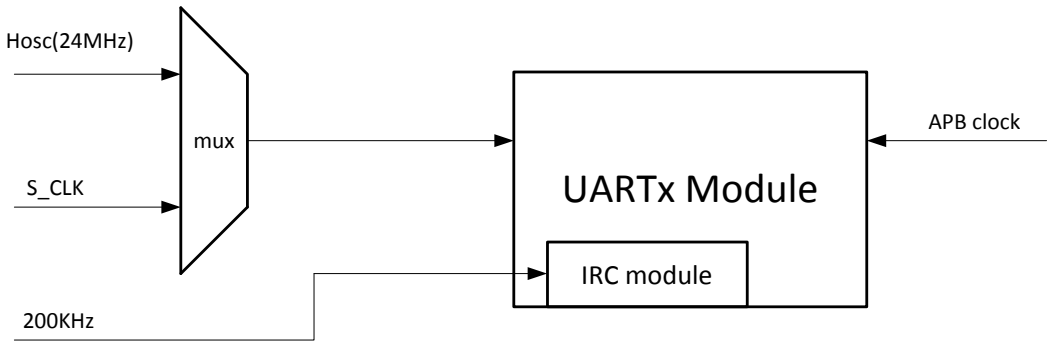


Figure 28-4 Clock for UARTx Module

For UART0 to support IRC function, a 200KHz should be additionally applied.

28.3.2 UART

UART (Universal Asynchronous Receiver/Transmitter) is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UART are now commonly included in microcontrollers.

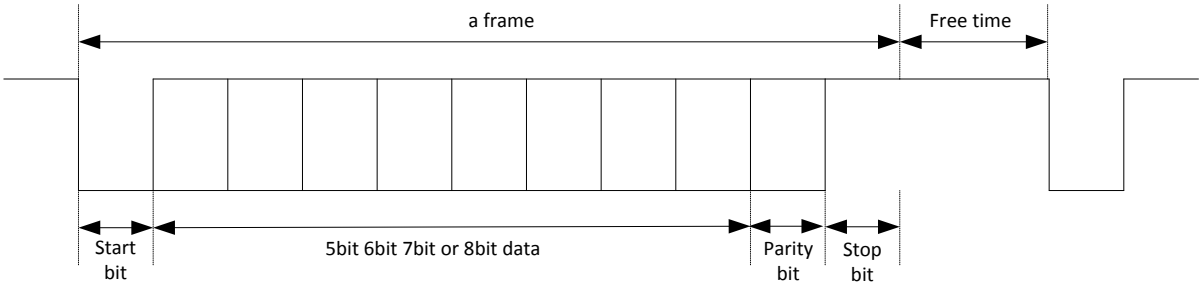


Figure 28-5 UART timing

RTS/CTS hardware Autoflow control flow:
When the receiver FIFO level reaches the trigger level of 28 bytes, RTS- will be pulled up to invalid state. The sending UART may send an additional byte after the trigger level is reached (in case the sending UART has another byte to send) because it may not recognize the invalid state of RTS- until after it has begun sending the additional byte. RTS- is automatically reasserted once the receiver FIFO is emptied by reading the receiver buffer register. The reassertion signals the sending UART to continue transmitting data.

The transmitter checks CTS- before sending the next data byte. When CTS- is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, CTS- must be released before the middle of the last stop bit that is currently being sent.

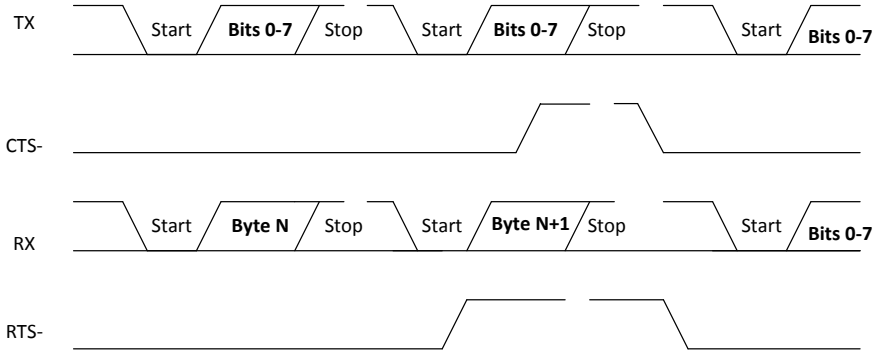


Figure 28-6 RTS/CTS Autoflow control timing

UART Baud Rate:
The UART Baud Rate must be selected by setting the UARTx_CLK_Con Register of the CMU. UARTxBauRate*8=S_CLK/UARTx_CLK_DIV

28.3.3 IRC

28.3.3.1 IRC 9012

The 9012 protocol uses a pulse distance encoding of the bits. Each pulse is one Tm (560µs) long 38kHz carrier burst. A logical "1" takes 4Tm (2.25ms) to transmit, while a logical "0" is only 2Tm (1.12ms). The recommended carrier duty-cycle is 1/4 or 1/3.

Tm=256/Fosc=0.56ms (Fosc=455kHz)
Repetition time=192Tm=108ms
Carrier frequency = Fosc/12

- 8 bit customer code and 8 bit command code length
- customer and command are transmitted twice for reliability
- Pulse distance modulation
- Bit time of 2Tm(1.12ms) for logic “0” or 4Tm (2.25ms) for logic “1”

With this protocol the LSB is transmitted first. In this case Customer code and Command is transmitted. A message is started by 8Tm (4.5ms) AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by 8Tm (4.5ms) space, which is then followed by the Customer code and Command. Customer code and Command are transmitted twice. The second time the command bits are inverted and can be used for verification of the received message.

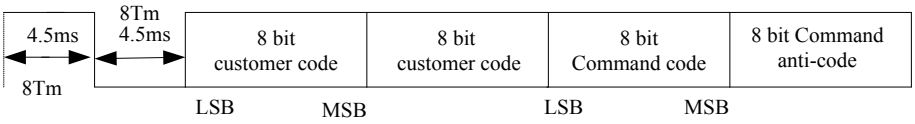


Figure 28-7 IR 9012 Protocol of Frame

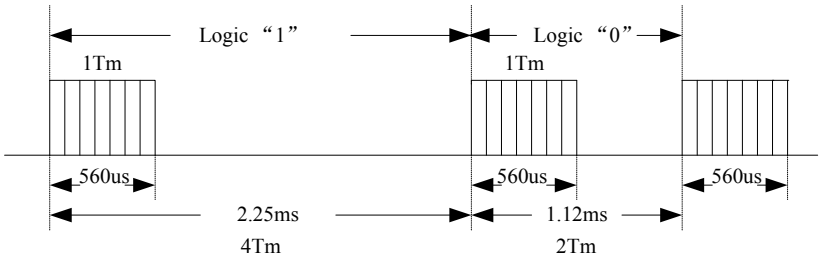


Figure 28-8 IR 9012 Logic transmission

A command is transmitted only once, even when the key on the remote control remains pressed. Every 192Tm a repeat code is transmitted for as long as the key remains down. This repeat code is simply one 8Tm (4.5ms) AGC pulse followed by one 8Tm (4.5ms) space and a logic “1” +1Tm (560µs) burst.

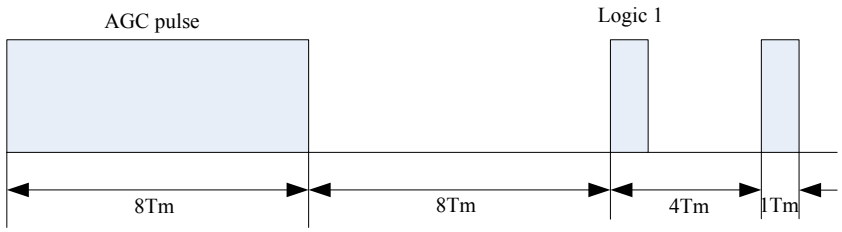


Figure 28-9 9012 Protocol of Repeat Code

28.3.3.2 IRC NEC

The NEC protocol uses a pulse distance encoding of the bits. Each pulse is one Tm (560µs) long 38kHz carrier burst. A logical "1" takes 4Tm (2.25ms) to transmit, while a logical "0" is only 2Tm (1.12ms). The recommended carrier duty-cycle is 1⁄4 or 1⁄3.

Tm=256⁄Fosc=0.56ms (Fosc=455kHz)
Repetition time=192Tm=108ms
Carrier frequency = Fosc/12

- 8 bit customer and 8 bit command length
- customer and command are transmitted twice for reliability
- Pulse distance modulation

- Bit time of 2Tm(1.12ms) for logic “0” or 4Tm (2.25ms) for logic “1”

With this protocol the LSB is transmitted first. In this case Customer code and Command is transmitted. A message is started by 16Tm (9ms) AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by 8Tm (4.5ms) space, which is then followed by the Customer code and Command. Customer code and Command are transmitted twice. The second time all bits are inverted and can be used for verification of the received message. The total transmission time is constant because every bit is repeated with its inverted length.

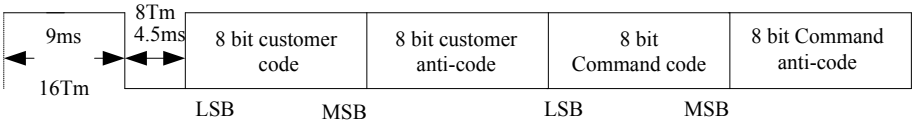


Figure 28-10 NEC Protocol Frame

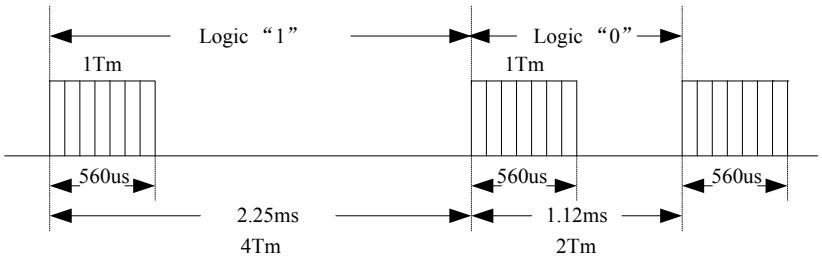


Figure 28-11 NEC Protocol Logic transmission

A command is transmitted only once, even when the key on the remote control remains pressed. Every 192Tm a repeat code is transmitted for as long as the key remains down. This repeat code is simply a 16Tm (9ms) AGC pulse followed by a 4Tm (2.25ms) space and one Tm (560µs) burst.

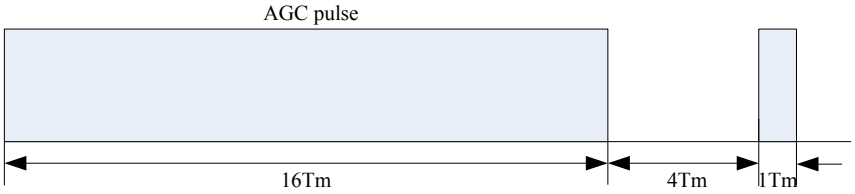


Figure 28-12 NEC Protocol Repeat Code

28.3.3.3 IRC RC5

The protocol uses bi-phase modulation (or so-called Manchester coding) of a 38kHz IR carrier frequency. All bits are of equal length of 1.8ms in this protocol, with half of the bit time filled with a burst of the 38kHz carrier and the other half being idle. A logical zero is represented by a burst in the first half of the bit time. A logical one is represented by a burst in the second half of the bit time. The pulse/pause ratio of the 38kHz carrier frequency is 1⁄3 or 1⁄4, to reduce power consumption.

1 bit-time = 3 x 256 /Fosc= 1.688ms (Fosc=455kHz)
Tm= 1 bit-time/2=0.844ms
Repetition time= 4 x 16 x 2Tm=108ms
Carrier frequency = Fosc/12

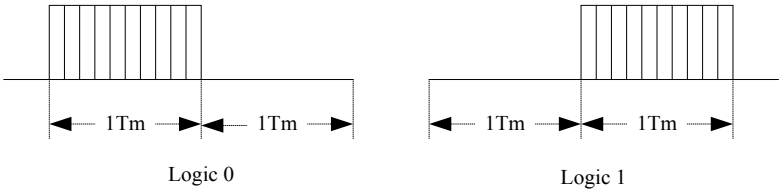


Figure 28-13 RC5 Protocol Logic

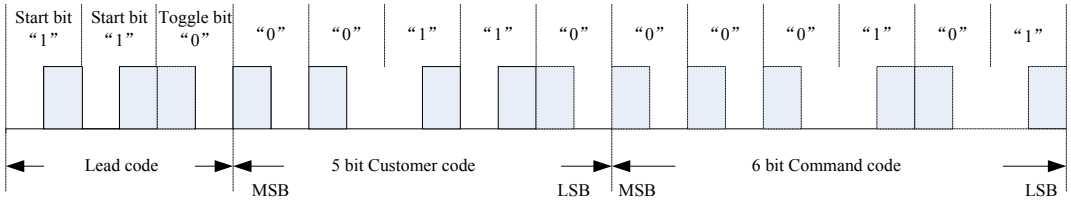


Figure 28-14 RC5 Protocol Frame

The first two pulses are the start pulses, and are both logical "1". Please note that half a bit time is elapsed before the receiver will notice the real start of the message.

The 3d bit is a toggle bit. This bit is inverted every time a key is released and pressed again. This way the receiver can distinguish between a key that remains down, or is pressed repeatedly.

The next 5 bits represent the IR device address, which is sent with MSB first. The address is followed by a 6 bit command, again sent with MSB first.

A message consists of a total of 14 bits, which adds up to a total duration of 28Tm. Sometimes a message may appear to be shorter because the first half of the start bit S1 remains idle. And if the last bit of the message is a logic "0" the last half bit of the message is idle too.

As long as a key remains down the message will be repeated every 128Tm(108ms). The toggle bit will retain the same logical level during all of these repeated messages. It is up to the receiver software to interpret this auto repeat feature.

Figure 28-15 RC5 Protocol of Repetition time

28.3.3.4 IRC RC6

Only support RC6 mode 0.

RC-6 signals are modulated on a 36 kHz Infra Red carrier. The duty cycle of this carrier has to be between 25% and 50%.

Data is modulated using Manchester coding. This means that each bit (or symbol) will have both a mark and space in the output signal. If the symbol is a "1" the first half of the bit time is a mark and the second half is a space. If the symbol is a "0" the first half of the bit time is a space and the second half is a mark.

The main timing unit is 1t, which is 16 times the carrier period (1/36k * 16 = 444µs)

1 T = 1 x 16 /36K= 444us

1Bit= 2T=888us

Transmission time= Total 22 Bits= 23.1 ms (message) + 2.7 ms (no signal)

Repetition time=240T= 106.7ms

LS	SB	mb2 ... mb0	TR	a7 ... a0	c7 .... c0	
Header				Control	Information	Signal free

Figure 28-16 RC6 Protocol

The RC6 Protocol frame can be separated into four fields: Header, Control, Information and Signal free field. The signal free field is not used.

Header Field:

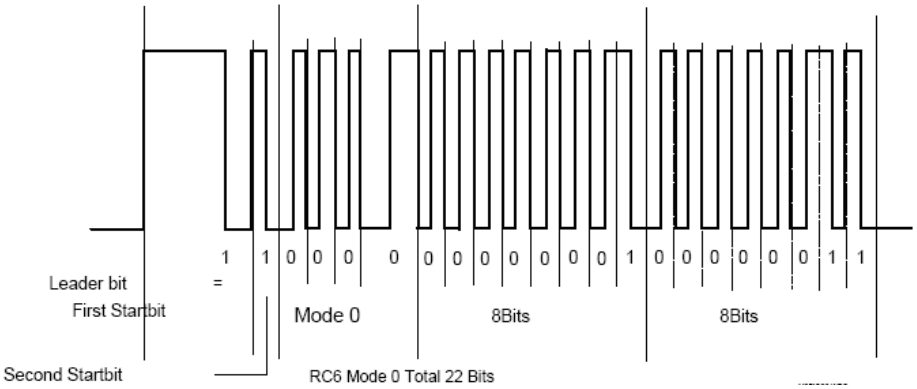


Figure 28-17 RC6 Protocol of Signal Frame

This leader bit is the start bit used to set the gain of the IR receiver unit, which has a mark time of 6T (2.666ms) and a space time of 2T (0.889ms).

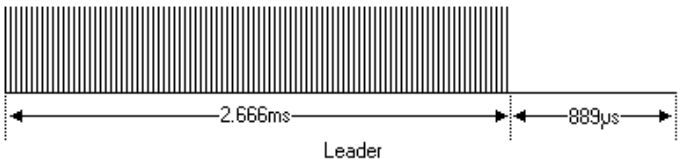


Figure 28-18 RC6 Protocol of Leader Bit

The normal bit, 0 and 1 are encoded by the position of the mark and space in the bit time, in which mark time is1T (0.444ms) and space time is1T (0.444ms).

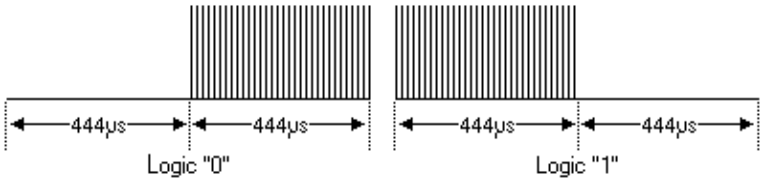


Figure 28-19 RC6 Protocol of Normal Bit

The trailer bit TR has a mark time of 2T (0.889ms) and a space time of 2T (0.889ms). Same, 0 and 1 are encoded by the position of the mark and space in the bit time. This bit functions like the traditional toggle bit, which will be inverted whenever a key is released. This bit separates a long key-press from a double key-press.

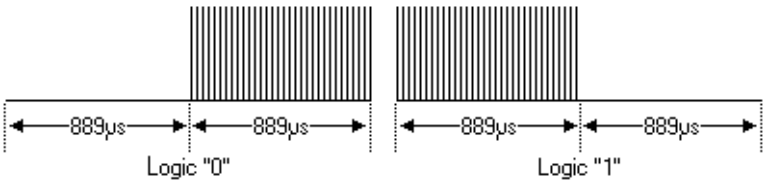


Figure 28-20 RC6 Protocol of Trailer Bit

Control field:

This field holds 8 bits which are used as address byte. This means that a total of 256 different devices can be controlled using mode 0 of RC-6. The MSB is transmitted first.

Information field:

The information field holds 8 bits which are used as command byte. This means that each device can have up to 256 different commands. The MSB is transmitted first.

28.3.3.5 IR Paddle

The infrared remote paddle support 20-bit signal, in which 18-bit are for keys, each bit of the received

18-bit signal represent a key. One bit is for master/slave identification signal, and the last bit is parity check bit.

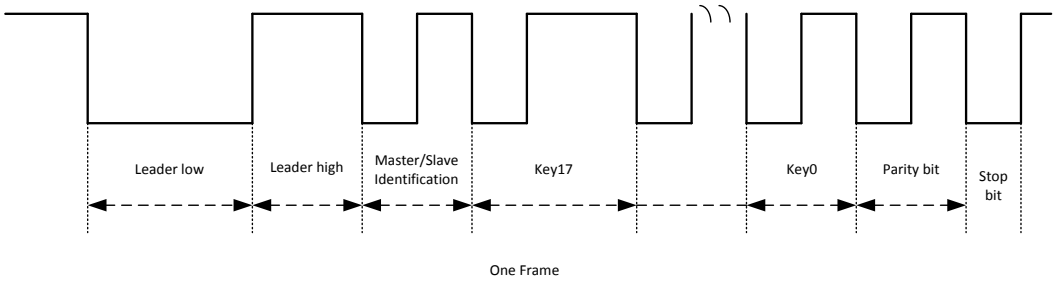


Figure 28-21 IR Receive Timing Sequence

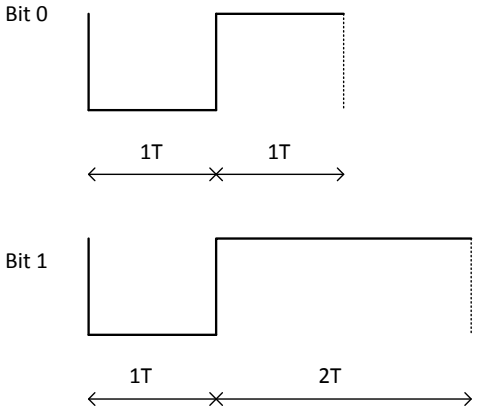


Figure 28-22 Signals from IR Receiver

Note:

1. *the logic of IR receiver and transmitter is logical opposite, i.e. when the transmitter is 1, the receiver is 0.*
2. *T=210us.*

28.4 Register List

Each UART is controlled by a register block.

Table 28-1 UART Registers Block Base Address

Name	Physical Base Address
UART0	0xB0120000
UART1	0xB0122000
UART2	0xB0124000
UART3	0xB0126000
UART4	0xB0128000
UART5	0xB012A000
UART6	0xB012C000
IRC	0xB0120050

Table 28-2 UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register
0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register

0x000c	UARTx_STAT	UART Status Register

Table 28-3 IRC Registers Offset Address

Offset	Register Name	Description
0x00	IR_CTL	Infrared remote control(IRC) interface control register
0x04	IR_STAT	IRC status register
0x08	IR_CC	IRC customer code register
0x0C	IR_KDC	IRC key data code register
0x10	IR_TCOUNTER	IR handle bit width counter
0x14	IR_RCC	The received customer code register, read only

28.5 Register Description

28.5.1 UARTx_CTL

UART Control Register

Offset=0x0000

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	DTCR	DMA TX counter reset Write 1 to this bit will reset UART TX internal DMA transmit counter. Auto clear to 0 while reset over.	RW	0
21	DRCR	DMA RX counter reset Write 1 to this bit will reset UART RX internal DMA transmit counter. Auto clear to 0 while reset over.	RW	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0:Disable 1:Enable	RW	0
19	TXIE	UART TX IRQ Enable. 0:Disable 1:Enable	RW	0
18	RXIE	UART RX IRQ Enable. 0:Disable 1:Enable	RW	0
17	TXDE	UART TX DRQ Enable. 0:Disable 1:Enable	RW	0
16	RXDE	UART RX DRQ Enable. 0:Disable 1:Enable	RW	0
15	EN	UART Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0

14	TRFS	UART TX/RX FIFO Select TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART_STAT Register. 0:RX FIFO 1:TX FIFO	RW	0
13	-	Reserved	R	0
12	AFE	Autoflow Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. This function only used in UART2. UART0 and UART1 not support 4-wire function	RW	0
11:7	-	Reserved	R	0
6:4	PRS	Parity Select. Bit 6:PEN, Parity enable Bit 5:STKP, Stick parity Bit 4:EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	0
3	-	Reserved	R	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	RW	0
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	0

Note:FIFO threshold setting requirement:

1. *TX FIFO (16 layers in total) threshold:*
   a) *IRQ:8 layers empty*
   b) *DRQ:Single mode*
2. *RX FIFO (32 layers in total) threshold:*
   a) *IRQ:16 layers received*
   b) *DRQ:single mode*
3. *When UART TX using DMA mode, after one DMA transmission, UART should write the TFER bit of UARTx_STAT after TX FIFO is empty, and reset the internal TX FIFO, then configure the next DMA transmission.*

28.5.2 UARTx_RXDAT

UART Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×32levels.	R	x

28.5.3 UARTx_TXDAT

UART Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:0	TXDAT	Received Data. The depth of FIFO is 8bit×16 levels	R	x

28.5.4 UARTx_STAT

UART Status Register

Offset=0x000C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0
17	UTBB	UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
16:11	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0
10	TFES	TX FIFO empty Status 1:empty 0:no empty	R	1
9	RFFS	RX FIFO full Status 0:no full 1:full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	x
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1:Full 0:No Full	R	0
5	RFEM	RX FIFO Empty. 1:Empty 0:No Empty	R	1
4	RXST	Receive Status. 0:receive OK 1:receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error. 0:No Error 1:Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	RX FIFO Error. 0:No Error 1:Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0

1	TIP	TX IRQ Pending Bit. 0:No IRQ 1:IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	RX IRQ Pending Bit. 0:No IRQ 1:IRQ Writing 1 to the bit to clear it.	RW	0

28.5.5 IR_CTL

infrared remote control register
Offset=0x00

Bits	Name	Description	Access	Reset
31:5	-	Reserved	R	0
4	IPE	IR Paddle enable 0:disable 1:enable When use IR Paddle, must set IRC enable bit; when this bit is set, other IRC mode is not valid.	RW	0
3	IRCE	IRC enable 0:disable 1:enable	RW	0
2	IIE	IRC IRQ enable 0:disable 1:enable	RW	0
1:0	ICMS	IRC coding mode select 00:9012 code 01:8-bits NEC code 10:RC5 code 11:RC6 code	RW	0

28.5.6 IR_STAT

Infrared remote control register
Offset = 0x04

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	IRFE	IR Receive FIFO empty bit (only use in IR Paddle mode) 0:empty 1:not empty, generate IRQ	R	0
6	UCMP	User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct user code the next time. 0:user code match 1:user code don't match	RW	0
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct key data code the next time 0:key data code match 1:key data code don't match	RW	0
4	RCD	Repeated code detected, write 1 to this bit will clear it, otherwise don't change 0:no repeat code 1:detect repeat code	RW	0

3	-	Reserved	-	-
2	IIP	IRC IRQ pending bit, write 1 to this bit will clear it 0:no IRQ pending 1:IRQ pending The precondition of generating interrupt is all the received code is correct, including user code and key value, moreover, if the user code and key value is not correct, the repeat code reveived following this frame can't generate interrupt. In IR Paddle mode When FIFO is not empty, generate IRQ	RW	0
1	-	Reserved	-	-
0	IREP	IRC receive error pending 0:receive ok 1:receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0

28.5.7 IR_CC

Infrared remote control customer code register
Offset = 0x08

Bit(s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	ICCC	Infrared remote control customer code **In RC5 mode:** Bit 4:0 is the customer code **In 9012 and NEC mode:** Bit 15:0 is the customer code, In RC6 mode: Bit 7:0 is the customer code. **In Paddle mode:** Reserved	RW	0

28.5.8 IR_KDC

Infrared remote control KEY data code register
Offset = 0x0C

Bit(s)	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19:0	IKDC	IRC key data code **In RC5 mode:** Bit 5:0 is the Key data **In 9012 and NEC mode:** Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data **In RC6 mode:** Bit 7:0 is the Key data; If key value is received, register will be updated, if repeat code is received, register won't be updated. **In IR Paddle mode** key data code is 20bit x 8 level RX FIFO	R	0

28.5.9 IR_TCOUNTER

Infrared remote control KEY data code register
Offset = 0x10

Bit(s)	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13:8	ILWC	IR Paddle Leader code width TL counter Determine the length of lead code width TL of infrared game paddle; Determine the number of 200kHz clock source cycles, each cycle is 5μs, 2 cycles (10μs) is a unit here, for example, to set T = 150μs, then 150/10 = 15 should be write here. Default value is 150μs.	RW	0xF
7:6	-	Reserved	-	-
5:0	IBWC	IR Paddle bit width T counter Determine the length of key width T of infrared game paddle; Determine the number of 200kHz clock source cycles, each cycle is 5μs, 2 cycles (10μs) is a unit here, for example, to set T = 210μs, then 210/10 = 21 should be write here. Default value is 210μs	RW	0x15

28.5.10 IR_RCC

Receive customer code register
Offset = 0x14

Bit(s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	ICCC	Received customer code **In RC5 mode:** Bit 4:0 is the customer code **In 9012 and NEC mode:** Bit 15:0 is the customer code, **In RC6 mode:** Bit 7:0 is the customer code, **In Paddle mode:** Reserved The received user code is used to display the received user code for customers' reference	R	0

28.6 Application Note

UART module can transmit data using interrupt, DMA or inquired but the IRC can't use DMA mode. The bellowing is the operation flow using inquired mode to transfer and receive data.

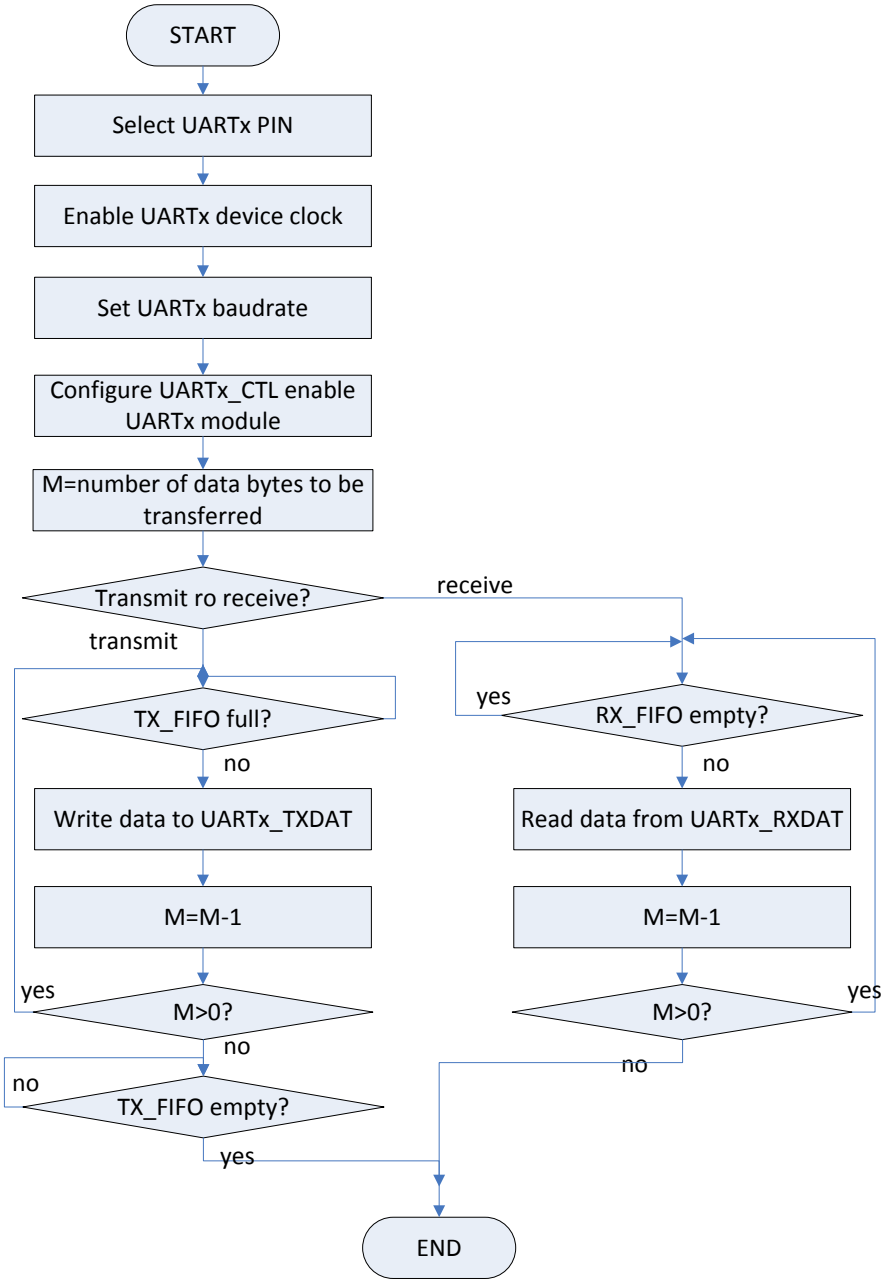


Figure 28-23 UART1 transmit and receive flow

29 TWI (Two Wire Interface)

29.1 Overview

TWI (Two Wire Interface) is used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI. TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

- Both master and slave functions support
- Support standard mode (100kbps), fast-speed mode (400kpbs), High-Speed mode(3.4Mbps)
- Multi-master capability
- 10bit address mode not support
- Internal Pull-Up Resistor (1.5kOhm) optional
- Four TWI modules
- 8Bit x128 TX FIFO and 8Bit x128 RX FIFO

Pull-up resistors are required on both of the TWI signal lines as the TWI drivers are open drain Typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal Pull-Up resistor in standard and fast mode.

HS-mode master devices need a current-source pull-up circuit on the SCLH output. This current-source shortens the rise time of the SCLH signal.

29.2 Block Diagram

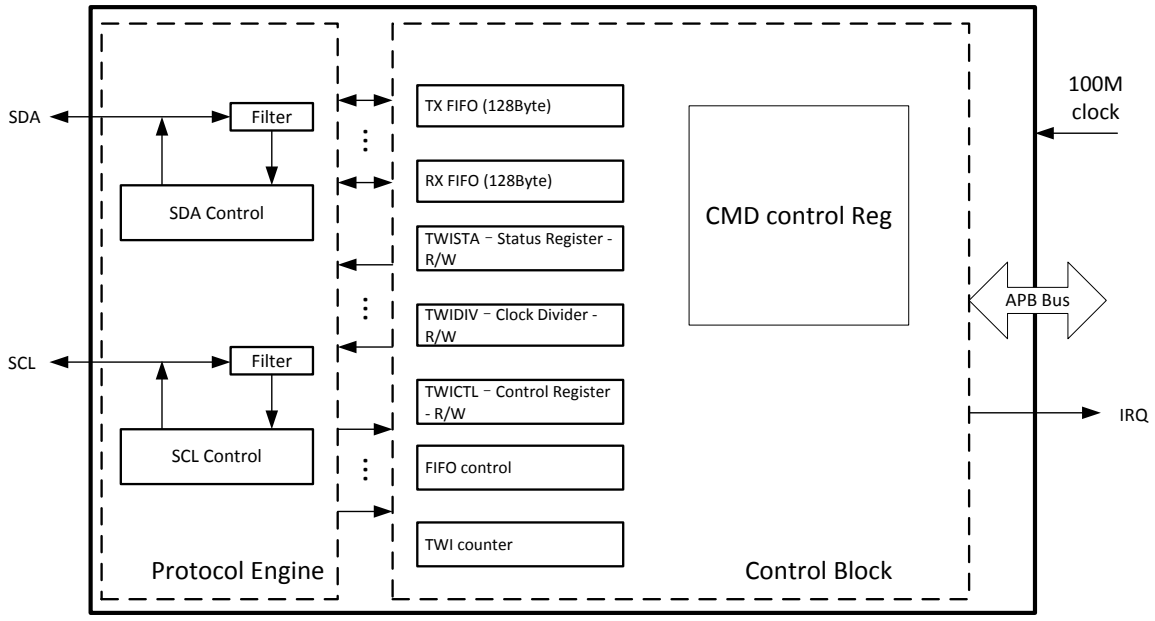


Figure 29-1 TWI Block Diagram

29.3 Function Description

29.3.1 Clock

TWI module clock originates from Ethernet_PLL, fixed at 100MHz, detailed see Chapter CMU.

29.3.2 Timing Parameter

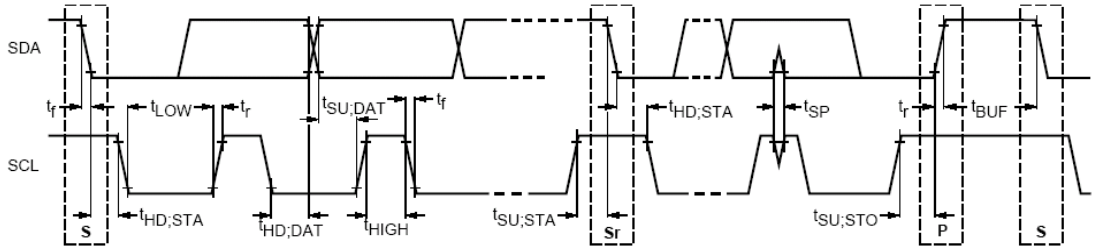


Figure 29-2 TWI Standard/Fast Mode Timing Sequence

Table 29-1 TWI Standard/Fast Mode Timing Parameter

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	4.0	–	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	–	1.3	–	us
HIGH period of the SCL clock	tHIGH	4.0	–	0.6	–	us
Set-up time for a repeated START condition	tSU;STA	4.7	–	0.6	–	us
Data set-up time	tSU;DAT	250	-	100	–	ns
Data Hold time	tHD	300	–	300	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20	300	ns
Set-up time for STOP condition	tSU;STO	4.0	–	0.6	–	us
Bus free time between a STOP and START condition	tBUF	4.7	–	1.3	–	us
Capacitive load for each bus line	Cb	–	400	–	400	pF

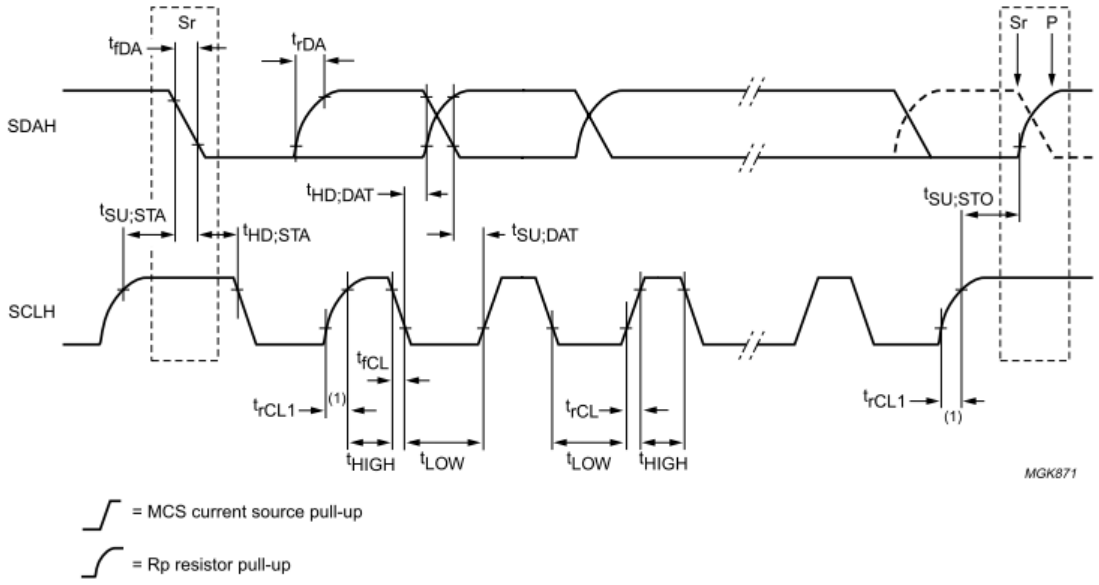


Figure 29-3 TWI High Speed Mode Timing Sequence

Table 29-2 TWI High Speed Mode Timing

PARAMETER	SYMBOL	C_b = 100 pF MAX.		C_b = 400 pF(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCLH clock frequency	f_{SCLH}	0	3.4	0	1.7	MHz
Set-up time (repeated) START condition	$t_{SU;STA}$	160	–	160	–	ns
Hold time (repeated) START condition	$t_{HD;STA}$	160	–	160	–	ns
LOW period of the SCLH clock	t_{LOW}	160	–	320	–	ns
HIGH period of the SCLH clock	t_{HIGH}	60	–	120	–	ns
Data set-up time	$t_{SU;DAT}$	10	–	10	–	ns
Data hold time	$t_{HD;DAT}$	0(3)	70	0(3)	150	ns
Rise time of SCLH signal	t_{rCL}	10	40	20	80	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	t_{rCL1}	10	80	20	160	ns
Fall time of SCLH signal	t_{fCL}	10	40	20	80	ns
Rise time of SDAH signal	t_{rDA}	10	80	20	160	ns
Fall time of SDAH signal	t_{fDA}	10	80	20	160	ns
Set-up time for STOP condition	$t_{SU;STO}$	160	–	160	–	ns
Capacitive load for SDAH and SCLH lines	C_b(2)	–	100	–	400	pF
Capacitive load for SDAH + SDA line and SCLH + SCL line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

29.4 Register List

Table 29-3 TWI Block Base Address

Name	Physical Base Address
TWI0	0xB0170000
TWI1	0xB0174000

TWI2	0xB0178000
TWI3	0xB017C000

Table 29-4 TWI Block Configuration Registers List

Offset	Register Name	Description
0x0000	TWIx_CTL	TWI Control Register
0x0004	TWIx_CLKDIV	TWI Clock Divide Register
0x0008	TWIx_STAT	TWI Status Register
0x000C	TWIx_ADDR	TWI Address Register
0x0010	TWIx_TXDAT	TWI TX Data Register
0x0014	TWIx_RXDAT	TWI RX Data Register
0x0018	TWIx_CMD	TWI Command Register
0x001C	TWIx_FIFOCTL	TWI FIFO control Register
0x0020	TWIx_FIFOSTAT	TWI FIFO status Register
0x0024	TWIx_DATCNT	TWI Data transmit counter
0x0028	TWIx_RCNT	TWI Data transmit remain counter

29.5 Register Description

29.5.1 TWIx_CTL

TWI Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	SHSM	Standard high speed mode 0:disable standard high speed mode 1:enable standard high speed mode	RW	0
9	FHSM	Force in High speed mode 0:not in High speed mode 1:Force to High speed mode (3.4M)	RW	0
8	AE	Arbitrate enable 0:disable 1:enable	RW	0
7	EN	Enable. When enable, reset the status machine to IDLE 0:Disable 1:Enable	RW	0
6	-	Reserved	-	-
5	IRQE	IRQ Enable. 0:Disable 1:Enable FIFO mode added: When the following conditions is satisfied, IRQ will generate: 1. when writing TX FIFO empty, counter doesn't count to 0, then IRQ generates; if the counter counts to 0, then IRQ generates after it is stopped. 2. when reading RX FIFO full. 3. stop signal is generated or received	RW	0

		4. received local slave address as slave device 6. received NACK(not neglected NACK)		
4	-	Reserved	R	0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00:No effect 01:Generating START condition 10:Generating STOP condition 11:Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus.	RW	0
1	RB	Release Bus. Write 1 to this bit will release the bus.	RW	0
0	GRAS	Generate ACK or NACK Signal. When receive data 0:generate the ACK signal at 9th clock of SCL 1:generate the NACK signal at 9th clock of SCL	RW	0

29.5.2 TWIx_CLKDIV

TWI Clock Divide Control Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0
17:16	CLKCOMP	Clk counter compensation 00:no compensation 01:10ns 10:20ns 11:30ns *Note:if the clock rising time too slow results in that the pin speed becomes slower than configuration, this bit can be used to compensate.*	RW	0
15:8	HDIV	High speed mode Clock Divider Factor (only for the master mode). Calculating SCL is as following: SCL=100M/(CLKDIV*6)	RW	0
7:0	CLKDIV	Clock Divider Factor (only for master mode). TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=100M/(CLKDIV*16)	RW	0

29.5.3 TWIx_STAT

TWI Status Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0
10	SRGC	Slave receive general call	R	0

		0:not receive a general call 1:receive a general call		
9	SAMB	Slave address match bit 0:slave address not match 1:slave address match	R	0
8	LBST	Last Byte Status Bit. 0:Indicate the last byte received or transmitted is address 1:Indicate the last byte received or transmitted is data	R	0
7	TCB	Transfer complete bit 0:not finish transfer 1:In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing 1 to this bit will clear it.	RW	0
6	BBB	Bus busy bit 0:Not busy 1:Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0
5	STAD	Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0:Start bit is not detected 1:Start bit is detected	RW	0
4	STPD	Stop detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0:Stop bit is not detected 1:Stop bit is detected	RW	0
3	LAB	Lose arbitration bit 0:not lose 1:lose arbitration Write 1 clear it The bit is clear when the TWI module is disable will clear it.	RW	0
2	IRQP	IRQ Pending Bit. 1:IRQ 0:No IRQ Set condition: 1. transfer complete 2. detect normal stop bit (no bus error) 3. arbit fail Clear condition: Writing 1 to this bit will clear it.	RW	0
1	BEB	Bus error bit 0:No error occur 1:Bus error occur Write “1” to clear this bit The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit.	RW	0

		Detect stop, start bit when sending or receiving data.		
0	RACK	Receive ACK or NACK when transmit data or address 0:NACK 1:ACK The bit will be updated when the 9th of next byte clock arrived	R	0

29.5.4 TWIx_ADDR

TWI Address Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. TWI_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master.	RW	0
0	-	Reserved.	R	0

29.5.5 TWIx_TXDAT

TWI Data Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:0	DA	The register of Data or address to be transfer, or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave TWI device address while the LSB is the Read/Write bit. 128 FIFO, 8*128	RW	0

29.5.6 TWIx_RXDAT

TWI Data Register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:0	DA	The Receive data Register 128 layer FIFO, 8*128	RW	0

29.5.7 TWIx_CMD

TWI Data Register

Offset=0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15	SECL	Start to execute the command list 0:not execute 1:execute command If this bit is not enabled, then FIFO cannot be used, but the original non-FIFO in TWI module can be used.	RW	0
14:13	-	Reserved	R	0
12	WRS	Write or Read select 0:write 1:read This bit only used in Slave mode. When used as master device, write or read flag can be identified by the bit[0] following the start bit.	RW	0
11	MSS	Master or slave mode select 0:slave mode 1:Master mode	RW	0
10	SE	Stop enable 0:disable 1:enable	RW	0
9	NS	NACK select 0:not select 1:select generate the NACK signal at 9th clock of SCL of the last byte when read data	RW	0
8	DE	Data enable 0:disable 1:enable The counts of data transmitted depend on the TWIx_CNT register.	RW	0
7:5	SAS	Second address select 000:no address 001:1 byte address 010:2 byte address 011:3 byte address 100:4 byte address 101:5 byte address 110:6 byte address 111:7 byte address The address domain following the Restart command.	RW	0
4	RBE	Restart bit enable 0:not send restart bit 1:send restart bit	RW	0
3:1	AS	Address select 000:no address 001:1 byte address 010:2 byte address 011:3 byte address 100:4 byte address 101:5 byte address 110:6 byte address 111:7 byte address	RW	0

		The address include slave address and slave internal memory address. The address domain following the Start command.		
0	SBE	Start bit enable 0:not send start bit 1:send start bit	RW	0

29.5.8 TWIx_FIFOCTL

TWI Counter Register
Offset=0x001C

Bits	Name	Description	Access	Reset
31:3	-	Reserved	R	0
2	TFR	TX FIFO reset bit Write 1 to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	RW	0
1	RFR	RX FIFO reset bit Write 1 to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	RW	0
0	NIB	NACK Ignore Bit 0:not ignore, when receive NACK when write, generate Error, do not continue the command list execute, generate IRQ 1:ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	RW	0

Note:the threshold of Tx FIFO and Rx FIFO generating IRQ is all-empty or all-full.

29.5.9 TWIx_FIFOSTAT

TWI Counter Register
Offset=0x0020

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0
23:16	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0
15:8	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0
7	-	Reserved	R	0
6	WRS	Write or read status bit when acts as slave, used only in FIFO mode 0:master write to slave 1:master read from slave	R	0
5	TFF	TX FIFO full bit 0:not full 1:full	R	0
4	TFE	TX FIFO empty bit 0:empty 1:not empty	R	0
3	RFF	RX FIFO full bit 0:not full 1:full	R	0

2	RFE	RX FIFO empty bit 0:empty 1:not empty	R	0
1	RNB	Receive NACK Error bit 0:not receive NACK 1:receive NACK when write data Write 1 to clear this bit When writing data outside, if besides the last byte, other byte receives NACK in the transmission, and if FIFOCTL[0] is 0, then this bit should write 1, stop executing CMD and generate interrupt; If FIFOCTL[0] is 1, then this bit should not be set, and continue executing CMD.	RW	0
0	CECB	Command Execute Complete bit 0:not complete 1:complete Writing this bit to 1 meaning that all the instruction and data has been written or read.	R	1

29.5.10 TWIx_DATCNT

TWI Counter Register
Offset=0x0024

Bits	Name	Description	Access	Reset
31:10	-	Reserved	R	0
9:0	TC	Data Transmit counter, is related to CMD register bit[8], if TWI_CMD[8] is not enabled, then this counter is invalid.	RW	0

29.5.11 TWIx_RCNT

TWI remain Counter Register
Offset=0x0028

Bits	Name	Description	Access	Reset
31:10	-	Reserved	R	0
9:0	TC	Remain counter Displaying the number of data that has not been transmitted.	R	0

29.6 Application Note

29.6.1 Standard/Fast Mode Control Flow

Write 8 byte data into EEPROM:

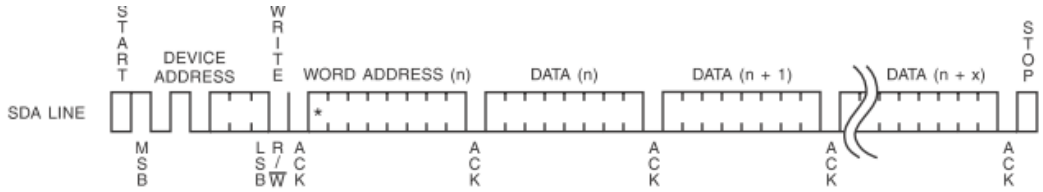


Figure 29-4 Write 8 Bytes Data Format

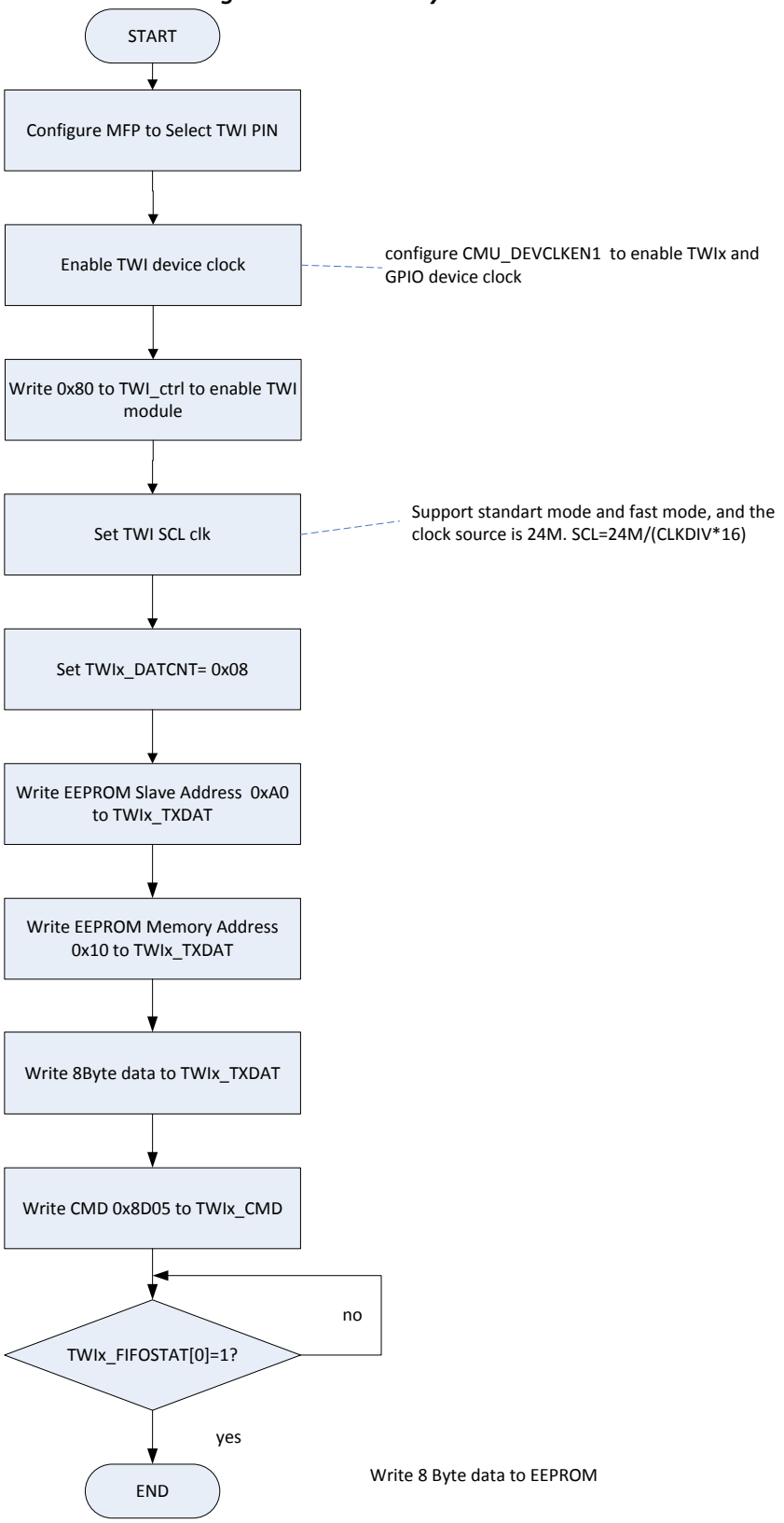


Figure 29-5 TWI Standard/Fast Mode Write 8 Byte data into EEPROM

Read 8 byte data from EEPROM:

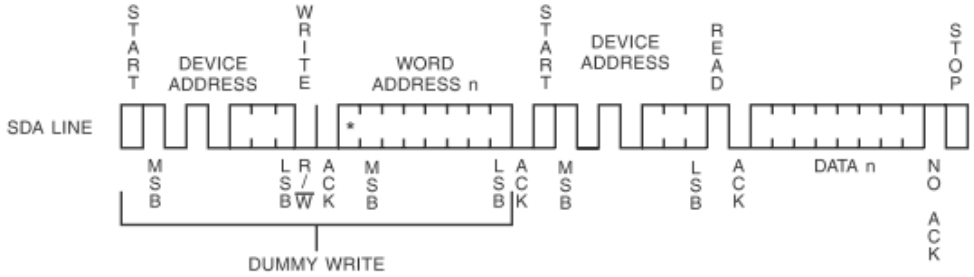


Figure 29-6 Read from EEPROM 8 byte data format

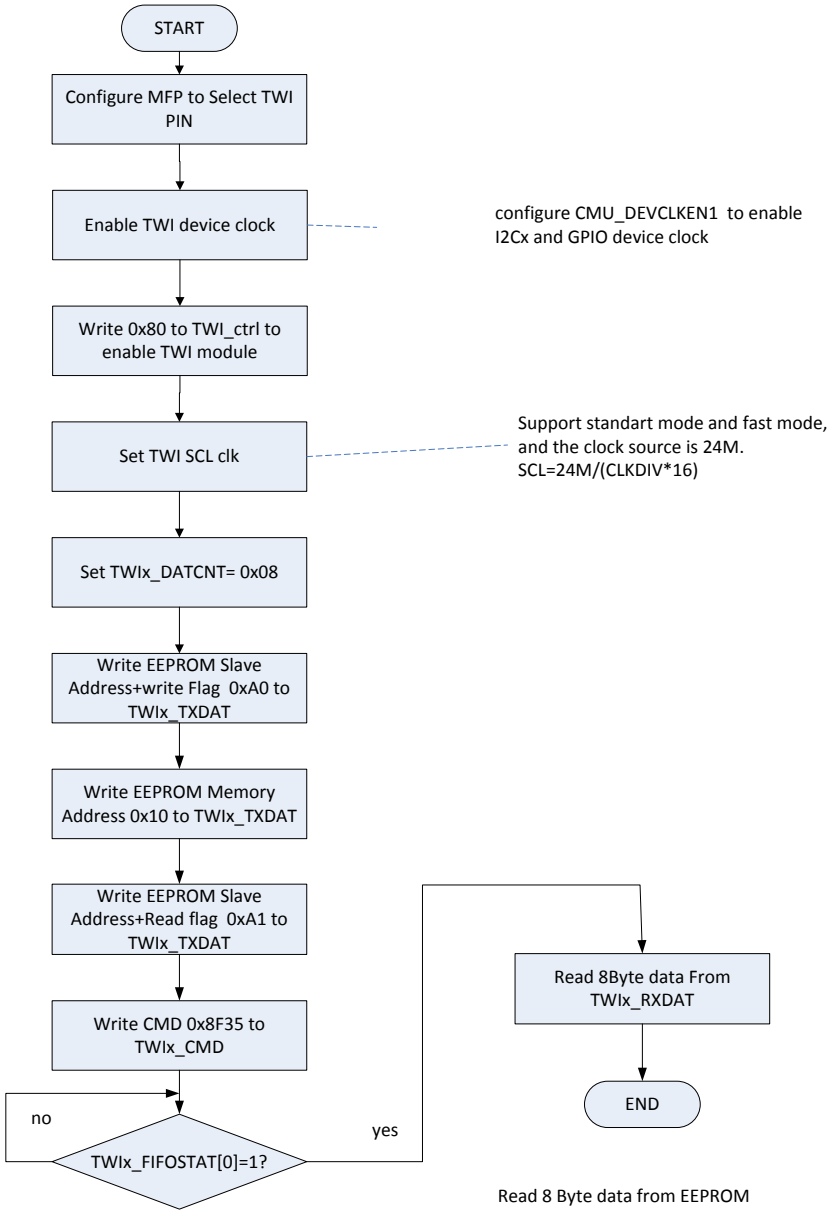


Figure 29-7 Flow of reading 8 byte data from EEPROM

29.6.2 High-Speed Mode Control Flow

High-Speed Mode (HS Mode)
To start HS Mode should send Master Code under FS Mode:

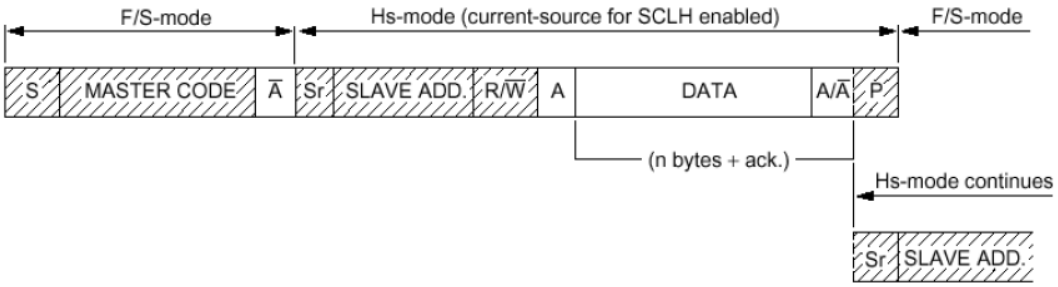


Figure 29-8 High Spead Data format

Detail information and operation flow, please refer to <*The TWI-Bus Specification*>

30 GPIO and PWM

30.1 Overview

This chapter will describe the multiplexing of the whole system and the GPIO/PWM function. There are 106 bits General purpose I/O port and 6 PWM (Pulse Width Modulation) output ports in S500 to bring more flexible application possibilities. The multiplexing is software controlled and can be configured for different applications. Some special pads with Built-in pull up or pull down resistors are described here in this module also. Features of GPIO and PWM module are listed below:

- Built-in pull-up or pull-down resistance in some functional pads

GPIO

- 106 GPIOs with independent output and input function
- Several different driving capacity of 106 GPIOs
- Software control for Multiplexing

PWM

- independent PWM signal from Hz to MHz
- PWM with 1024-level duty adjustment
- PWM with high level or low level active

30.2 Block Diagram

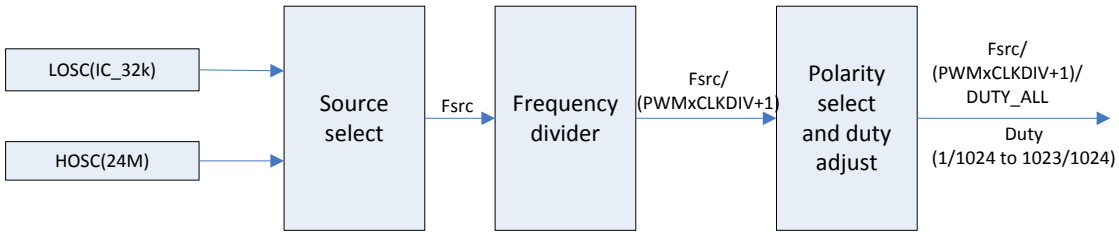


Figure 30-1 PWM Block Diagram

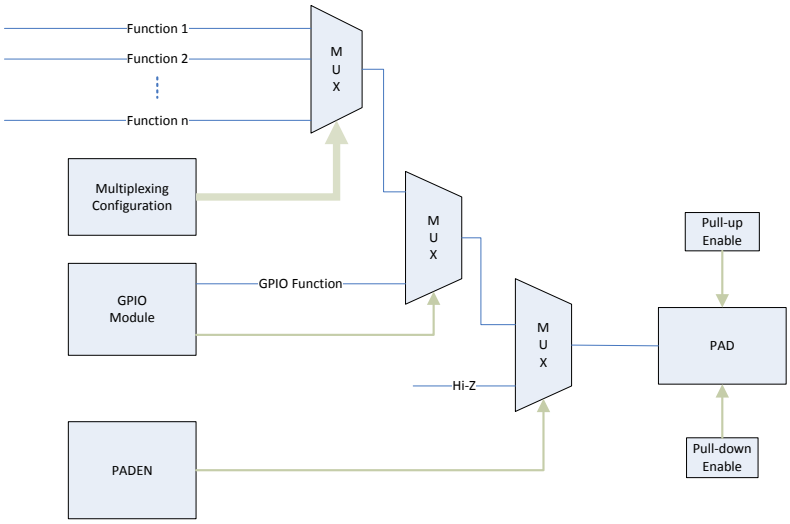


Figure 30-2 Multiplexing Top View Diagram

30.3 Function Description

30.3.1 GPIO

In S500, several different kinds of function signals share the common IO pads. The multiplexing is used to alternate the function of the IO pads which are driven by different module.
IO pads are alternated to corresponding module functions only when setting the MFP_CTLx registers to the relative value.
The GPIOs have higher priority than other module functions no matter when they are configured as input or output, which brings more flexibility in application. When using other module function signal, the OUTEN and INEN of the corresponding GPIOs should be Disable. Otherwise, the module function will be disable.PAD MUX have higher priority than GPIOs.
The GPIOs can output high voltage level or low voltage level when OUTEN is enable. When INEN is enabled, GPIOs can be used as input for detecting the voltage level through watching the GPIO DAT registers. The GPIOs are assorted to several driving capacity. Select the proper driving current before using it.
Note: GPIOs have higher priority than other module functions shared with them no matter when they are used as output or input. if PAD_CTL.PAD_EN is disabled, GPIO cannot work even if the corresponding GPIO register has been set.

30.3.2 PWM

PWM output module is embedded in S500, in the purpose of controlling the external backlight IC, micro-step motor or the buzzer conveniently. It supplies widely variable output frequency from Hz to MHz and 1024-level duty occupancy for precise adjustment.

30.3.3 Source Select

The clock sent to Frequency Divider is called Fsrc. To set Fsrc, refer to bit12 of the register CMU_PWMxCLK. Fsrc can be get from two clocks sources, One is LOSC(32k), which is applied to PWM frequency below 500Hz.The other is HOSC(24M),which is applied to PWM frequency between 500Hz and 375KHz.

30.3.4 Frequency Divide

Divide the frequency according to the setting of PWMxCLKDIV in register CMU_PWMxCLK[9:0]. After the dividing, frequency becomes Fsrc/(PWMxCLKDIV+1). To set the frequency divider, refer to the register CMU_PWMxCLK[9:0].

30.3.5 Polarity Select And Duty Adjust

The PWM can be high voltage or low voltage active. The polarity select bit is for setting if the active duty is high voltage or low. To set the polarity select, please refer to the register PWMx_CTL[20].

About the duty cycle adjustment, please refer to the register PWMx_CTL[19:0], When POL_SEL=0， duty cycle= 1- DUTY_ACTIVE / DUTY_ALL; When POL_SEL=1, duty cycle= DUTY_ACTIVE / DUTY_ALL.

30.3.6 Multiplexing

In S500, several different kinds of function signals share the common IO pads. The multiplexing is used to alternate the function of the IO pads which are driven by different module.
IO pads are alternated to corresponding module functions only when setting the MFP_CTLx registers to the correct value.

The GPIOs have higher priority than other module functions no matter when they are configured as input or output, which brings more flexibility in application. When using other module function signal, the OUTEN and INEN of the corresponding GPIOs should be Disable. Otherwise, the module function will be disable.PAD MUX have higher priority than GPIOs.

30.3.7 Configuration

It needs to set the proper configuration of MFP_CTLx before using any module function. One pad can only be one function at a time. To know more about configuration of pad function, refer to the register description.

30.4 Register List

Table 30-1 GPIO/MFP/PWM Base Address

Name	Physical Base Address
GPIO_MFP_PWM	0xB01B0000

Table 30-2 GPIO/MFP/PWM Register List

Offset	Register Name	Description
0x0000	GPIO_AOUTEN	GPIOA Output Enable Register
0x0004	GPIO_AINEN	GPIOA Input Enable Register
0x0008	GPIO_ADAT	GPIOA Data Register
0x000C	GPIO_BOUTEN	GPIOB Output Enable Register
0x0010	GPIO_BINEN	GPIOB Input Enable Register
0x0014	GPIO_BDAT	GPIOB Data Register
0x0018	GPIO_COUTEN	GPIOC Output Enable Register
0x001C	GPIO_CINEN	GPIOC Input Enable Register
0x0020	GPIO_CDAT	GPIOC Data Register
0x0024	GPIO_DOUTEN	GPIOD Output Enable Register
0x0028	GPIO_DINEN	GPIOD Input Enable Register
0x002C	GPIO_DDAT	GPIOD Data Register
0x0030	GPIO_EOUTEN	GPIOE Output Enable Register
0x0034	GPIO_EINEN	GPIOE Input Enable Register
0x0038	GPIO_EDAT	GPIOE Data Register
0x0040	MFP_CTL0	Multiplexing Control 0 Register
0x0044	MFP_CTL1	Multiplexing Control 1 Register
0x0048	MFP_CTL2	Multiplexing Control 2 Register
0x004C	MFP_CTL3	Multiplexing Control 3 Register
0x0050~0x005C	PWM_CTL0~3	PWM0~3 Output Control Register
0x0060	PAD_PULLCTL0	PAD Pull Control Register 0
0x0064	PAD_PULLCTL1	PAD Pull Control Register 1
0x0068	PAD_PULLCTL2	PAD Pull Control Register 2
0x006C	PAD_ST0	PAD Schmitt Trigger enable Register0
0x0070	PAD_ST1	PAD Schmitt Trigger enable Register1
0x0074	PAD_CTL	PAD Control Register
0x0078	PWM_CTL4	PWM4 Output Control Register
0x007C	PWM_CTL5	PWM5 Output Control Register
0x0080	PAD_DRV0	PAD Drive Capacity0 Select Register
0x0084	PAD_DRV1	PAD Drive Capacity1 Select Register
0x0088	PAD_DRV2	PAD Drive Capacity2 Select Register

0x0200	INTC_EXTCTL	Interrupt control and status register
0x0204	INTC_GPIOCTL	GPIO Interrupt Type control register
0x0208	INTC_GPIOA_PD	GPIOA Interrupt Pending Register
0x020C	INTC_GPIOA_MSK	GPIOA Interrupt Mask Register
0x0210	INTC_GPIOB_PD	GPIOB Interrupt Pending Register
0x0214	INTC_GPIOB_MSK	GPIOB Interrupt Mask Register
0x0218	INTC_GPIOC_PD	GPIOC Interrupt Pending Register
0x021C	INTC_GPIOC_MSK	GPIOC Interrupt Mask Register
0x0220	INTC_GPIOD_PD	GPIOD Interrupt Pending Register
0x0224	INTC_GPIOD_MSK	GPIOD Interrupt Mask Register
0x0228	INTC_GPIOE_PD	GPIOE Interrupt Pending Register
0x022C	INTC_GPIOE_MSK	GPIOE Interrupt Mask Register
0x0230	INTC_GPIOA_TYPE0	GPIOA Interrupt TYPE0 Register
0x0234	INTC_GPIOA_TYPE1	GPIOA Interrupt TYPE1 Register
0x0238	INTC_GPIOB_TYPE0	GPIOB Interrupt TYPE0 Register
0x023C	INTC_GPIOB_TYPE1	GPIOB Interrupt TYPE1 Register
0x0240	INTC_GPIOC_TYPE0	GPIOC Interrupt TYPE0 Register
0x0244	INTC_GPIOC_TYPE1	GPIOC Interrupt TYPE1 Register
0x0248	INTC_GPIOD_TYPE0	GPIOD Interrupt TYPE0 Register
0x024C	INTC_GPIOD_TYPE1	GPIOD Interrupt TYPE1 Register
0x0250	INTC_GPIOE_TYPE	GPIOE Interrupt TYPE Register

30.5 Register Description

30.5.1 GPIO_AOUTEN

GPIOA Output Enable Register
Offset = 0x0000

Bits	Name	Description	Access	Reset
31:0	GPIOA_OUTEN	GPIOA[31:0] Output Enable. 0:Disable 1:Enable	RW	0

30.5.2 GPIO_AINEN

GPIOA Input Enable Register
Offset = 0x0004

Bits	Name	Description	Access	Reset
31:0	GPIOA_INEN	GPIOA[31:0] Input Enable. 0:Disable 1:Enable	RW	0

30.5.3 GPIO_ADAT

GPIOA Data Register
Offset = 0x0008

Bits	Name	Description	Access	Reset
31:0	GPIOA_DAT	GPIOA[31:0] Input/Output Data.	RW	0

30.5.4 GPIO_BOUTEN

GPIOB Output Enable Register
Offset = 0x000C

Bits	Name	Description	Access	Reset
31:0	GPIOB_OUTEN	GPIOB[31:0] Output Enable. 0:Disable 1:Enable	RW	0

30.5.5 GPIO_BINEN

GPIOB Input Enable Register
Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	GPIOB_INEN	GPIOB[31:0] Input Enable. 0:Disable 1:Enable	RW	0

30.5.6 GPIO_BDAT

GPIOB Data Register
Offset = 0x0014

Bits	Name	Description	Access	Reset
31:0	GPIOB_DAT	GPIOB[31:0] Input/Output Data.	RW	0

30.5.7 GPIO_COUTEN

GPIOC Output Enable Register
Offset = 0x0018

Bits	Name	Description	Access	Reset
31:0	GPIOC_OUTEN	GPIOC[31:0] Output Enable. 0:Disable 1:Enable	RW	0

30.5.8 GPIO_CINEN

GPIOC Input Enable Register
Offset = 0x001C

Bits	Name	Description	Access	Reset
31:0	GPIOC_INEN	GPIOC[31:0] Input Enable. 0:Disable 1:Enable	RW	0

30.5.9 GPIO_CDAT

GPIOC Data Register
Offset = 0x0020

Bits	Name	Description	Access	Reset
31:0	GPIOC_DAT	GPIOC[31:0] Input/Output Data.	RW	0

30.5.10 GPIO_DOUTEN

GPIOD Output Enable Register
Offset = 0x0024

Bits	Name	Description	Access	Reset
31:0	GPIOD_OUTEN	GPIOD[31:0] Output Enable. 0:Disable 1:Enable	RW	0

30.5.11 GPIO_DINEN

GPIOD Input Enable Register
Offset = 0x0028

Bits	Name	Description	Access	Reset
31:0	GPIOD_INEN	GPIOD[31:0] Input Enable. 0:Disable 1:Enable	RW	0

30.5.12 GPIO_DDAT

GPIOD Data Register
Offset = 0x002C

Bits	Name	Description	Access	Reset
31:0	GPIOD_DAT	GPIOD[31:0] Input/Output Data.	RW	0

30.5.13 GPIO_EOUTEN

GPIOE Output Enable Register
Offset = 0x0030

Bits	Name	Description	Access	Reset
31:4	-	Reserved	R	0
3:0	GPIOE_OUTEN	GPIOE[3:0] Output Enable. 0:Disable 1:Enable	RW	0

30.5.14 GPIO_EINEN

GPIOE Input Enable Register
Offset = 0x0034

Bits	Name	Description	Access	Reset
31:4	-	Reserved	R	0
3:0	GPIOE_INEN	GPIOE[3:0] Input Enable. 0:Disable 1:Enable	RW	0

30.5.15 GPIO_EDAT

GPIOE Data Register
Offset = 0x0038

Bits	Name	Description	Access	Reset
31:4	-	Reserved	R	0
3:0	GPIOE_DAT	GPIOE[3:0] Input/Output Data.	RW	0

30.5.16 MFP_CTL0

Multiplexing Control 0 Register
Offset = 0x0040

Bits	Name	Description	Access	Reset
31:26	-	Reserved	R	0
25:23	LCD0_D18	P_LCD0_D18 PAD multiplex select. 000:NOR_A2 001:SENS1_CLKOUT 010:PWM2 011:PWM4 100:LCD0_D18 Other Reserved	RW	0
22:20	RMII_CRS_DV	P_ETH_CRS_DV PAD multiplex select. 000:RMII_CRS_DV 001:SMII_RX 010:SPI2_MISO 011:UART4_RX 100:PWM4 Other Reserved	RW	0
19	-	Reserved	R	0
18:16	RMII_TXD01	P_ETH_TXD0, P_ETH_TXD1 PAD multiplex select. 000:RMII_TXD0, RMII_TXD1 001:SMII_TX, SMII_SYNC 010:SPI2_SCLK, SPI2_SS 011:UART6_RX, UART6_TX 100:PWM4,PWM5 others:Reserved	RW	0
15:13	RMII_TXEN_RXER	P_ETH_TX_EN, P_ETH_RX_ER PAD multiplex select. 000:RMII_TX_EN, RMII_RX_ER 001:UART2_RX, UART2_TX 010:SPI3_SCLK, SPI3_MOSI 011:PWM0, PWM1 Other Reserved	RW	0
12:11	-	Reserved	R	0
10:8	RMII_RXD10	P_ETH_RXD1, P_ETH_RXD0 PAD multiplex select. 000:RMII_RXD[1:0] 001:UART2_RTSB, UART2_CTSB 010:SPI3_SS, SPI3_MISO 011:PWM2, PWM3 100:UART5_TX, UART5_RX others:Reserved	RW	0
7:6	RMII_REF_CLK	P_ETH_REF_CLK PAD multiplex select. 00:RMII_REF_CLK/SMII_CLK 01:UART4_TX	RW	0

		10:SPI2_MOSI 11:Reserved *Note:the IE/OE of this PAD is effected by MAC_CTL[8]:if it is 0, then the reference clock output from CMU and will be sent to PHY outside, so this PAD is output; If it is 1, then external reference clock is used, and this PAD is input.*		
5	I2S_D0	P_I2S_D0 PAD multiplex select. 0:I2S_D0 1:NOR_A16	RW	0
4:3	I2S_PCM1	P_I2S_LRCLK0, P_I2S_MCLK0 PAD multiplex select. 00:I2S_LRCLK0, I2S_MCLK0 01:NOR_A18, NOR_A19 10:PCM1_SYNC, PCM1_CLK 11:Reserved	RW	0
2:1	I2S_PCM0	P_I2S_BCLK0,P_I2S_BCLK1, P_I2S_LRCLK1, P_I2S_MCLK1 PAD multiplex select. 00:I2S_BCLK0, I2S_BCLK1, I2S_LRCLK1, P_I2S_MCLK1 01:NOR_A17, NOR_A21, NOR_A22, NOR_A23 10:PCM0_IN,PCM0_OUT,PCM0_CLK, PCM0_SYNC Other:Reserved	RW	0
0	I2S_D1	P_I2S_D1 PAD multiplex select. 0:I2S_D1 1:NOR_A20	RW	0

30.5.17 MFP_CTL1

Multiplexing Control 1 Register
Offset = 0x0044

Bits	Name	Description	Access	Reset
31:29	KS_IN[0:2]	P_KS_IN[0:2] PAD multiplex select. 000:KS_IN[0:2] 001:TCK, TMS, TDI 010:NOR_A[5:7] 011:PWM0, PWM1, PWM0 100:PWM4, PWM5, PWM0 101:SENS1_D4, SENS1_D5, SENS1_D6 110:PWM4, PWM1, PWM0 111:DRV_VBUS0	RW	1
28:26	KS_IN3_OUT[0:1]	P_KS_IN3, P_KS_OUT[0:1] PAD multiplex select. 000:KS_IN3, KS_OUT[0:1] 001:TDO, UART5_RX, TRST 010:NOR_A[8:10] 011:PWM1, PWM2, PWM3 100:Reserved 101:SENS1_D7, SENS1_PCLK, SENS1_VSYNC 110:-, SD0_CMD, SD0_CLK 111:Reserved	RW	1

<table>
<tr><td>25:23</td><td>KS_OUT2</td><td>P_KS_OUT2 PAD multiplex select.
000:SD0_D1B
001:KS_OUT2
010:NOR_A11
011:PWM2
100:UART5_TX
101 :SENS1_HSYNC
others:Reserved</td><td>RW</td><td>0x4</td></tr>
<tr><td>22:21</td><td>LVDS_O_PN</td><td>LVDS ODD PAD multiplex select.
(Note:switch to digital function before using GPIO)
<table>
<tr><th>PAD</th><th>00:</th><th>10:</th><th>01,11:</th></tr>
<tr><td>OEP</td><td>OEP</td><td>LCD0_DCLK0</td><td rowspan="10">Reserved</td></tr>
<tr><td>OEN</td><td>OEN</td><td>LCD0_HSYNC0</td></tr>
<tr><td>ODP</td><td>ODP</td><td>LCD0_VSYNC0</td></tr>
<tr><td>ODN</td><td>ODN</td><td>LCD0_LDE0</td></tr>
<tr><td>OCP</td><td>OCP</td><td>LCD0_D23</td></tr>
<tr><td>OCN</td><td>OCN</td><td>LCD0_D22</td></tr>
<tr><td>OBP</td><td>OBP</td><td>LCD0_D21</td></tr>
<tr><td>OBN</td><td>OBN</td><td>LCD0_D20</td></tr>
<tr><td>OAP</td><td>OAP</td><td>LCD0_D19</td></tr>
<tr><td>OAN</td><td>OAN</td><td>LCD0_D15</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>20:19</td><td>DSI_DN0</td><td>DSI_DN0 PAD multiplex select.
00:DSI_DN0
01:UART2_TX
10:SPI0_MOSI
11:Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>18:17</td><td>DSI_DP2</td><td>DSI_DP2 PAD multiplex select.
00:DSI_DP2
01:UART2_RTSB
10:SPI0_SCLK
11:SD1_CLKB</td><td>RW</td><td>0</td></tr>
<tr><td>16:14</td><td>LCD0_D17</td><td>P_LCD0_D17 PAD multiplex select.
000:NOR_A0
001:SD0_CLKB
010:SD1_CMD
011:PWM3
100:LCD0_D17
Other Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>13:12</td><td>DSI_DP3</td><td>DSI_DP3 PAD multiplex select.
00:DSI_DP3
01:SD1_CLKB
10:SD1_CLK
11:LCD0_D16</td><td>RW</td><td>0</td></tr>
<tr><td>11:10</td><td>DSI_DN3</td><td>DSI_DN3 PAD multiplex select.
00:DSI_DN3
01:Reserved
10:SD1_D3
11:LCD0_D9</td><td>RW</td><td>0</td></tr>
<tr><td>9:7</td><td>DSI_DP0</td><td>DSI_DP0 PAD multiplex select.
000:DSI_DP0
001:Reserved</td><td>RW</td><td>0</td></tr>
</table>

		010:SD0_CLKB 011:UART2_RX 100:SPI0_MISO 1xx:Reserved		
6:5	LVDS_EE_PN1	LVDS EE PN PAD multiplex select. *Note:GPIO should set to non-zero value* 00:EEP, EEN 01:NOR_RD, NOR_WR 10:Reserved 11:LCD0_D14, LCD0_D13	RW	0
4:3	SPI0_TWI_PCM	P_SPI0_SCLK, P_SPI0_MOSI PAD multiplex select. 00:SPI0_SCLK, SPI0_MOSI 01:NOR_A12, NOR_A15 10:TWI3_SCLK, TWI3_SDATA 11:PCM0_CLK, PCM0_SYNC	RW	0
2:0	SPI0_I2S_PCM	P_SPI0_SS, P_SPI0_MISO PAD multiplex select. 000:SPI0_SS, SPI0_MISO 001:NOR_A[13:14] 010:I2S_LRCLK1, I2S_MCLK1 011:PCM1_OUT, PCM1_IN/ 100:PCM0_OUT, PCM0_IN 1xx:Reserved	RW	0

30.5.18 MFP_CTL2

Multiplexing Control 2 Register
Offset = 0x0048

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>31</td><td>-</td><td>Reserved</td><td>R</td><td>0</td></tr>
<tr><td>30:29</td><td>DSI_DNP1_CP</td><td>DSI_DP1, DSI_CP, DSI_CN PAD multiplex select.
00:DSI_DP1, DSI_DN1, DSI_CP, DSI_CN
01:SD1_D2, -, SD1_D1, SD1_D0
10:LCD0_D8, LCD0_D2, LCD0_D1, LCD0_D0
11:Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>28:27</td><td>LVDS_E_PN</td><td>LVDS EA~ED PAD multiplex select.
(Note:switch to digital function before using GPIO)
<table>
<tr><th>PAD</th><th>00:</th><th>01:</th><th>10:</th><th>11:</th></tr>
<tr><td>EDP</td><td>EDP</td><td>NOR_D13</td><td>LCD0_D12</td><td rowspan="8">Reserved</td></tr>
<tr><td>EDN</td><td>EDN</td><td>NOR_D12</td><td>LCD0_D11</td></tr>
<tr><td>ECP</td><td>ECP</td><td>NOR_D11</td><td>LCD0_D10</td></tr>
<tr><td>ECN</td><td>ECN</td><td>NOR_A4</td><td>LCD0_D7</td></tr>
<tr><td>EBP</td><td>EBP</td><td>NOR_D15</td><td>LCD0_D6</td></tr>
<tr><td>EBN</td><td>EBN</td><td>NOR_D14</td><td>LCD0_D5</td></tr>
<tr><td>EAP</td><td>EAP</td><td>NOR_D9</td><td>LCD0_D4</td></tr>
<tr><td>EAN</td><td>EAN</td><td>NOR_D8</td><td>LCD0_D3</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>26:24</td><td>DSI_DN2</td><td>DSI_DN2 PAD multiplex select.
000:DSI_DN2
001:Reserved
010:SD1_D1B
011:UART2_CTSB
100:SPI0_SS
1xx:Reserved</td><td>RW</td><td>0</td></tr>
</table>

23	UART2_RTSB	P_UART2_RTSB PAD multiplex select. 0:UART2_RTSB 1:UART0_RX	RW	0
22	UART2_CTSB	P_UART2_CTSB PAD multiplex select. 0:UART2_CTSB 1:UART0_TX	RW	0
21	UART3_RTSB	P_UART3_RTSB PAD multiplex select. 0:UART3_RTSB 1:UART5_RX	RW	0
20	UART3_CTSB	P_UART3_CTSB PAD multiplex select. 0:UART3_CTSB 1:UART5_TX	RW	0
19:17	SD0_D0	P_SD0_D0 PAD multiplex select. 000:SD0_D0 001:NOR_D0 010:Reserved 011:TRST 100:UART2_RX 101:UART5_RX 11x:Reserved	RW	0
16:14	SD0_D1	P_SD0_D1 PAD multiplex select. 000:SD0_D1 001:NOR_D1 010:Reserved 011:Reserved 100:UART2_TX 101:UART5_TX 11x:Reserved	RW	0
13:11	SD0_D2_D3	P_SD0_D[2:3] PAD multiplex select. 000:SD0_D[2:3] 001:NOR_D[2:3] 010:Reserved 011:TDO, TDI 100:UART2_RTSB, UART2_CTSB 101:UART1_TX, UART1_RX 11x:Reserved	RW	0
10:9	SD1_D0_D3	P_SD1_D[0:3] PAD multiplex select. 00:SD0_D[4:7] 01:NOR_D[4:7] 10:Reserved 11:SD1_D[0:3]	RW	0
8:7	SD0_CMD	P_SD0_CMD PAD multiplex select. 00:SD0_CMD 01:NOR_A1 10:Reserved 11:TMS	RW	0
6:5	SD0_CLK	P_SD0_CLK PAD multiplex select. 00:SD0_CLK 01:Reserved 10:TCK 11:Reserved	RW	0
4:3	SD1_CMD	P_SD1_CMD PAD multiplex select. 00:SD1_CMD	RW	0

		01:NOR_CEB0_7 10:Reserved 11:Reserved		
2:0	UART0_RX	P_UART0_RX PAD multiplex select. 000:UART0_RX 001:UART2_RX 010:SPI1_MISO 011:TWI0_SDATA 100:PCM1_IN 101:I2S_MCLK1 11x:Reserved	RW	0

30.5.19 MFP_CTL3

Multiplexing Control 3 Register
Offset = 0x004C

Bits	Name	Description	Access	Reset
31	-	Reserved	-	-
30	CLKO_25M	P_CLKO_25M PAD multiplex select. 0:Reserved 1:CLKO_25M	RW	0
29:28	CSI_CN_CP	CSI_CN, CSI_CP PAD multiplex select. 00:CSI_CN, CSI_CP 01:SENS0_VSYNC, SENS0_HSYNC others:Reserved	RW	0
27:24	-	Reserved	-	-
23:22	SENS0_CKOUT	P_SENSOR0_CKOUT PAD multiplex select. 00:SENS0_CKOUT 01:NOR_D10 10:SENS1_CKOUT 11:PWM1	RW	0
21:19	UART0_TX	P_UART0_TX PAD multiplex select. 000:UART0_TX 001:UART2_TX 010:SPI1_SS 011:TWI0_SCLK 100:SPDIF 101:PCM1_OUT 110:I2S_LRCLK1 1xx:Reserved	RW	0
18:16	TWI0_MFP	P_TWI0_SCLK, P_TWI0_SDATA PAD multiplex select. 000:TWI0_SCLK, TWI0_SDATA 001:UART2_RTSB, UART2_CTSB 010:TWI1_SCLK, TWI1_SDATA 011:UART1_TX, UART1_RX 100:SPI1_SCLK, SPI1_MOSI others:Reserved	RW	0
15:14	CSI_DN_DP	CSI_DN0123, CSI_DP0123 PAD multiplex select. 00:CSI_DN0, CSI_DP0, CSI_DN1, CSI_DP1, CSI_DN2, CSI_DP2, CSI_DN3, CSI_DP3 01:SENS0_D2, SENS0_D3, SENS0_D6, SENS0_D7, SENS0_D0, SENS0_D1, SENS0_D5, SENS0_D4	RW	0

		others:Reserved		
13:12	SENS0_PCLK	P_SENSOR0_PCLK PAD multiplex select. 00:SENSOR0_PCLK 01:NOR_A3 10:PWM0 11:Reserved	RW	0
11:10	PCM1_IN	P_PCM1_IN PAD multiplex select. 00:PCM1_IN 01:SENS1_D3 10:UART4_RX 11:PWM4	RW	0
9:8	PCM1_CLK	P_PCM1_CLK PAD multiplex select. 00:PCM1_CLK 01:SENS1_D2 10:UART4_TX 11:PWM5	RW	0
7:6	PCM1_SYNC	P_PCM1_SYNC PAD multiplex select. 00:PCM1_SYNC 01:SENS1_D1 10:UART6_RX 11:TWI3_SCLK	RW	0
5:4	PCM1_OUT	P_PCM1_OUT PAD multiplex select. 00:PCM1_OUT 01:SENS1_D0 10:UART6_TX 11:TWI3_SDATA	RW	0
3	DNAND_DATA_WR	P_NAND_D0~7, NAND_RDBN, NAND_RDB PAD multiplex select. 0:NAND_D0~7, NAND_RDBN, NAND_RDB 1:SD2_D0—7, SD2_CMD, SD2_CLK	RW	0
2	DNAND_ACLE_CE0_1	P_NAND_ALE, P_NAND_CLE, P_NAND_CEB0, P_NAND_CEB1 PAD multiplex select. 0:NAND_ALE, NAND_CLE, NAND_CEB0, NAND_CEB1 1:SPI2_MISO, SPI2_MOSI, SPI2_SCLK, SPI2_SS	RW	0
1:0	DNAND_CE2_3	P_NAND_CEB2, P_NAND_CEB3 PAD multiplex select. 00:NAND_CEB2, NAND_CEB3 01:PWM5, PWM4 10:Reserved 11:Reserved	RW	0

30.5.20 PWM_CTL0~3

PWMx Output Control Register (x = 0~3)
Offset = 0x0050 + 4 * x

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0
20	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active	RW	0
19:10	DUTY_ACTIVE	The PWM clk cycle within active period	RW	0
9:0	DUTY_ALL	The PWM clk cycle within a whole PWM period	RW	0

30.5.21 PAD_PULLCTL0

PAD Pull Control Register 0
Offset = 0x0060

Bits	Name	Description	Access	Reset
31	-	Reserved	R	0
30	P_PCM1_SYNC_P	P_PCM1_SYNC PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
29	P_PCM1_OUT_P	P_PCM1_OUT PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
28	P_KS_OUT2_P	P_KS_OUT2 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
27	P_LCD0_D17_P	P_LCD0_D17 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
26	DSI_DN3_P	DSI_DN3 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
25:17	-	Reserved	-	-
16	P_ETH_RX_ER_P	P_ETH_RX_ER PAD pull control. 0:100K pull-down disable 1:100K pull-down enable	RW	0
15:14	P_SIRQ0_P	P_SIRQ0 PAD pull control. 00:100K pull-up disable and 100K pull-down disable 01:100K pull-up enable and 100K pull-down disable 10:100K pull-up disable and 100K pull-down enable 11:Reserved (Hardware forbidden)	RW	0
13:12	P_SIRQ1_P	P_SIRQ1 PAD pull control. 00:100K pull-up disable and 100K pull-down disable 01:100K pull-up enable and 100K pull-down disable 10:100K pull-up disable and 100K pull-down enable 11:Reserved (Hardware forbidden)	RW	0
11:10	P_SIRQ2_P	P_SIRQ2 PAD pull control. 00:100K pull-up disable and 100K pull-down disable 01:100K pull-up enable and 100K pull-down disable 10:100K pull-up disable and 100K pull-down enable 11:Reserved (Hardware forbidden)	RW	0
9	P_TWI0_SDATA_P	P_TWI0_SDATA PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0

8	P_TWI0_SCLK_P	P_TWI0_SCLK PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
7	P_KS_IN0_P	P_KS_IN0 PAD pull control. 0:100K pull-up disable 1:100K pull-up enable	RW	1
6	P_KS_IN1_P	P_KS_IN1 PAD pull control. 0:100K pull-up disable 1:100K pull-up enable	RW	1
5	P_KS_IN2_P	P_KS_IN2 PAD pull control. 0:100K pull-up disable 1:100K pull-up enable	RW	1
4	P_KS_IN3_P	P_KS_IN3 PAD pull control. 0:100K pull-up disable 1:100K pull-up enable	RW	0
3	-	Reserved	-	-
2	P_KS_OUT0_P	P_KS_OUT0 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
1	P_KS_OUT1_P	P_KS_OUT1 PAD pull control. 0:100K pull-up disable 1:100K pull-up enable	RW	1
0	DSI_DP1_P	DSI_DP1 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0

30.5.22 PAD_PULLCTL1

PAD Pull Control Register 1
Offset = 0x0064

Bits	Name	Description	Access	Reset
31	DSI_CP_P	DSI_CP PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
30	DSI_CN_P	DSI_CN PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
29	-	Reserved	R	0
28	DSI_DN2_P	DSI_DN2 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
27:26	-	Reserved	R	0
25	P_DNAND_RDBN_P	P_DNAND_RDBN PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
24:18	-	Reserved	R	0
17	P_SD0_D0_P	P_SD0_D0 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	1
16	P_SD0_D1_P	P_SD0_D1 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0

15	P_SD0_D2_P	P_SD0_D2 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
14	P_SD0_D3_P	P_SD0_D3 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	1
13	P_SD0_CMD_P	P_SD0_CMD PAD pull control. 0:50K pull-up disable 1:50K pull-up enable	RW	1
12	P_SD0_CLK_P	P_SD0_CLK PAD pull control. 0:50K pull-up disable 1:50K pull-up enable	RW	1
11	P_SD1_CMD_P	P_SD1_CMD PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
10:7	-	Reserved	R	0
6	P_SD1_D0_P	P_SD1_D0 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
5	P_SD1_D1_P	P_SD1_D1 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
4	P_SD1_D2_P	P_SD1_D2 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
3	P_SD1_D3_P	P_SD1_D3 PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
2	P_UART0_RX_P	P_UART0_RX PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
1	P_UART0_TX_P	P_UART0_TX PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
0	P_CLKO_25M_P	P_CLKO_25M PAD pull control. 0:100K pull-down disable 1:100K pull-down enable	RW	1

30.5.23 PAD_PULLCTL2

PAD Pull Control Register 2
Offset = 0x0068

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0
12	P_SPI0_SCLK_P	P_SPI0_SCLK PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
11	P_SPI0_MOSI_P	P_SPI0_MOSI PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
10	P_TWI1_SDATA_P	P_TWI1_SDATA PAD pull control. 0:1.5-2.5K pull-up disable	RW	0

		1:1.5-2.5K pull-up enable		
9	P_TWI1_SCLK_P	P_TWI1_SCLK PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
8	P_TWI2_SDATA_P	P_TWI2_SDATA PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
7	P_TWI2_SCLK_P	P_TWI2_SCLK PAD pull control. 0:1.5-2.5K pull-up disable 1:1.5-2.5K pull-up enable	RW	0
6:5	P_DNAND_DQSN_P	P_DNAND_DQSN PAD pull control. 00:30K pull-up disable 01:Reserved 10:30K pull-up enable 11:Reserved	RW	0x2
4:3	P_DNAND_DQS_P	P_DNAND_DQS PAD pull control. 00:10-50K pull-up disable and 30K pull-down disable 01:10-50K pull-up enable and 30K pull-down disable 10:10-50K pull-up disable and 30K pull-down enable 11:Reserved (Hardware forbidden)	RW	0x2
2	P_DNAND_D[0:7]_P	P_DNAND_D[0:7] PAD pull control. 0:10-50K pull-up disable 1:10-50K pull-up enable	RW	0
1:0	-	Reserved	R	0

30.5.24 PAD_ST0

PAD Schmitt Trigger enable Register0
Offset = 0x006C

Bits	Name	Description	Access	Reset
31	-	Reserved	R	0
30	P_TWI0_SDATA_ST	P_TWI0_SDATA pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
29	P_UART0_RX_ST	P_UART0_RX pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
28:24	-	Reserved	R	0
23	P_I2S_MCLK1_ST	P_I2S_MCLK1 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
22	P_ETH_REF_CLK_ST	P_ETH_REF_CLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
21	P_ETH_TX_EN_ST	P_ETH_TX_EN pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0

20	P_ETH_TXD0_ST	P_ETH_TXD0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
19	P_I2S_LRCLK1_ST	P_I2S_LRCLK1 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
18:17	-	Reserved	R	0
16	DSI_DP0_ST	DSI_DP0 PAD Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
15	DSI_DN0_ST	DSI_DN0 PAD Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
14	P_UART0_TX_ST	P_UART0_TX pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
13	P_SPI0_SCLK_ST	P_SPI0_SCLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
12	P_SD0_CLK_ST	P_SD0_CLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
11	P_KS_IN0_ST	P_KS_IN0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
10	-	Reserved	R	0
9	P_SENSOR0_PCLK	P_SENSOR0_PCLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
8	-	Reserved	R	0
7	P_TWI0_SCLK_ST	P_TWI0_SCLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
6	P_KS_OUT0_ST	P_KS_OUT0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
5	P_KS_OUT1_ST	P_KS_OUT1 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
4	P_KS_OUT2_ST	P_KS_OUT2 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
3:0	-	Reserved	R	0

30.5.25 PAD_ST1

PAD Schmitt Trigger enable Register1
Offset = 0x0070

Bits	Name	Description	Access	Reset
31	DSI_DP2_ST	DSI_DP2 PAD Schmitt trigger enable 1:enable Schmitt trigger	RW	0

		0:disable Schmitt trigger		
30	DSI_DN2_ST	DSI_DN2 PAD Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
29	P_I2S_LRCLK0_ST	P_I2S_LRCLK0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
28	-	Reserved	RW	0
27	P_UART3_CTSB_ST	P_UART3_CTSB pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
26	P_UART3_RTSB_ST	P_UART3_RTSB pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
25	P_UART3_RX_ST	P_UART3_RX pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
24	P_UART2_RTSB_ST	P_UART2_RTSB pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
23	P_UART2_CTSB_ST	P_UART2_CTSB pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
22	P_UART2_RX_ST	P_UART2_RX pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
21	P_ETH_RXD0_ST	P_ETH_RXD0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
20	P_ETH_RXD1_ST	P_ETH_RXD1 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
19	P_ETH_CRS_DV_ST	P_ETH_CRS_DV pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
18	P_ETH_RX_ER_ST	P_ETH_RX_ER pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
17	P_ETH_TXD1_ST	P_ETH_TXD1 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
16:13	-	Reserved	R	0
12	OAP_ST	OAP PAD schmitt trigger enable 1:enable schmitt trigger 0:disable schmitt trigger	RW	0
11	P_PCM1_CLK_ST	P_PCM1_CLK PAD Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
10	P_PCM1_IN_ST	P_PCM1_IN PAD Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
9	P_PCM1_SYNC_ST	P_PCM1_SYNC PAD Schmitt trigger enable	RW	0

		1:enable Schmitt trigger 0:disable Schmitt trigger		
8	P_TWI1_SCLK_ST	P_TWI1_SCLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
7	P_TWI1_SDATA_ST	P_TWI1_SDATA pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
6	P_TWI2_SCLK_ST	P_TWI2_SCLK pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	1
5	P_TWI2_SDATA_ST	P_TWI2_SDATA pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
4	P_SPI0_MOSI_ST	P_SPI0_MOSI pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
3	P_SPI0_MISO_ST	P_SPI0_MISO pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
2	P_SPI0_SS_ST	P_SPI0_SS pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
1	P_I2S_BCLK0_ST	P_I2S_BCLK0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0
0	P_I2S_MCLK0_ST	P_I2S_MCLK0 pad Schmitt trigger enable 1:enable Schmitt trigger 0:disable Schmitt trigger	RW	0

30.5.26 PAD_CTL

PAD Control Register
Offset = 0x0074

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	SPI0_CLR	0:The PADs used as SPI0 function can not controlled by PADEN bit. They are always enabled. 1:Clear this default state to make the PADs used as SPI0 function controlled by PADEN bit.	RW	0
1	PADEN	PAD Enable. **All** of the PAD are enabled (Not high-z) with their functions determined by the multi-function register's values. 0:Disable 1:Enable	RW	0
0	-	Reserved	R	0

30.5.27 PWM_CTL4~5

PWMx Output Control Register (x =4~5)
Offset = 0x0068 + 4 * x

Bits	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active	RW	0
19:10	DUTY_ACTIVE	The PWM clk cycle within active period	RW	0
9:0	DUTY_ALL	The PWM clk cycle within a whole PWM period	RW	0

30.5.28 PAD_DRV0

PAD Drive Capacity0 Select Register
Offset = 0x0080

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:28	SIRQ012	P_SIRQ[0:2] PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
27:24	-	Reserved	-	-
23:22	RMII_TXD01_TXEN	P_ETH_TXD01, P_ETH_TX_EN PAD driving strength select. 00:Level1 01:Level3 10:Level5 11:Reserved	RW	0
21:20	RMII_RXER	P_ETH_RX_ER PAD driving strength select. 00:Level1 01:Level2 10:Level4 11:Reserved	RW	0
19:18	RMII_CRS_DV	RMII_CRS_DV PAD driving strength select. 00:Level1 01:Level2 10:Level4 11:Reserved	RW	0
17:16	RMII_RXD10	P_ETH_RXD1, P_ETH_RXD0 PAD driving strength select. 00:Level1 01:Level2 10:Level4 11:Reserved	RW	0
15:14	RMII_REF_CLK	P_ETH_REF_CLK PAD driving strength select. 00:Level1 01:Level3 10:Level5 11:Reserved	RW	0

13:12	SMI_MDC_MDIO	P_ETH_MDC, P_ETH_MDIO PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
11:10	I2S_D0	P_I2S_D0 PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
9:8	I2S_BCLK0	P_I2S_BCLK0 PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
7:6	I2S3	P_I2S_LRCLK0, P_I2S_MCLK0, P_I2S_D1 PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
5:4	I2S13	P_I2S_BCLK1, P_I2S_LRCLK1, P_I2S_MCLK1 PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
3:2	PCM1	P_PCM1_IN, P_PCM1_CLK, P_PCM1_SYNC, P_PCM1_OUT PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
1:0	KS_IN[0:3]	P_KS_IN[0:3] PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0

30.5.29 PAD_DRV1

PAD Drive Capacity1 Select Register
Offset = 0x0084

Bits	Name	Description	Access	Reset
31:30	KS_OUT[0:2]	P_KS_OUT[0:2] PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
29:28	LVDS_ALL	LVDS PAD driving strength select. 00:Level1	RW	0

		01:Level2 10:Level3 11:Reserved		
27:26	LCD_DSI	P_LCD0_D[17:18], DSI_DP3, DSI_DN3, DSI_DP1, DSI_DN1, DSI_CP, DSI_CN PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
25:24	DSI	DSI_DP0, DSI_DN0, DSI_DP2, DSI_DN2 PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
23:22	SD0_D0_D3	P_SD0_D[0:3] PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Level5	RW	0
21:20	SD1_D0_D3	P_SD1_D[0:3] PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
19:18	SD0_CMD	P_SD0_CMD PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Level5	RW	0
17:16	SD0_CLK	P_SD0_CLK PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Level5	RW	0
15:14	SD1_CMD	P_SD1_CMD PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
13:12	SD1_CLK	P_SD1_CLK PAD driving strength select. 00:Level1 01:Level2 10:Level4 11:Reserved	RW	0
11:10	SPI0_ALL	P_SPI0_SCLK, P_SPI0_SS, P_SPI0_MISO, P_SPI0_MOSI PAD driving strength select. 00:Level1 01:Level2 10:Level4	RW	0

		11:Reserved		
9:0	-	Reserved	R	0

30.5.30 PAD_DRV2

PAD Drive Capacity2 Select Register
Offset = 0x0088

Bits	Name	Description	Access	Reset
31:30	UART0_RX	P_UART0_RX PAD driving strength select. 00:Level1 01:Level2 10:Level4 11:Reserved	RW	0
29:28	UART0_TX	P_UART0_TX PAD driving strength select. 00:Level1 01:Level2 10:Level4 11:Reserved	RW	0
27:26	UART2_ALL	P_UART2_RX, P_UART2_TX, P_UART2_RTSB, P_UART2_CTSB PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
25	-	Reserved	R	0
24:23	TWI0_ALL	P_TWI0_SCLK, P_TWI0_SDATA PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
22:21	TWI12_ALL	P_TWI1_SCLK, P_TWI1_SDATA, P_TWI2_SCLK, P_TWI2_SDATA PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
20	-	Reserved	R	0
19:18	SENS0_PCLK	P_SENSOR0_PCLK PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
17:14	-	Reserved	R	0
13:12	SENS0_CKOUT	P_SENSOR0_CKOUT PAD driving strength select. 00:Level1 01:Level2 10:Level3	RW	0

		11:Reserved		
11:4	-	Reserved	R	0
3:2	UART3_ALL	P_UART3_RX, P_UART3_TX, P_UART3_RTSB, P_UART3_CTSB PAD driving strength select. 00:Level1 01:Level2 10:Level3 11:Reserved	RW	0
1:0	-	Reserved	R	0

30.5.31 INTC_EXTCTL

External Interrupt Control and Status Register (VDD)
Offset = 0x0200

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:22	E0TYPE	External Interrupt 0 Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21	E0EN	Enable external interrupt 0(IRQ) 0 Disable 1 Enable	RW	0
20	SIRQ0_CLK_SEL	External Interrupt SIRQ0 sample clk select 0:32K 1:24M	RW	0
19:17	-	Reserved	-	-
16	E0PD	External Interrupt 0 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 0 is edge-triggered, this bit must be cleared by software after detected.	RW	0
15:11	-	Reserved	-	-
15:14	E1TYPE	External Interrupt 1 Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13	E1EN	Enable External interrupt 1(IRQ) 0 Disable 1 Enable	RW	0
12	SIRQ1_CLK_SEL	External Interrupt SIRQ1 sample clk select 0:32K 1:24M	RW	0
11:9	-	Reserved	-	-
8	E1PD	External Interrupt 1 Pending 0 External interrupt source 1 is not active. 1 External interrupt source 1 is active.	RW	0

		Write 1 to the bit will clear it. If external interrupt source 1 is edge-triggered, this bit must be cleared by software after detected.		
7:6	E2TYPE	External Interrupt 2 Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5	E2EN	Enable external interrupt 2(IRQ) 0 Disable 1 Enable	RW	0
4	SIRQ2_CLK_SEL	External Interrupt SIRQ2 sample clk select 0:32K 1:24M	RW	0
3:1	-	Reserved	-	-
0	E2PD	External Interrupt 2 Pending 0 External interrupt source 2 is not active. 1 External interrupt source 2 is active. Write 1 to the bit will clear it. If external interrupt source 2 is edge-triggered, this bit must be cleared by software after detected.	RW	0

30.5.32 INTC_GPIOCTL

GPIO Interrupt Type Control Register
Offset = 0x0204

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	GPIOE_CLK_SEL	GPIOE Interrupt sample clk select 0:32K 1:24M	RW	0
21	GEEN	Enable GPIOE interrupt 0 Disable 1 Enable	RW	0
20	GEPD	GPIOE Interrupt Pending 0 GPIOE interrupt source is not active. 1 GPIOE interrupt source is active. Write 1 to the bit will clear it. If GPIOE is edge-triggered, this bit must be cleared by software after detected.	RW	0
19:18	-	Reserved	-	-
17	GPIOD_CLK_SEL	GPIOD Interrupt sample clk select 0:32K 1:24M	RW	0
16	GDEN	Enable GPIOD interrupt 0 Disable 1 Enable	RW	0
15	GDPD	GPIOD Interrupt Pending 0 GPIOD interrupt source is not active. 1 GPIOD interrupt source is active. Write 1 to the bit will clear it. If GPIOD is edge-triggered, this bit must be cleared by	RW	0

		software after detected.		
14:13	-	Reserved	-	-
12	GPIOC_CLK_SEL	GPIOC Interrupt sample clk select 0:32K 1:24M	RW	0
11	GCEN	Enable GPIOC interrupt 0 Disable 1 Enable	RW	0
10	GCPD	GPIOC Interrupt Pending 0 GPIOC interrupt source is not active. 1 GPIOC interrupt source is active. Write 1 to the bit will clear it. If GPIOC is edge-triggered, this bit must be cleared by software after detected.	RW	0
9:8	-	Reserved	-	-
7	GPIOB_CLK_SEL	GPIOB Interrupt sample clk select 0:32K 1:24M	RW	0
6	GBEN	Enable GPIOB interrupt 0 Disable 1 Enable	RW	0
5	GBPD	GPIOB Interrupt Pending 0 GPIOB interrupt source is not active. 1 GPIOB interrupt source is active. Write 1 to the bit will clear it. If GPIOB is edge-triggered, this bit must be cleared by software after detected.	RW	0
4:3	-	Reserved	-	-
2	GPIOA_CLK_SEL	GPIOA Interrupt sample clk select 0:32K 1:24M	RW	0
1	GAEN	Enable GPIOA interrupt 0 Disable 1 Enable	RW	0
0	GAPD	GPIOA Interrupt Pending 0 GPIOA interrupt source is not active. 1 GPIOA interrupt source is active. Write 1 to the bit will clear it. If GPIOA is edge-triggered, this bit must be cleared by software after detected.	RW	0

30.5.33 INTC_GPIOA_PD

GPIOA Interrupt Pending Register (VDD)
Offset = 0x0208

Bits	Name	Description	Access	Reset
31:0	GPIOA_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOA number. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	R	x

30.5.34 INTC_GPIOA_MSK

GPIOA Interrupt Mask Register (VDD)
Offset = 0x020c

Bits	Name	Description	Access	Reset
31:0	GPIOA_MSK	GPIOA Interrupt Mask bit. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	RW	0

30.5.35 INTC_GPIOB_PD

GPIOB Interrupt Pending Register (VDD)
Offset = 0x0210

Bits	Name	Description	Access	Reset
31:0	GPIOB_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOB number. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	R	x

30.5.36 INTC_GPIOB_MSK

GPIOB Interrupt Mask Register (VDD)
Offset = 0x0214

Bits	Name	Description	Access	Reset
31:0	GPIOB_MSK	GPIOB Interrupt Mask bit. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	RW	0

30.5.37 INTC_GPIOC_PD

GPIOC Interrupt Pending Register (VDD)
Offset = 0x0218

Bits	Name	Description	Access	Reset
31:0	GPIOC_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOC number. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	R	x

30.5.38 INTC_GPIOC_MSK

GPIOC Interrupt Mask Register (VDD)
Offset = 0x021C

Bits	Name	Description	Access	Reset
31:0	GPIOC_MSK	GPIOC Interrupt Mask bit. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	RW	0

30.5.39 INTC_GPIOD_PD

GPIOD Interrupt Pending Register (VDD)
Offset = 0x0220

Bits	Name	Description	Access	Reset
31:0	GPIOD_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOD number. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	R	x

30.5.40 INTC_GPIOD_MSK

GPIOD Interrupt Mask Register (VDD)
Offset = 0x0224

Bits	Name	Description	Access	Reset
31:0	GPIOD_MSK	GPIOD Interrupt Mask bit. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	RW	0

30.5.41 INTC_GPIOE_PD

GPIOE Interrupt Pending Register (VDD)
Offset = 0x0228

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	GPIOE_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOE number. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	R	x

30.5.42 INTC_GPIOE_MSK

GPIOE Interrupt Mask Register (VDD)
Offset = 0x022C

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	GPIOE_MSK	GPIOE Interrupt Mask bit. 0:Interrupt source n request is not active 1:Interrupt source n request is active.	RW	0

30.5.43 INTC_GPIOA_TYPE0

GPIOA Interrupt Pending Register0 (VDD)
Offset = 0x0230

Bits	Name	Description	Access	Reset
31:30	GA31_TYPE	GPIOA31 Interrupt Type 00:High level active.	RW	0

		01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.		
29:28	GA30_TYPE	GPIOA30 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GA29_TYPE	GPIOA29 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GA28_TYPE	GPIOA28 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GA27_TYPE	GPIOA27 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21:20	GA26_TYPE	GPIOA26 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GA25_TYPE	GPIOA25 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GA24_TYPE	GPIOA24 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GA23_TYPE	GPIOA23 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GA22_TYPE	GPIOA22 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GA21_TYPE	GPIOA21 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

9:8	GA20_TYPE	GPIOA20 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GA19_TYPE	GPIOA19 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GA18_TYPE	GPIOA18 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GA17_TYPE	GPIOA17 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GA16_TYPE	GPIOA16 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.44 INTC_GPIOA_TYPE1

GPIOA Interrupt Pending Register1 (VDD)
Offset = 0x0234

Bits	Name	Description	Access	Reset
31:30	GA15_TYPE	GPIOA15 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
29:28	GA14_TYPE	GPIOA14 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GA13_TYPE	GPIOA13 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GA12_TYPE	GPIOA12 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GA11_TYPE	GPIOA11 Interrupt Type	RW	0

		00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.		
21:20	GA10_TYPE	GPIOA10 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GA9_TYPE	GPIOA9 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GA8_TYPE	GPIOA8 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GA7_TYPE	GPIOA7 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GA6_TYPE	GPIOA6 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GA5_TYPE	GPIOA5 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GA4_TYPE	GPIOA4 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GA3_TYPE	GPIOA3 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GA2_TYPE	GPIOA2 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GA1_TYPE	GPIOA1 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered.	RW	0

		11:Falling edge-triggered.		
1:0	GA0_TYPE	GPIOA0 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.45 INTC_GPIOB_TYPE0

GPIOB Interrupt Pending Register0 (VDD)
Offset = 0x0238

Bits	Name	Description	Access	Reset
31:30	GB31_TYPE	GPIOB31 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
29:28	GB30_TYPE	GPIOB30 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GB29_TYPE	GPIOB29 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GB28_TYPE	GPIOB28 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GB27_TYPE	GPIOB27 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21:20	GB26_TYPE	GPIOB26 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GB25_TYPE	GPIOB25 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GB24_TYPE	GPIOB24 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered.	RW	0

		11:Falling edge-triggered.		
15:14	GB23_TYPE	GPIOB23 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GB22_TYPE	GPIOB22 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GB21_TYPE	GPIOB21 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GB20_TYPE	GPIOB20 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GB19_TYPE	GPIOB19 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GB18_TYPE	GPIOB18 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GB17_TYPE	GPIOB17 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GB16_TYPE	GPIOB16 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.46 INTC_GPIOB_TYPE1

GPIOB Interrupt Pending Register1 (VDD)
Offset = 0x023c

Bits	Name	Description	Access	Reset
31:30	GB15_TYPE	GPIOB15 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

29:28	GB14_TYPE	GPIOB14 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GB13_TYPE	GPIOB13 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GB12_TYPE	GPIOB12 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GB11_TYPE	GPIOB11 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21:20	GB10_TYPE	GPIOB10 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GB9_TYPE	GPIOB9 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GB8_TYPE	GPIOB8 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GB7_TYPE	GPIOB7 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GB6_TYPE	GPIOB6 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GB5_TYPE	GPIOB5 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GB4_TYPE	GPIOB4 Interrupt Type 00:High level active. 01:Low level active.	RW	0

		10:Rising edge-triggered. 11:Falling edge-triggered.		
7:6	GB3_TYPE	GPIOB3 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GB2_TYPE	GPIOB2 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GB1_TYPE	GPIOB1 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GB0_TYPE	GPIOB0 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.47 INTC_GPIOC_TYPE0

GPIOC Interrupt Pending Register0 (VDD)
Offset = 0x0240

Bits	Name	Description	Access	Reset
31:30	GC31_TYPE	GPIOC31 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
29:28	GC30_TYPE	GPIOC30 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GC29_TYPE	GPIOC29 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GC28_TYPE	GPIOC28 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GC27_TYPE	GPIOC27 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered.	RW	0

		11:Falling edge-triggered.		
21:20	GC26_TYPE	GPIOC26 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GC25_TYPE	GPIOC25 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GC24_TYPE	GPIOC24 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GC23_TYPE	GPIOC23 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GC22_TYPE	GPIOC22 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GC21_TYPE	GPIOC21 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GC20_TYPE	GPIOC20 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GC19_TYPE	GPIOC19 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GC18_TYPE	GPIOC18 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GC17_TYPE	GPIOC17 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GC16_TYPE	GPIOC16 Interrupt Type 00:High level active.	RW	0

		01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.		

30.5.48 INTC_GPIOC_TYPE1

GPIOC Interrupt Pending Register1 (VDD)
Offset = 0x0244

Bits	Name	Description	Access	Reset
31:30	GC15_TYPE	GPIOC15 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
29:28	GC14_TYPE	GPIOC14 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GC13_TYPE	GPIOC13 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GC12_TYPE	GPIOC12 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GC11_TYPE	GPIOC11 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21:20	GC10_TYPE	GPIOC10 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GC9_TYPE	GPIOC9 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GC8_TYPE	GPIOC8 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GC7_TYPE	GPIOC7 Interrupt Type 00:High level active. 01:Low level active.	RW	0

		10:Rising edge-triggered. 11:Falling edge-triggered.		
13:12	GC6_TYPE	GPIOC6 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GC5_TYPE	GPIOC5 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GC4_TYPE	GPIOC4 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GC3_TYPE	GPIOC3 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GC2_TYPE	GPIOC2 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GC1_TYPE	GPIOC1 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GC0_TYPE	GPIOC0 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.49 INTC_GPIOD_TYPE0

GPIOD Interrupt Pending Register0 (VDD)
Offset = 0x0248

Bits	Name	Description	Access	Reset
31:30	GD31_TYPE	GPIOD31 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
29:28	GD30_TYPE	GPIOD30 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered.	RW	0

		11:Falling edge-triggered.		
27:26	GD29_TYPE	GPIOD29 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GD28_TYPE	GPIOD28 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GD27_TYPE	GPIOD27 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21:20	GD26_TYPE	GPIOD26 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
19:18	GD25_TYPE	GPIOD25 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GD24_TYPE	GPIOD24 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GD23_TYPE	GPIOD23 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GD22_TYPE	GPIOD22 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GD21_TYPE	GPIOD21 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GD20_TYPE	GPIOD20 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GD19_TYPE	GPIOD19 Interrupt Type 00:High level active.	RW	0

		01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.		
5:4	GD18_TYPE	GPIOD18 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GD17_TYPE	GPIOD17 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GD16_TYPE	GPIOD16 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.50 INTC_GPIOD_TYPE1

GPIOD Interrupt Pending Register1 (VDD)
Offset = 0x024C

Bits	Name	Description	Access	Reset
31:30	GD15_TYPE	GPIOD15 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
29:28	GD14_TYPE	GPIOD14 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
27:26	GD13_TYPE	GPIOD13 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
25:24	GD12_TYPE	GPIOD12 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
23:22	GD11_TYPE	GPIOD11 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
21:20	GD10_TYPE	GPIOD10 Interrupt Type 00:High level active.	RW	0

		01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.		
19:18	GD9_TYPE	GPIOD9 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
17:16	GD8_TYPE	GPIOD8 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
15:14	GD7_TYPE	GPIOD7 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
13:12	GD6_TYPE	GPIOD6 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
11:10	GD5_TYPE	GPIOD5 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
9:8	GD4_TYPE	GPIOD4 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
7:6	GD3_TYPE	GPIOD3 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GD2_TYPE	GPIOD2 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GD1_TYPE	GPIOD1 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GD0_TYPE	GPIOD0 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.5.51 INTC_GPIOE_TYPE

GPIOE Interrupt Pending Register0 (VDD)
Offset = 0x0250

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:6	GE3_TYPE	GPIOE3 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
5:4	GE2_TYPE	GPIOE2 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
3:2	GE1_TYPE	GPIOE1 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0
1:0	GE0_TYPE	GPIOE0 Interrupt Type 00:High level active. 01:Low level active. 10:Rising edge-triggered. 11:Falling edge-triggered.	RW	0

30.6 Application Note

30.6.1 GPIO Operation

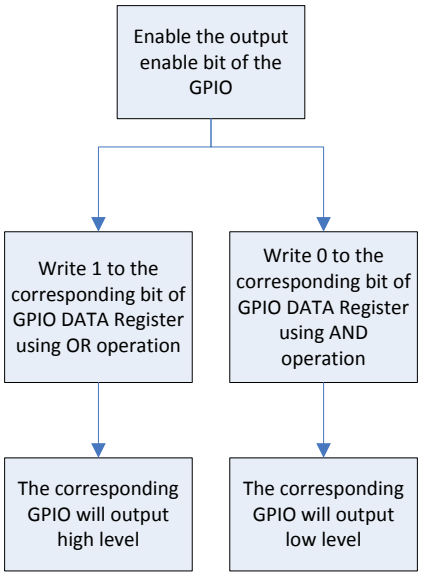


Figure 30-3 GPIO Output Procedure

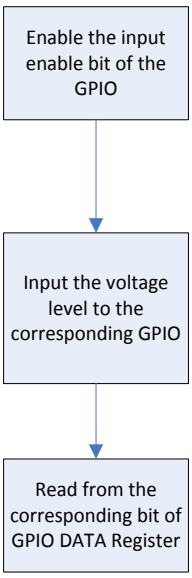


Figure 30-4 GPIO Input Procedure

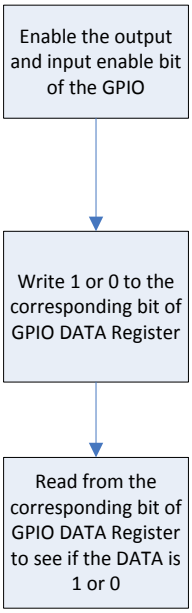


Figure 30-5 GPIO Loop Procedure

30.6.2 PWM Operation

The common application diagram of PWM is as followed:

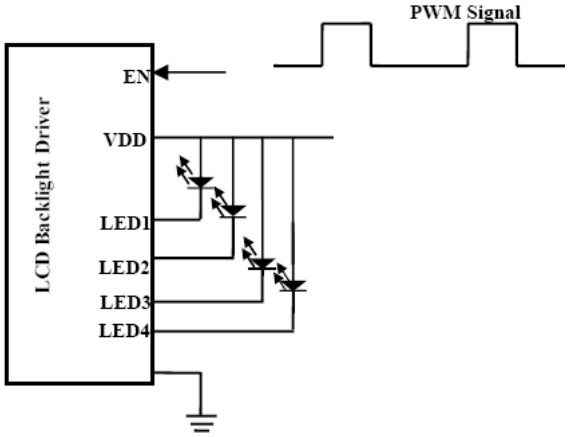


Figure 30-6 PWM Application Diagram

The PWM signal output from S500 controls the Enable signal of LCD backlight driver IC. So the driver IC is modulated by the PWM. The higher the duty occupancy of PWM signal, the brighter the LCD displays. In other words, changing the PWM duty can change the brightness of the LCD.

The maximum frequency of PWM signal is relevant to the switch speed of the backlight IC and the LED. If the frequency is too high, backlight IC and the LED cannot have enough time to switch, so that the change of brightness is not obvious through adjusting of PWM duty occupancy.

The frequency of PWM is best not to be in the frequency range of audio (20Hz~20KHz), for the risk of producing noise.

31 KEY Scan

31.1 Overview

KEY Scan module is used for key pad expansion, there are 4 working modes supported in Key Scan module. The four modes are Parallel Out/ Parallel In, Serial Out/Parallel In, Serial Out/Serial In and IO Scan. The number of keys and multi-key are different in each mode. Features of Key Scan module are listed below:

- Matrix of Parallel Out/Parallel In can be programmed to 4*3
- Matrix of Serial Out/Parallel In can be programmed to 8*4 or 16*4
- Matrix of Serial Out/Serial In can be programmed to 8*8, 8*16 and 16*16
- The maximum number of key in IO scan Normal Mode is c_n^2+n (n is number of IO)
- The maximum number of key in IO scan Diode Mode is $2*c_n^2+n$ (n is number of IO)
- Supports programmable scan timing

31.2 Block Diagram

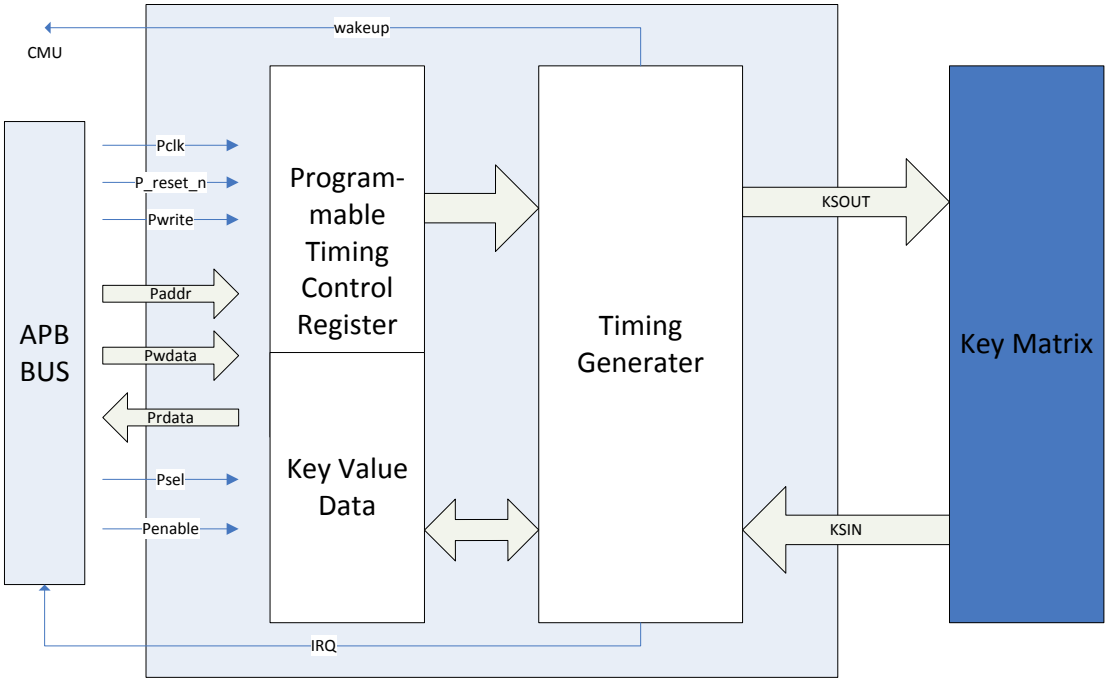


Figure 31-1 KEY Block Diagram

31.3 Function Description

There are 4 working modes supported in Key Scan module. They are Parallel Out/ Parallel In, Serial Out/Parallel In, Serial Out/Serial In and IO Scan. The number of key and multi-key is different in each mode.

31.3.1 Parallel Out/Parallel In

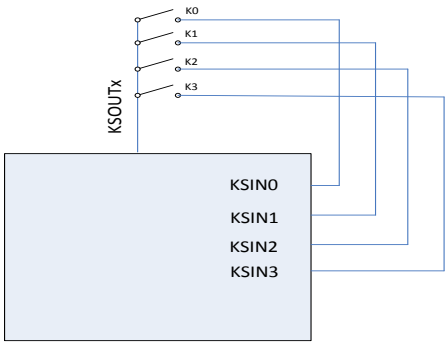


Figure 31-2 Parallel Out/Parallel In

The figure shows the key matrix in parallel out/parallel in. The matrix of parallel out/parallel in can be configured to 4Ksinx*3Ksoutx. There are pull-up resistances in KSINs.

The state machine of working is consists of 4 stages:

Idle	Debounce	Scan	Wait	Idle

Idle is active when no key is pressed. When any key pressed, it will go into Debounce state in order to avoid bouncing. During the Scan, each KSOUTx outputs low voltage in turn. KSOUTx's output can be set open-drain or push-pull.

In this mode, key value data were stored in KEY_DAT0. On the condition of matrix 4*3, key value described as below.

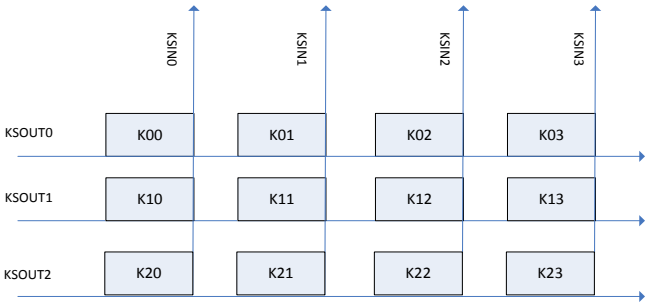


Figure 31-3 Parallel Out/Parallel In key matrix

Table 31-1 Parallel Out/Parallel In key value

Key	**K00**	**K01**	**K02**	**K03**	**K10**	**K11**
Value	0xFFFFFFFE	0xFFFFFFFD	0xFFFFFFFB	0xFFFFFFF7	0xFFFFFFEF	0xFFFFFFDF
Key	**K12**	**K13**	**K20**	**K21**	**K22**	**K23**
Value	0xFFFFFFBF	0xFFFFFF7F	0xFFFFFEFF	0xFFFFFDFF	0xFFFFFBFF	0xFFFFF7FF

31.3.2 Serial Out/Parallel In

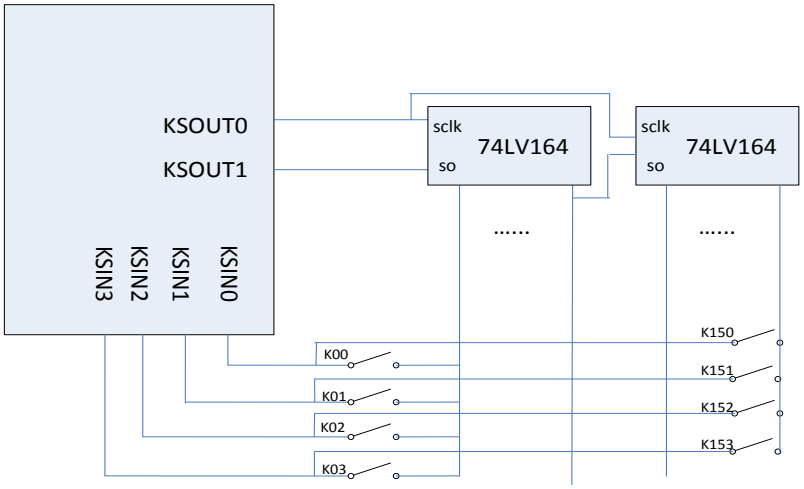


Figure 31-4 Serial Out/Parallel In

Serial Out/Parallel In mode may enlarge the number of supported key. In this mode, 74LV164 should be used. One or two 76LV164 may extend key numbers to 8*4 or 16*4. KSOUT0 connect to SCLK of 74LV164, KSOUT1 connect to SO of 74LV164.

Key value is stored in KEY_DAT0 and KEY_DAT1 which described as below.

Table 31-2 Serial Out/Parallel In Key value in KEY_DAT0

Key	K00	K01	K02	K03	K10	K11	K12	K13
Value	0xFFFFFFFE	0xFFFFFFFD	0xFFFFFFFB	0xFFFFFFF7	0xFFFFFFEF	0xFFFFFFDF	0xFFFFFFBF	0xFFFFFF7F
Key	K20	K21	K22	K23	K30	K31	K32	K33
Value	0xFFFFFEFF	0xFFFFFDFF	0xFFFFFBFF	0xFFFFF7FF	0xFFFFEFFF	0xFFFFDFFF	0xFFFFBFFF	0xFFFF7FFF
Key	K40	K41	K42	K43	K50	K51	K52	K54
Value	0xFFFEFFFF	0xFFFDFFFF	0xFFFBFFFF	0xFFF7FFFF	0xFFEFFFFF	0xFFDFFFFF	0xFFBFFFFF	0xFF7FFFFF
Key	K60	K61	K62	K63	K70	K71	K72	K73
Value	0xFEFFFFFF	0xFDFFFFFF	0xFBFFFFFF	0xF7FFFFFF	0xEFFFFFFF	0xDFFFFFFF	0xBFFFFFFF	0x7FFFFFFF

Table 31-3 Serial Out/Parallel In Key value in KEY_DAT1

Key	K80	K81	K82	K83	K90	K91	K92	K93
Value	0xFFFFFFFE	0xFFFFFFFD	0xFFFFFFFB	0xFFFFFFF7	0xFFFFFFEF	0xFFFFFFDF	0xFFFFFFBF	0xFFFFFF7F
Key	K100	K101	K102	K103	K110	K111	K112	K113
Value	0xFFFFFEFF	0xFFFFFDFF	0xFFFFFBFF	0xFFFFF7FF	0xFFFFEFFF	0xFFFFDFFF	0xFFFFBFFF	0xFFFF7FFF
Key	K120	K121	K122	K123	K130	K131	K132	K133
Value	0xFFFEFFFF	0xFFFDFFFF	0xFFFBFFFF	0xFFF7FFFF	0xFFEFFFFF	0xFFDFFFFF	0xFFBFFFFF	0xFF7FFFFF
Key	K140	K141	K142	K143	K150	K151	K152	K153
Value	0xFEFFFFFF	0xFDFFFFFF	0xFBFFFFFF	0xF7FFFFFF	0xEFFFFFFF	0xDFFFFFFF	0xBFFFFFFF	0x7FFFFFFF

31.3.3 Serial Out/Serial In

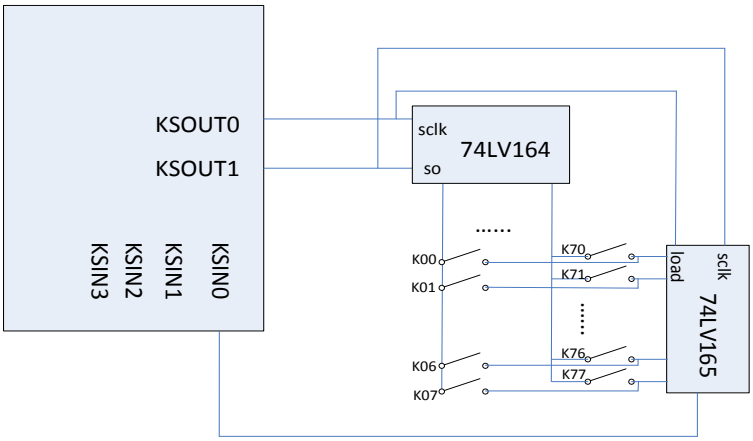


Figure 31-5 Serial Out/Parallel In

Serial Out/Serial In mode may extend key numbers. In this mode, 74LV164 and 74LV165 must be used. 74LV164 and 74LV165 share the same control signals. KSOUT0 acts as SCLK of 74LV164 or LOAD of 74LV165. KSOUT1 acts as SO of 74LV164 or SCLK of 74LV165. KSIN0 reads from 74LV165. Outputs of 74LV164 and inputs of 74LV165 form key matrix. Matrix of 8*8(one 74LV164 and one 74LV165), 8*16(one 74LV164 and two 74LV165) and 16*16(two 74LV164 and two 74LV165) are supported. With the different of key matrix, key value is stored in different KEY_DATx. The matrix of 16*16 will use as many as 8 KEY_DAT registers. Matrix of 8*8 uses KEY_DAT [0:1]. Matrix of 8*16 uses KEY_DAT [0:3]. The key value's format is similar to that in Serial Out/Parallel In mode. Idle time is 3ms in this mode.

The timing of Serial Out/Serial In mode is below:

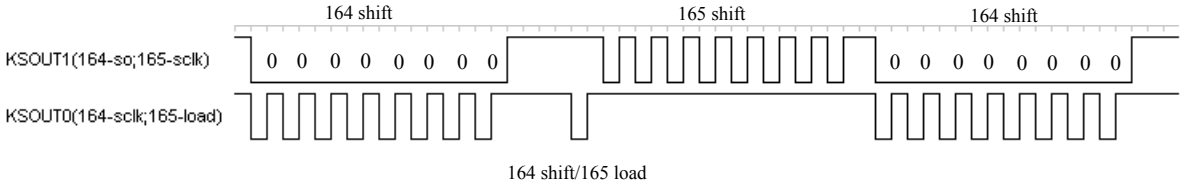


Figure 31-6 Timing of 8*8 Matrix in Idle

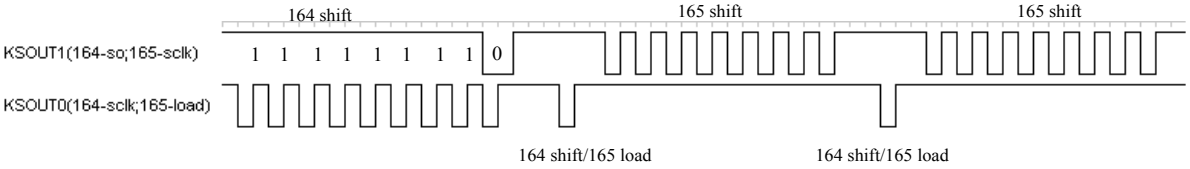


Figure 31-7 Timing of 8*8 Matrix in Scan

31.3.4 IO Scan

In this mode, the controller detects the connection between each pair of IOs and the connection between IO to GND automatically. Two modes are supported in IO scans: Normal Mode and Diode Mode.

31.4 Register List

Table 31-4 KEY Registers Address

Name	Physical Base Address
KEY	0xB01A0000

Table 31-5 KEY Controller Registers

Offset	Register Name	Description
0x0000	KEY_CTL	Key Control Register
0x0004	KEY_DAT0	Key Data Register0
0x0008	KEY_DAT1	Key Data Register1
0x000C	KEY_DAT2	Key Data Register2
0x0010	KEY_DAT3	Key Data Register3
0x0014	KEY_DAT4	Key Data Register4
0x0018	KEY_DAT5	Key Data Register5
0x001C	KEY_DAT6	Key Data Register6
0x0020	KEY_DAT7	Key Data Register7

Note:Register Key_CTL&Key_DATx's power comes from VDD.

31.5 Register Description

31.5.1 KEY_CTL

Key control Register
Offset = 0x00

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:21	WTS	Key Scan Wait Time Select. Key Scan Wait Time=WTS*32ms 000:0ms 001:32ms 010:64ms 011:96ms 100:128ms 101:160ms 110:192ms 111:224ms	RW	0
20:19	PRS	Key Scan Period Select: 00:20ms 01:40ms 10:80ms 11:160ms	RW	0
18:17	DTS	Key Scan Debounce Time Select. 00:10ms 01:20ms 10:40ms 11:No debounce time(Debounce disable)	RW	0
16	IRCL	Key Scan IRQ Cleared (only used when shutting down APB Clock).	R	1
15	IRP	Key Scan IRQ Pending Bit. 0:No IRQ 1:IRQ Writing 1 to the bit will clear the bit.	RW	0
14	IREN	Key Scan IRQ Enable. 0:Disable 1:Enable	RW	0

13	IOMS	IO Scan mode select: 0:Normal Mode 1:Diode Mode This bit is available on the condition that KMS is set as 11.	RW	0
12	OTYP	KSOUT output type, Only for Parallel Out Key mode 0:Opendrain output 1:Push pull output	RW	0
11:5	PENM	Pin [A:G] enable in all modes. 0:mask pin 1:enable pin Pin [A:G] are corresponding to KSIN[0:3],KSOUT[0:2].These bits must be set to the correspond state in different modes. When in IO mode, 1 will enable the internal pull-up resistant and OEN/IEN of the corresponding pin. When in the all Parallel In mode, 1 will enable the internal pull-up resistant and IEN of the corresponding KSIN. When in the Serial/Parallel Out mode, 1 will enable the OEN of the corresponding KSOUT. When in the Serial In mode, 1 will enable the IEN of KSIN0.	RW	0
4:3	MXS	Matrix Select 00:8*8(one 164 and one 165) in Serial Out/Serial In mode 8*4(KSIN)in Serial Out/Parallel In mode 3(KSOUT)*4(KSIN) in Parallel Out/Parallel In mode 01:8*16(one 164 and two 165) in Serial Out/Serial In mode 16*4(KSIN) in Serial Out/Parallel In mode 10:16*16(two 164 and two 165) in Serial Out/Serial In mode 11:Reserved	RW	0
2:1	KMS	Key scan mode select: 00:Parallel Out/Parallel In 01:Serial Out/Parallel In 10:Serial Out/Serial In 11:IO Scan	RW	0
0	KEN	Key Scan Enable. 0:Disable 1:Enable	RW	0

31.5.2 KEY_DAT0

Key Data Register0
Offset = 0x04

Bit	Name	Description	Access	Reset
31:0	KDAT	Key Data.	R	0xFFFFFFFF

Key Scan Data Register0's definition in IO Scan mode

Bit	Name	Description	Access	Reset
31:28	-	Reserved	R	0xF
27	F-GN	Key value of F to G in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
26	E-GN	Key value of E to G in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1

25	E-FN	Key value of E to F in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
24	D-GN	Key value of D to G in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
23	D-FN	Key value of D to F in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
22	D-EN	Key value of D to E in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
21	C-GN	Key value of C to G in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
20	C-FN	Key value of C to F in Normal and Diode Mode. 0:key pressed. 1:key not pressed.	R	1
19	C-EN	Key value of C to E in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
18	C-DN	Key value of C to D in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
17	B-GN	Key value of B to G in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
16	B-FN	Key value of B to F in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
15	B-EN	Key value of B to E in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
14	B-DN	Key value of B to D in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
13	B-CN	Key value of B to C in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
12	A-GN	Key value of A to G in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
11	A-FN	Key value of A to F in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
10	A-EN	Key value of A to E in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
9	A-DN	Key value of A to D in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
8	A-CN	Key value of A to C in Diode and Normal Mode. 0:key pressed.	R	1

		1:key not pressed.		
7	A-BN	Key value of A to B in Diode and Normal Mode. 0:key pressed. 1:key not pressed.	R	1
6	G-GND	Key value of G to GND. 0:key pressed. 1:key not pressed.	R	1
5	F-GND	Key value of F to GND. 0:key pressed. 1:key not pressed.	R	1
4	E-GND	Key value of E to GND. 0:key pressed. 1:key not pressed.	R	1
3	D-GND	Key value of D to GND. 0:key pressed. 1:key not pressed.	R	1
2	C-GND	Key value of C to GND. 0:key pressed. 1:key not pressed.	R	1
1	B-GND	Key value of B to GND. 0:key pressed. 1:key not pressed.	R	1
0	A-GND	Key value of A to GND. 0:key pressed. 1:key not pressed.	R	1

Note:In IO Scan mode, the mapping of point [A:G] to pin is fixed. A is corresponding to KSIN0. B is corresponding to KSIN1. C is corresponding to KSIN2. D is corresponding to KSIN3. E is corresponding to KSOUT0. F is corresponding to KSOUT1. G is corresponding to KSOUT2.

31.5.3 KEY_DAT1

Key Data Register1
Offset = 0x08

Bit	Name	Description	Access	Reset
31:0	KDAT	Key Data.	R	0xFFFFFFFF

Key Scan Data Register1's definition in IO Scan mode

Bit	Name	Description	Access	Reset
31:21	-	Reserved	R	1
20	G-FD	Key value of G to F in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
19	G-ED	Key value of G to E in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
18	F-ED	Key value of F to E in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
17	G-DD	Key value of G to D in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
16	F-DD	Key value of F to D in Diode Mode.	R	1

		0:key pressed. 1:key not pressed.		
15	E-DD	Key value of E toD in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
14	G-CD	Key value of G to C in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
13	F-CD	Key value of B to D in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
12	E-CD	Key value of E to C in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
11	D-CD	Key value of D to C in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
10	G-BD	Key value of G to B in Diode Mode. 0:key pressed. 1:key not pressed.		1
9	F-BD	Key value of F to B in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
8	E-BD	Key value of E to B in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
7	D-BD	Key value of D to B in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
6	C-BD	Key value of C to B in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
5	G-AD	Key value of G to A in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
4	F-AD	Key value of F to A in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
3	E-AD	Key value of E to A in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
2	D-AD	Key value of D to A in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
1	C-AD	Key value of C to A in Diode Mode. 0:key pressed. 1:key not pressed.	R	1
0	B-AD	Key value of B to A in Diode Mode 0:key pressed. 1:key not pressed.	R	1

Note:In IO Scan mode, the mapping of point [A:G] to pin is fixed. A is corresponding to KSIN0. B is corresponding to KSIN1. C is corresponding to KSIN2. D is corresponding to KSIN3. E is corresponding to KSOUT0. F is corresponding to KSOUT1. G is corresponding to KSOUT2.

31.5.4 KEY_DAT2

Key Data Register2
Offset = 0x0C

Bit	Name	Description	Access	Reset
31:0	KDAT	Key scan Data.	R	0xFFFFFFFF

31.5.5 KEY_DAT3

Key Data Register3
Offset = 0x10

Bit	Name	Description	Access	Reset
31:0	KDAT	Key scan Data.	R	0xFFFFFFFF

31.5.6 KEY_DAT4

Key Data Register4
Offset = 0x14

Bit	Name	Description	Access	Reset
31:0	KDAT	Key scan Data.	R	0xFFFFFFFF

31.5.7 KEY_DAT5

Key Data Register5
Offset = 0x18

Bit	Name	Description	Access	Reset
31:0	KDAT	Key scan Data.	R	0xFFFFFFFF

31.5.8 KEY_DAT6

Key Data Register6
Offset = 0x1C

Bit	Name	Description	Access	Reset
31:0	KDAT	Key scan Data.	R	0xFFFFFFFF

31.5.9 KEY_DAT7

Key Data Register7
Offset = 0x20

Bit	Name	Description	Access	Reset
31:0	KDAT	Key scan Data.	R	0xFFFFFFFF

31.6 Application Note

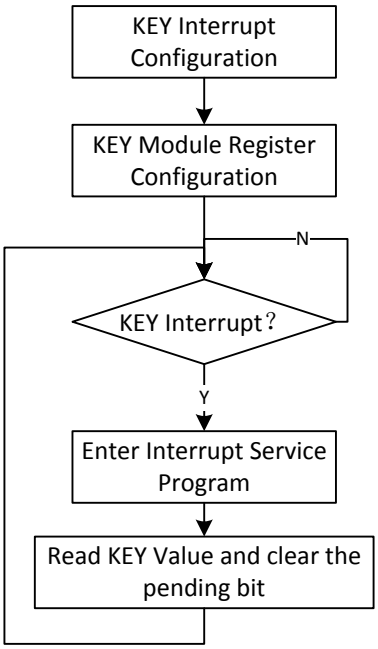


Figure 31-8 KEY Interrupt Configuration process

Appendix

Acronyms and Terms

ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
ALE	Address-Locked Enable
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
AV Data	Audio/Video Data
BIST	Built-in Self-Test
CLE	Command-Locked Enable
CMU	Clock Management Unit
CP0	System Control Coprocessor
CRC	Cyclic Redundancy Check
CSI	MIPI Camera Serial Interface
CVBS	Composite Video Broadcasting Signal
DAC	Digital-to-Analog Converter
DB	Decibel
DC	Direct Current
DCU	DDR SDRAM Control Unit
DE	Display Engine
DFI	DDR PHY Interface
DMA	Direct Memory Access
DMM	Dynamic Memory Management
DSI	MIPI Display Serial Interface
DSP	Digital Signal Processing
DVB	Digital Video Broadcasting
DVFS	Dynamic Voltage Frequency Scaling
EAV	End of Active Video
ECC	Error Correct Code
EMMC	Embedded Multi Media Card
FIFO	First In First Out
FIR	Fast Infrared
GPIO	General Purpose Input Output
HDCP	High -bandwidth Digital Content Protection
HDMI	High Definition Media Interface
I2S	Inter-IC Sound
IF	Interface
IR	Infrared
IrDA	Infrared Data Association
IRQ	Interrupt Request
JPEG	Joint Photographic Experts Group
LCD	Liquid Crystal Display
LCDC	Liquid Crystal Display Controller
Li-Ion	Lithium Ion (battery type)

LRADC	Low Resolution ADC
LVDS	Low voltage differential signaling
MAC	Multiplier Accumulator Control
MIPI	Mobile Industry Processor Interface
MIPS	Million Instructions per Second
MIR	Mid Infrared
MJPEG	Motion JPEG
MLC	Multi-level Cell
MMC	MultiMedia Card
MMU	Memory Management Unit
MPEG	Moving Picture Experts Group
MS	Memory stick card
NIC	Network in Chip
NOC	Network on Chip
NTSC	National Television Standards Committee
OLED	Polymer Light-Emitting Diode
OS	Operation System
PA	Power Amplifier
PAL	Phase Alteration Line
PCM	Pulse Code Modulation
PFM	Pulse Frequency Modulation
PLL	Phase-Locked Loop
PMU	Power Management Unit
PWM	Pulse Width Modulation
RGB	Red Green Blue
RISC	Reduced Instruction Set Computing
RSA	RSA Public-key Cryptosystems
RTC	Real-Time Clock
SAV	Start of Active Video
SD	Secure Digital
SIR	Slow Infrared
SLC	Single-Level Cell
SMC	State Machine Controller
SoC	System on Chip
SPEC	Specification
SPI	Serial Peripheral Interface
SPRAM	Scratch Pad RAM
SW	Software
TFT	Thin Film Transistor
THD	Total Harmonic Distortion
TLB	Translation Look-aside Buffer
TS(MPEG2 TS)	Transport Stream
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
USB HSIC	Universal Serial Bus Hi-Speed Inter-Chip
WMA	Windows Media Audio
WMV	Windows Media Video

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