A20

User Manual

Revision 1.1

Sep. 17, 2013

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Revision History

Revision	Date	Description
1.0	March 22, 2013	Initial version
1.1	Septermber 17, 2013	Modify TVD and TVE description

Allwinner Technology

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1.1. Overview

Allwinner A20 processor is a dual-core ARM Cortex-A7 mobile application solution designed for tablet and smart TV applications.

A20 processor is based on a dual-core ARM Cortex-A7 CPU architecture, which is the most energy efficient application processor from ARM so far and incorporates all the features of Cortex-A15. It also integrates the powerful ARM Mali400 MP2 GPU, delivering a reliable system performance as well as good game compatibility. Besides, A20 supports 2160p video decoding and H.264 HP 1080p video encoding.

Additionally, A20 processor features a wide range of interfaces and connectivity, including 4-CH CVBS in, 4-CH CVBS out, HDMI with HDCP, VGA, LVDS/RGB LCD, SATA, USB, and GMAC, etc. More importantly, A20 processor is pin-compatible with its predecessor A10, which greatly simplifies the product design process and makes the upgrade of a design much easier.

The A20 features are listed below:

Dual-Core CPU

- Dual Cortex-A7
  - ARMv7 ISA standard ARM instruction set
  - Thumb-2
  - Jazeller RCT
  - NEON Advanced SIMD
  - VFPv4 floating point
  - Hardware virtualization support
  - Large Physical Address Extensions(LPAE)
  - JTAG debug
  - One general timer for individual CPU
  - 32KB Instruction and 32KB Data L1 cache for individual CPU

Graphic Engine

- 3D
  - Mali400 MP2 GPU
  - Support OpenGL ES 2.0 / OpenVG 1.1 standard
- 2D
  - Support BLT and ROP2/3/4
  - Support 90° /180° /270° rotation
  - Support mirror/ alpha (plane and pixel alpha) /color key

– Format conversion: ARGB 8888/4444/1555, RGB565, MONO 1/2/4/8bpp, Palette 1/2/4/8bpp (input only), YUV 444/422/420

Memory

- **Internal BROM**

  – Support system boot from NAND Flash, SPI Nor Flash (SPI0), SD Card/TF card (SDC0/2)

  – Support system code download through USB OTG (USB0)

- **SDRAM**

  – Support DDR3/DDR3L/DDR2

  – Support 32-bit bus width

  – Support 2GB address space

- **NAND Flash**

  – Comply to ONFI 2.3 and Toggle 1.0

  – Support 64-bit ECC per 512 bytes or 1024 bytes

  – Support 8bits data bus width

  – Support 1.8V/3.3V signal voltage

  – Support 1K/2K/4K/8K/16K page size

  – Support up to 8 CE and 2 RB

  – Support system boot from NAND flash

  – Support SLC/MLC NAND and EF-NAND

  – Support SDR/DDR NAND interface

- **SD/MMC Interface**

  – Comply with eMMC standard specification V4.3

  – Comply with SD physical layer specification V3.0

  – Comply with SDIO card specification V2.0

  – Support 1/4/8 bits bus width

  – Support HS/DS/SDR12/SDR25 bus mode

  – Support eMMC mandatory and alternative boot operations

  – Support four independent SD/MMC/SDIO controllers

  – Support SDSC/SDHC/SDXC/MMC/ RS-MMC card

  – Support eMMC/iNand Flash

  – Support 1GB/2GB/4GB/8GB/16GB/32GB/64GB /128GB SD/MMC card

  – Support SDIO interrupt detection

  – Support descriptor-based internal DMA controller for efficient scatter and gather operations

System Resources

- **Timer**

  – 6 timers: clock source can be switched over 24M/32K for all timers, and external signals can be used as clock source for Timer4/5

  – Two 33-bit AVS counters

  – Watchdog to generate reset signal or interrupt

  – Real time counter for second, minute, hour, day, month, and year

- **High Speed Timer**

  – 4 channels

  – Clock source is fixed to AHB, and the pre-scale ranges from 1 to 16

  – 56-bit counter that can be separated to 24-bit high register and 32-bit low register

- **DMA**

  – 16 channels

  – Support data width of 8/32 bits

  – Support linear and IO address modes

- **CCU**

  – 8PLLs, a main 24MHz oscillator, an on-chip RC oscillator and a 32768Hz oscillator (optional)

- **GIC**

  – Support 16 SGIs, 16 PPIs, and 128 SPIs

  – Support ARM architecture security extensions

  – Support ARM architecture virtualization extensions

  – Support uniprocessor and multiprocessor environments

Video Engine (Phoenix 3.0)

- Video Decoding

  – Support picture size up to 3840x2160

  – Support decoding speed up to 1080p@60fps

  – Supported formats: Mpeg1/2, Mpeg4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP6/8, AVS jizun, Jpeg/Mjpeg, etc.

- Video Encoding

  – H.264 HP up to 1080p@30fps

  – Jpeg baseline: picture size up to 4080x4080

  – Alpha blending

  – Thumb generation

  – 4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

Display Engine

- Four moveable and size-adjustable layers, each layer size up to 8192x8192 pixels
- Ultra-Scaling engine
  - 8-tap scale filter in horizontal and 4 tap in vertical
  - Source image size from 8x4 to 8192x8192 resolution and destination image size from 8x4 to 8192x8192 resolution
- Support multiple image input formats
  - mono 1/2/4/8 bpp
  - palette 1/2/4/8 bpp
  - 6/24/32 bpp color
  - YUV444/420/422/411
- Support alpha blending/color key/gamma/harware cursor/sprite
- Output color correction: luminance/hue/saturation, etc
- Support de-interlace
- Video enhancement: lum peaking/DCTi/black and white level extension
- 3D input/output format conversion and display

Video Output

- HDMI 1.4 transmitter with HDCP
- LVDS/Sync RGB/CPU LCD interface up to 1920x1200 resolution
- Support 4-channel CVBS, or 2-channel S-video, or 1-channel YPbPr/VGA (YPbPr/VGA up to 1080p)
- Support two-channel independent display

Video Input

- Support TV decoder: 4-ch analog CVBS or 1-ch YPbPr(480i/576i/480p/576p) signal input
- Dual CMOS sensor parallel interfaces that support YUV format only
  - CSI0 up to 1080p@30fps
  - CSI1 up to 720p@30fps
- Support BT656 interface
- Support 24-bit YUV444/RGB interface

Analog Audio Output

- Stereo audio DAC
- Stereo capless headphone drivers
  - Up to 100dB SNR during DAC playback
  - Support 8KHz~192KHz DAC sample rate
- One low-noise analog microphone bias
- Dedicated headphone outputs

- Two mixers to meet different requirements
  - Output mixer for LINEINL/R, FMINL/R, MIC1/2 and Stereo DAC output
  - ADC record mixer for LINEINL/R, FMINL/R, MIC1/2 and Stereo DAC output

Analog Audio Input

- Support four analog audio inputs
  - Two microphone inputs
  - Differential or stereo line-in input
  - Stereo FM-in input
- Stereo audio ADC
  - 96dBA SNR
  - Support 8KHz ~ 48KHz ADC sample rate

RTP

- 12-bit SAR ADC
- Dual touch detection
- Sampling frequency up to 2MHz

Connectivity

USB2.0 OTG

- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Support up to 5 user-configurable endpoints for Bulk , Isochronous, Control and Interrupt

USB EHCI/OHCI

- Two EHCI/OHCI-compliant hosts

EMAC

- Support 10/100Mbps MII data transfer rate

GMAC

- Comply with the IEEE 802.3-2002 standard
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
- Support 10/100/1000Mbps data transfer rates RGMII interface to communicate with an external Gigabit PHY
- Support 10/100Mbps MII PHY interface

Digital Audio In/Out

- One I2S compliant audio interface, supporting 8-channel and 2-channel input

- One PCM, supporting linear sample(8-bit or 16-bit), 8-bit u-law and A-law companded sample
- One AC97 audio codec, supporting 2-channel and 6-channel audio data output

Transport Stream Controller

- Support both SPI and SSI
- Speed up to 150Mbps for both SPI and SSI
- Support 32-channel PID filter
- Support hardware PCR packet detect

Open-Drain TWI

- Up to 5 TWIs compliant with TWI protocol

Smart Card Reader

- One smart card reader controller supporting ISO/IEC 7816-3 and EMV2000 specifications
- Support synchronous and any other non-ISO 7816 and non-EMV cards

SPI

- Master/Slave configurable
- Up to 4 independent SPI controllers: SPI0 with one CS signal for system boot, SPI1/2/3 each with two CS signals

UART

- Up to 8 UART controllers:UART0 with two wires for debug tools, UART1 with 8 wires, UART2/3 each with 4 wires, and others each with 2 wires

PS2

- Two PS2 compliant to IBM PS2 and AT-compatible keyboard and mouse interface
- Dual-role controller: a PS2 host or a PS2 device

IR

- Two IR controllers supporting CIR, MIR and FIR modes

SATA

- One SATA Host controller
- Support SATA 1.5Gb/s and SATA 3.0Gb/s
- Comply with SATA spec 2.6
- Support external SATA(eSATA)

CAN

- One CAN bus controller
- Support the CAN2.0 A/B protocol specification
- Programmable data rate up to 1Mbps

Keypad

- One keypad matrix interface up to 8 rows and 8 colums
- Interrupt for key press or key release
- Internal debouncing filter to prevent switching noises

LRADC

- 6-bit resolution
- Voltage input range between 0V to 2V

PWM

- 2 PWM outputs
- Support cycle mode and pulse mode
- The pre-scale is from 1 to 64

Security System

- Security System
  - Support AES, DES, 3DES, SHA-1, MD5
  - Support ECB/CBC/CNT modes for AES/DES/3DES
  - 128-bit, 192-bit and 256-bit key size for AES
  - 160-bit hardware PRNG with 192-bit seed
- Security JTAG

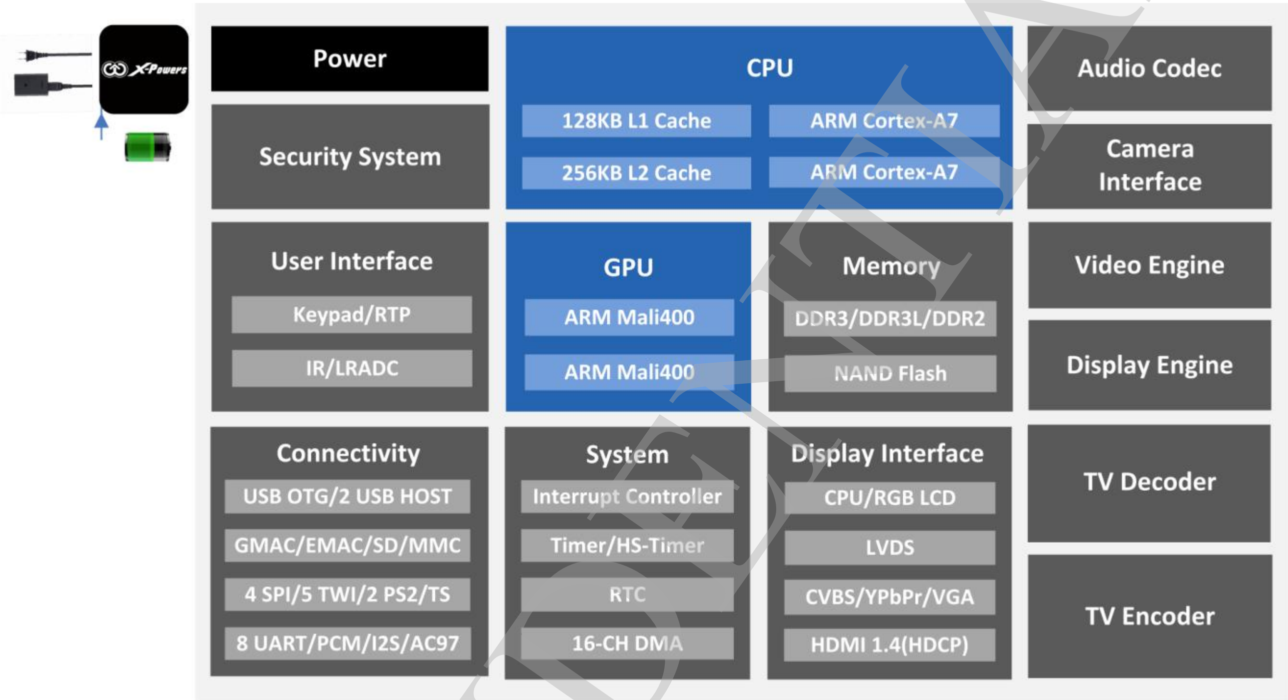
Power Management

- Flexible PLL clock generator and OSC for 32KHz
- Flexible clock gate
- Support DVFS for CPU frequency and voltage adjustment
- Support standby mode (only DDR+RTC-Domain power exist)

Package

- FBGA 441 balls,0.80mm ball pitch, 19x19x1.4mm

1.2. A20 Block Diagram



1.3. Memory Mapping

Module	Address	Size(Bytes)
SRAM A1	0x0000 0000---0x0000 3FFF	16K
SRAM A2	0x0000 4000---0x0000 7FFF	16K
SRAM A3	0x0000 8000---0x0000 B3FF	13K
SRAM A4	0x0000 B400---0x0000 BFFF	3K
SRAM NAND		2K
SRAM D	0x0001 0000---0x0001 0FFF	4K
SRAM B(Secure)	0x0002 0000---0x0002 FFFF	64K
SRAM Controller	0x01C0 0000---0x01C0 0FFF	4K
DRAM Controller	0x01C0 1000---0x01C0 1FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
NAND Flash	0x01C0 3000---0x01C0 3FFF	4K
Transport Stream	0x01C0 4000---0x01C0 4FFF	4K
SPI 0	0x01C0 5000---0x01C0 5FFF	4K
SPI 1	0x01C0 6000---0x01C0 6FFF	4K
Memory Stick	0x01C0 7000---0x01C0 7FFF	4K
TVD	0x01C0 8000---0x01C0 8FFF	4K
CSI 0	0x01C0 9000---0x01C0 9FFF	4K
TVE 0	0x01C0 A000---0x01C0 AFFF	4K
EMAC	0x01C0 B000---0x01C0 BFFF	4K
LCD 0	0x01C0 C000---0x01C0 CFFF	4K
LCD 1	0x01C0 D000---0x01C0 DFFF	4K
Video Engine	0x01C0 E000---0x01C0 EFFF	4K
SD/MMC 0	0x01C0 F000---0x01C0 FFFF	4K
SD/MMC 1	0x01C1 0000---0x01C1 0FFF	4K
SD/MMC 2	0x01C1 1000---0x01C1 1FFF	4K
SD/MMC 3	0x01C1 2000---0x01C1 2FFF	4K

Module	Address	Size(Bytes)
USB 0	0x01C1 3000---0x01C1 3FFF	4K
USB 1	0x01C1 4000---0x01C1 4FFF	4K
Security System	0x01C1 5000---0x01C1 5FFF	4K
HDMI	0x01C1 6000---0x01C1 6FFF	4K
SPI 2	0x01C1 7000---0x01C1 7FFF	4K
SATA	0x01C1 8000---0x01C1 8FFF	4K
PATA	0x01C1 9000---0x01C1 9FFF	4K
ACE	0x01C1 A000---0x01C1 AFFF	4K
TVE 1	0x01C1 B000---0x01C1 BFFF	4K
USB 2	0x01C1 C000---0x01C1 CFFF	4K
CSI 1	0x01C1 D000---0x01C1 DFFF	4K
	0x01C1 E000---0x01C1 EFFF	4K
SPI3	0x01C1 F000---0x01C1 FFFF	4K
CCU	0x01C2 0000---0x01C2 03FF	1K
Interrupt	0x01C2 0400---0x01C2 07FF	1K
PIO	0x01C2 0800---0x01C2 0BFF	1K
Timer	0x01C2 0C00---0x01C2 0FFF	1K
SPDIF	0x01C2 1000---0x01C2 13FF	1K
AC97	0x01C2 1400---0x01C2 17FF	1K
IR0	0x01C2 1800---0x01C2 1BFF	1K
IR 1	0x01C2 1C00---0x01C2 1FFF	1K
IIS-1	0x01C2 2000---0x01C2 23FF	1K
IIS-0	0x01C2 2400---0x01C2 27FF	1K
LRADC 0/1	0x01C2 2800---0x01C2 2BFF	1K
AD/DA	0x01C2 2C00---0x01C2 2FFF	1K
Keypad	0x01C2 3000---0x01C2 33FF	1K
	0x01C2 3400---0x01C2 37FF	1K
SID	0x01C2 3800---0x01C2 3BFF	1K
SJTAG	0x01C2 3C00---0x01C2 3FFF	1K
	0x01C2 4000---0x01C2 43FF	1K
IIS-2	0x01C2 4400---0x01C2 47FF	1K
	0x01C2 4800---0x01C2 4BFF	1K

Module	Address	Size(Bytes)
	0x01C2 4C00---0x01C2 4FFF	1K
TP	0x01C2 5000---0x01C2 53FF	1K
PMU	0x01C2 5400---0x01C2 57FF	1K
	0x01C2 5800---0x01C2 5BFF	1K
CPU Configuration	0x01C2 5C00---0x01C2 5FFF	1K
	0x01C2 6000---0x01C2 63FF	1K
	0x01C2 6400---0x01C2 67FF	1K
	0x01C2 6800---0x01C2 6BFF	1K
	0x01C2 6C00---0x01C2 6FFF	1K
	0x01C2 7000---0x01C2 73FF	1K
	0x01C2 7400---0x01C2 77FF	1K
	0x01C2 7800---0x01C2 7BFF	1K
	0x01C2 7C00---0x01C2 7FFF	1K
UART 0	0x01C2 8000---0x01C2 83FF	1K
UART 1	0x01C2 8400---0x01C2 87FF	1K
UART 2	0x01C2 8800---0x01C2 8BFF	1K
UART 3	0x01C2 8C00---0x01C2 8FFF	1K
UART 4	0x01C2 9000---0x01C2 93FF	1K
UART 5	0x01C2 9400---0x01C2 97FF	1K
UART 6	0x01C2 9800---0x01C2 9BFF	1K
UART 7	0x01C2 9C00---0x01C2 9FFF	1K
PS2-0	0x01C2 A000---0x01C2 A3FF	1K
PS2-1	0x01C2 A400---0x01C2 A7FF	1K
/	0x01C2 A800---0x01C2 ABFF	1K
TWI 0	0x01C2 AC00---0x01C2 AFFF	1K
TWI 1	0x01C2 B000---0x01C2 B3FF	1K
TWI 2	0x01C2 B400---0x01C2 B7FF	1K
TWI 3	0x01C2 B800---0x01C2 BBFF	1K
CAN	0x01C2 BC00---0x01C2 BFFF	1K
TWI 4	0x01C2 C000---0x01C2 C3FF	1K
Smart Card Reader	0x01C2 C400---0x01C2 C7FF	1K
GPS	0x01C3 0000---0x01C3 FFFF	64K

Module	Address	Size(Bytes)
Mali400	0x01C4 0000---0x01C4 FFFF	64K
GMAC	0x01C5 0000---0x01C5 FFFF	64K
HSTIMER	0x01C6 0000---0x01C6 0FFF	4K
GIC Registers	0x01C8 0000---0x01C8 7FFF	32K
HDMI1	0x01CE 0000---0x01CF FFFF	128K
CPUBIST	0x3F50 1000---0x3F50 1FFF	4K
SRAM C	0x01D0 0000---0x01DF FFFF	Module SRAM
DE_FE0	0x01E0 0000---0x01E1 FFFF	128K
DE_FE1	0x01E2 0000---0x01E3 FFFF	128K
DE_BE0	0x01E6 0000---0x01E7 FFFF	128K
DE_BE1	0x01E4 0000---0x01E5 FFFF	128K
MP	0x01E8 0000---0x01E9 FFFF	128K
AVG	0x01EA 0000---0x01EB FFFF	128K
CoreSight Debug Module	0x3F50 0000---0x3F50 FFFF	64K
DDR-II/DDR-III	0x4000 0000---0xBFFF FFFF	2G
BROM	0xFFFF 0000—0xFFFF 7FFF	32K

1.4. CPU Configuration

1.4.1. Overview

The CPU configuration module features:

- Software reset control for each individual CPU
- CPU configuration for each individual CPU
- Three 64-bit idle counters and two 64-bit common counters

1.4.2. CPU Configuration Register List

Module Name	Base Address
CPU Configuration	0x01C25C00

Register Name	Offset	Description
CPU0_RST_CTRL	0x0040	CPU0 Reset Control
CPU0_CTRL_REG	0x0044	CPU0 Control Register
CPU0_STATUS_REG	0x0048	CPU0 Status Register
CPU1_RST_CTRL	0x0080	CPU1 Reset Control
CPU1_CTRL_REG	0x0084	CPU1 Control Register
CPU1_STATUS_REG	0x0088	CPU1 Status Register
GENER_CTRL_REG	0x0184	General Control Register
EVENT_IN	0x0190	Event Input Register
PRIVATE_REG	0x01A4	Private Register
IDLE_CNT0_LOW_REG	0x0200	Idle Counter 0 Low Register
IDLE_CNT0_HIGH_REG	0x0204	Idle Counter 0 High Register
IDLE_CNT0_CTRL_REG	0x0208	Idle Counter 0 Control Register
IDLE_CNT1_LOW_REG	0x0210	Idle Counter 1 Low Register
IDLE_CNT1_HIGH_REG	0x0214	Idle Counter 1 High Register
IDLE_CNT1_CTRL_REG	0x0218	Idle Counter 1 Control Register
OSC24M_CNT64_CTRL_REG	0x0280	64-bit Counter Control Register
OSC24M_CNT64_LOW_REG	0x0284	64-bit Counter Low Register
OSC24M_CNT64_HIGH_REG	0x0288	64-bit Counter High Register
LOSC_CNT64_CTRL_REG	0x0290	64-bit Counter Control Register
LOSC_CNT64_LOW_REG	0x0294	64-bit Counter Low Register
LOSC_CNT64_HIGH_REG	0x0298	64-bit Counter High Register

1.4.3. CPUCFG Register Description

1.4.3.1. CPU0 RESET CONTROL(DEFAULT: 0X00000003)

Offset: 0x40			Register Name: CPU0_RST_CTRL
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x1	CPU0_CORE_REST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x1	CPU0_RESET. CPU0 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

1.4.3.2. CPU0 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x44			Register Name: CPU0_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU0_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

1.4.3.3. CPU0 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x48			Register Name: CPU0_ STATUS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

1.4.3.4. CPU1 RESET CONTROL(DEFAULT: 0X00000000)

Offset: 0x80			Register Name: CPU1_RST_CTRL
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x0	CPU1_CORE_REST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x0	CPU1_RESET. CPU1 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

1.4.3.5. CPU1 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x84			Register Name: CPU1_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU1_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

1.4.3.6. CPU1 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x88			Register Name: CPU1_ STATUS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

1.4.3.7. GENERAL CONTROL REGISTER(DEFAULT :0X00000020)

Offset: 0x184			Register Name: GENER_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:9	/	/	/.
8	R/W	0x0	CFGSDISABLE.

Offset: 0x184			Register Name: GENER_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			Disables write access to some secure GIC registers.
7:6	/	/	/
5	R/W	0x1	L2_RST. L2 Reset.(SCU global reset) 0: Apply reset to shared L2 memory system controller. 1: Do not apply reset to shared L2 memory system controller.
4	R/W	0x0	L2_RST_DISABLE. Disable automatic L2 cache invalidate at reset: 0: L2 cache is reset by hardware. 1: L2 cache is not reset by haredware.
3:2	/	/	/
1:0	R/W	0x0	L1_RST_DISABLE. L1 Reset Disable[1:0]. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

1.4.3.8. EVENT INPUT REGISTER(DEFAULT : 0X00000000)

Offset: 0x190			Register Name: EVENT_IN
Bit	Read/ Write	Default/Hex	Description
31:1	/	/	/.
0	R/W	0x0	EVENT_IN. Event input that can wake-up CPU0/1 from WFE standby mode.

1.4.3.9. PRIVATE REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A4			Register Name: PRIVATE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	

1.4.3.10. IDLE COUNTER 0 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x200			Register Name: IDLE_CNT0_LOW_REG.
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT0_LO. Idle Counter 0 [31:0]. This counter clock source is 24MHz. If the CPU is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 0 high register.

1.4.3.11. IDLE COUNTER 0 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x204			Register Name: IDLE_CNT0_HIGH_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT0_HI. Idle Counter 0 [63:32]. Any write to this register will clear this register and the idle counter 0 low register.

1.4.3.12. IDLE COUNTER 0 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x208			Register Name: IDLE_CNT0_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable. 0: disable 1: enable. Note: Idle Counter 0 is used for CPU0
1	R/W	0x0	IDLE_RL_EN. Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN.

Offset: 0x208			Register Name: IDLE_CNT0_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

1.4.3.13. IDLE COUNTER 1 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x210			Register Name: IDLE_CNT1_LOW_REG.
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	IDLE_CNT1_LO. Idle Counter 1 [31:0]. This counter clock source is 24MHz. If the CPU is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 1 high register.

1.4.3.14. IDLE COUNTER 1 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x214			Register Name: IDLE_CNT1_HIGH_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	IDLE_CNT1_HI. Idle Counter 1[63:32]. Any write to this register will clear this register and the idle counter 1 low register.

1.4.3.15. IDLE COUNTER 1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x218			Register Name: IDLE_CNT1_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable.

Offset: 0x218			Register Name: IDLE_CNT1_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			0: disable 1: enable. Note: Idle Counter 1 is used for CPU1
1	R/W	0x0	IDLE_RL_EN. Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN. Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

1.4.3.16. OSC24M 64-BIT COUNTER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x280			Register Name: OSC24M_CNT64_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:5	/	/	/.
4	R/W	0x0	CNT64_SYNCH Wite 1 then write 0 (a high pulse) to force the 64-bit system counter synchronize the OSC24M 64-bit counter.
3	/	/	/
2	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: /
1	R/W	0x0	CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: no effect, 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	CNT64_CLR_EN. 64-bit Counter Clear Enable. 0: no effect, 1: to clear the 64-bit Counter Low/Hi registers and

Offset: 0x280			Register Name: OSC24M_CNT64_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			it will change to zero after the registers are cleared.

Note: This 64-bit counter will start to count as soon as the System Power On finishes.

1.4.3.17. OSC24M 64-BIT COUNTER LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x284			Register Name: OSC24M_CNT64_LOW_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CNT64_LO. 64-bit Counter [31:0].

1.4.3.18. OSC24M 64-BIT COUNTER HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x288			Register Name: OSC24M_CNT64_HIGH_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CNT64_HI. 64-bit Counter [63:32].

1.4.3.19. LOSC 64-BIT COUNTER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x290			Register Name: LOSC_CNT64_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: LOSC 1: /
1	R/W	0x0	CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: no effect, 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero after the registers are

Offset: 0x290			Register Name: LOSC_CNT64_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			latched.
0	R/W	0x0	CNT64_CLR_EN. 64-bit Counter Clear Enable. 0: no effect, 1: to clear the 64-bit Counter Low/Hi registers and it will change to zero after the registers are cleared.

Note: This 64-bit counter will start to count as soon as the System Power On finished.

1.4.3.20. LOSC 64-BIT COUNTER LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x294			Register Name: LOSC_CNT64_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNT64_LO. 64-bit Counter [31:0].

1.4.3.21. LOSC 64-BIT COUNTER HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x298			Register Name: LOSC_CNT64_HIGH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNT64_HI. 64-bit Counter [63:32].

1.5. CCU

1.5.1. Overview

The CCU (Clock Control Unit) is made up of 7 PLLs, a main oscillator, an on-chip RC oscillator and a 32768Hz low-power oscillator.

A20 integrates two crystal oscillators: The 24MHz crystal is mandatory, which is used to provide clock source for the PLL and the main digital blocks, and the 32768Hz oscillator, which is only used to provide a low power, accurate reference for the RTC.

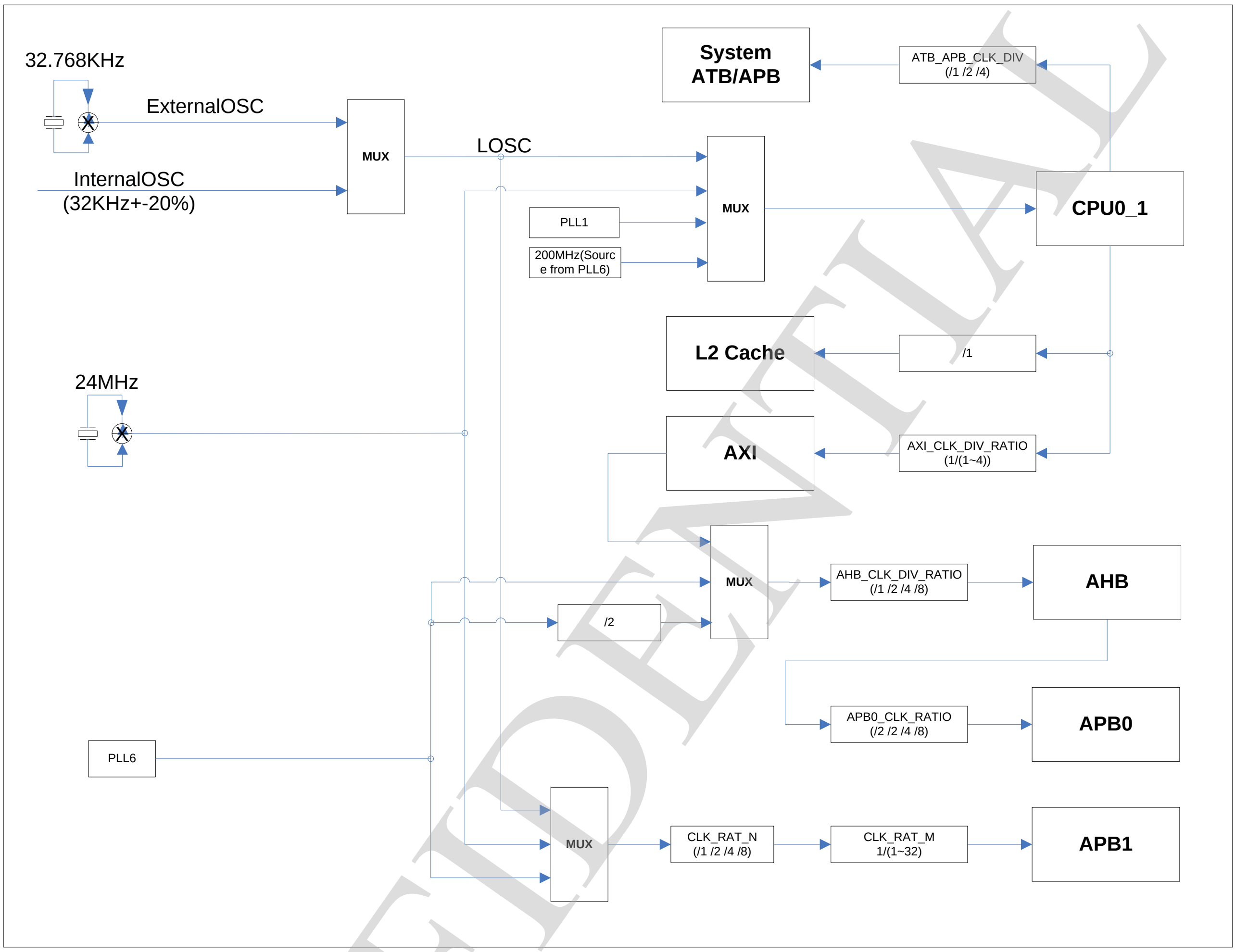
A20 also provides following clock domain to allow for user interfaces of high performance and low power consumption.

Clock Domain	**Module**	**Speed Range**	**Description**
OSC24M	Most Clock Generator	24MHz	Root clock for most blocks
RC_osc	Timer,Key	32KHz	Source for the RTC/Timer
32K768Hz	Timer,Key	32768Hz	Low-power source for the RTC/Timer
CPU32_clk	CPU32	2K~1200M	Divided from CPU32_clk or OSC24M
AHB_clk	AHB Devices	8K~276M	Divided from CPU32_clk
APB_clk	Peripheral	0.5K~138M	Divided from AHB_clk
SDRAM_clk	SDRAM	0~400MHz	Sourced from the PLL
USB_clk	USB	480MHz	Sourced from the PLL
Audio_clk	A/D,D/A	24.576MHz /22.5792MHz	Sourced from the PLL

The CCU features:

- 8 PLLs, a main oscillator, an on-chip RC oscillator and a 32768Hz low-power oscillator
- PLL1 is the main clock of CPU0/1
- Clock configuration for corresponding module
- Software-controlled clock gating
- 2 clock output channels

1.5.2. Clock Tree Diagram



1.5.3. CCU Register List

Module Name	Base Address
CCU	0x01C20000

Register Name	Offset	Description
PLL1_CFG_REG	0x0000	PLL1 CONTROL
PLL1_TUN_REG	0x0004	PLL1 TUNING
PLL2_CFG_REG	0x0008	PLL2 CONTROL
PLL2_TUN_REG	0x000C	PLL2 TUNING

Register Name	Offset	Description
PLL3_CFG_REG	0x0010	PLL3 CONTROL
PLL4_CFG_REG	0x0018	PLL4 CONTROL
PLL5_CFG_REG	0x0020	PLL5 CONTROL
PLL5_TUN_REG	0x0024	PLL5 TUNING
PLL6_CFG_REG	0x0028	PLL6 CONTROL
PLL6_TUN_REG	0x002C	PLL6 TUNING
PLL7_CFG_REG	0x0030	PLL7 CONTROL
/	0x0034	/
PLL1_TUN2_REG	0x0038	PLL1 TUNING2
PLL5_TUN2_REG	0x003C	PLL5 TUNING2
PLL8_CFG_REG	0x0040	PLL8 CONTROL
OSC24M_CFG_REG	0x0050	OSC24M CONTROL
CPU_AHB_APB0_CFG_REG	0x0054	CPU, AHB AND APB0 DIVIDE RATIO
APB1_CLK_DIV_REG	0x0058	APB1 CLOCK DIVIDOR
AHB_GATING_REG0	0x0060	AHB MODULE CLOCK GATING 0
AHB_GATING_REG1	0x0064	AHB MODULE CLOCK GATING 1
APB0_GATING_REG	0x0068	APB0 MODULE CLOCK GATING
APB1_GATING_REG	0x006C	APB1 MODULE CLOCK GATING
NAND_SCLK_CFG_REG	0x0080	NAND CLOCK CONFIGURATION REGISTER
MS_SCLK_CFG_REG	0x0084	MEMORY STICK CLOCK CONFIGURATION REGISTER
SD0_CLK_REG	0x0088	SD0 CLOCK REGISTER
SD1_CLK_REG	0x008C	SD1 CLOCK REGISTER
SD2_CLK_REG	0x0090	SD2 CLOCK REGISTER
SD3_CLK_REG	0x0094	SD3 CLOCK REGISTER
TS_CLK_REG	0x0098	TRANSPORT STREAM CLOCK REGISTER
SS_CLK_REG	0x009C	SECURITY SYSTEM CLOCK REGISTER
SPI0_CLK_REG	0x00A0	SPI0 CLOCK REGISTER
SPI1_CLK_REG	0x00A4	SPI1 CLOCK REGISTER
SPI2_CLK_REG	0x00A8	SPI2 CLOCK REGISTER
IR0_CLK_REG	0x00B0	IR0 CLOCK REGISTER

Register Name	Offset	Description
IR1_CLK_REG	0x00B4	IR1 CLOCK REGISTER
IIS0_CLK_REG	0x00B8	IIS0 CLOCK REGISTER
AC97_CLK_REG	0x00BC	AC97 CLOCK REGISTER
SPDIF_CLK_REG	0x00C0	SPDIF CLOCK REGISTER
KEYPAD_CLK_REG	0x00C4	KEYPAD CLOCK REGISTER
SATA_CLK_REG	0x00C8	SATA CLOCK REGISTER
USB_CLK_REG	0x00CC	USB CLOCK REGISTER
SPI3_CLK_REG	0x00D4	SPI 3 CLOCK REGISTER
IIS1_CLK_REG	0x00D8	IIS 1 CLOCK REGISTER
IIS2_CLK_REG	0x00DC	IIS 2 CLOCK REGISTER
DRAM_CLK_REG	0x0100	DRAM CLOCK REGISTER
BE0_SCLK_CFG_REG	0x0104	DISPLAY ENGINE BACKEND CLOCK CONFIGURATION REGISTER
BE1_SCLK_CFG_REG	0x0108	DISPLAY ENGINE BACKEND 0 CLOCK CONFIGURATION REGISTER
FE0_CLK_REG	0x010C	DISPLAY ENGINE FRONTEND CLOCK CONFIGURATION REGISTER
FE1_CLK_REG	0x0110	DISPLAY ENGINE FRONTEND1 CLOCK CONFIGURATION REGISTER
MP_CLK_REG	0x0114	MIXER PROCESSOR CLOCK REGISTER
LCD0_CH0_CLK_REG	0x0118	LCD0 CHANNAL 0 CLOCK REGISTER
LCD1_CH0_CLK_REG	0x011C	LCD1 CHANNEL0 CLOCK REGISTER
CSI_SCLK_REG	0x0120	CSI SPECIAL CLOCK REGISTER
TVD_CLK_REG	0x0128	TVD CLOCK REGISTER
LCD0_CH1_CLK_REG	0x012C	LCD0 CHANNEL 1 CLOCK REGISTER
LCD1_CH1_CLK_REG	0x0130	LCD1 CHANNEL 1 CLOCK REGISTER
CSI0_CLK_REG	0x0134	CSI0 CLOCK REGISTER
CSI1_CLK_REG	0x0138	CSI1 CLOCK REGISTER
VE_CLK_REG	0x013C	VIDEO ENGINE CLOCK REGISTER
AUDIO_CODEC_CLK_REG	0x0140	AUDIO CODEC CLOCK REGISTER
AVS_CLK_REG	0x0144	AVS CLOCK REGISTER
ACE_CLK_REG	0x0148	ACE CLOCK REGISTER
LVDS_CLK_REG	0x014C	LVDS CLOCK REGISTER

Register Name	Offset	Description
HDMI_CLK_REG.	0x0150	HDMI CLOCK REGISTER
MALI400_CLK_REG	0x0154	MALI 400 CLOCK REGISTER
MBUS_SCLK_CFG_REG	0x015C	MBUS CLOCK CONFIGURATION REGISTER
GMAC_CLK_REG	0x0164	GMAC CLOCK REGISTER
HDMI1_RST_REG	0x0170	HDMI1 RESET REGISTER
HDMI1_CTRL_REG	0x0174	HDMI1 CONTROL REGISTER
HDMI1_SLOW_CLK_REG	0x0178	HDMI1 SLOW CLOCK REGISTER
HDMI1_REPEAT_CLK_REG	0x017C	HDMI1 REPEAT CLOCK REGISTER
CLK_OUTA_REG	0x01F0	CLK OUTA
CLK_OUTB_REG	0x01F4	CLK OUTB

1.5.4. CCU Register Description

1.5.4.1. PLL1-CORE(DEFAULT: 0X21005000)

Offset: 0x00			Register Name: PLL1_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL1_Enable. 0: Disable, 1: Enable. The PLL1 output=(24MHz*N*K)/(M*P). The PLL1 output is for the CORECLK. Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled. Its default is 384MHz.
30	/	/	/
29:26	/-	/	/
25	R/W	0x0	EXG_MODE. Exchange mode.
24:20	/	/	/

Offset: 0x00			Register Name: PLL1_CFG_REG
Bit	Read/ Write	Default/Hex	Description
19:18	/	/	/
17:16	R/W	0x0	PLL1_OUT_EXT_DIVP. PLL1 Output external divider P. The range is 1/2/4/8.
15:13	/	/	/
12:8	R/W	0x10	PLL1_FACTOR_N PLL1 Factor N.. Factor=0, N=1; Factor=1, N=1; Factor=2, N=2 …… Factor=31,N=31
7:6	/	/	/
5:4	R/W	0x0	PLL1_FACTOR_K. PLL1 Factor K.(K=Factor + 1) The range is from 1 to 4.
3	R/W	0x0	SIG_DELT_PAT_IN. Sigma-delta pattern input.
2	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
1:0	R/W	0x0	PLL1_FACTOR_M. PLL1 Factor M. (M=Factor + 1) The range is from 1 to 4.

1.5.4.2. PLL1-TUNING(DEFAULT: 0X0A101000)

Offset: 0x04			Register Name: PLL1_TUN_REG
Bit	Read/ Write	Default/Hex	Description
31:0	/	/	/

1.5.4.3. PLL2-AUDIO(DEFAULT: 0X08100010)

Offset: 0x08			Register Name: PLL2_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL2_Enable. 0: Disable, 1: Enable. The PLL2 is for Audio. PLL2 Output = 24MHz*N/PLL2_PRE_DIV/PLL2_POST_DIV. 1X = 48*N/PreDiv/PostDiv/2(not 50% duty) 2X = 48*N/PreDiv/4(8X/4 50% duty) 4X = 48*N/PreDiv/2(8X/2 50% duty) 8X = 48*N/PreDiv(not 50% duty)
30	/	/	/
29:26	R/W	0x2	PLL2_POST_DIV. PLL2 post-dividor[3:0]. 0000: 0x1 0001: 0x1 0010: 0x2 …… 1111: 0xf
25:21	/	/	/
20:16	/	/	/
15	/	/	/
14:8	R/W	0x0	PLL2_Factor_N. PLL2 Factor N. Factor=0, N=1; Factor=1, N=1; …… Factor=0x7F, N=0x7F;
7:5	/	/	/
4:0	R/W	0x10	PLL2_PRE_DIV. PLL2 pre-dividor[4:0]. PLL2_PRE_DIV=divider 00000: 0x1 00001: 0x1 ……

Offset: 0x08			Register Name: PLL2_CFG_REG
Bit	Read/ Write	Default/Hex	Description
			11111: 0x1F

1.5.4.4. PLL2-TUNING(DEFAULT: 0X00000000)

Offset: 0x0C			Register Name: PLL2_TUN_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

1.5.4.5. PLL3-VIDEO 0(DEFAULT: 0X0010D063)

Offset: 0x10			Register Name: PLL3_CFG_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	PLL3_Enable.

Offset: 0x10			Register Name: PLL3_CFG_REG
Bit	Read/ Write	Default/Hex	Description
			0: Disable, 1: Enable. In the integer mode, The PLL3 output=3MHz*M. In the fractional mode, the PLL3 output is selected by bit 14. The PLL3 output range is 27MHz~381MHz.
30:27	/	/	/
26:24	/	/	/
23:21	/	/	/
20:16	/	/	/
15	R/W	0x1	PLL3_MODE_SEL. PLL3 mode select. 0: fractional mode, 1: integer mode.
14	R/W	0x1	PLL3_FUNC_SET. PLL3 fractional setting. 0: 270MHz, 1: 297MHz.
13	/	/	/
12:8	/	/	/
7	/	/	/
6:0	R/W	0x63	PLL3_FACTOR_M. PLL3 Factor M. The range is from 9 to 127.

1.5.4.6. PLL4-VE(DEFAULT: 0X21009911)

Offset: 0x18			Register Name: PLL4_CFG_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	PLL4_Enable. 0: Disable, 1: Enable. The output = 24MHz*N*K Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled.
30	R/W	0x0	PLL4_BYPASS_EN. PLL4 Output Bypass Enable.

Offset: 0x18			Register Name: PLL4_CFG_REG
Bit	Read/ Write	Default/Hex	Description
			0: Disable, 1: Enable. If the bypass is enabled, the PLL4 output is 24MHz.
29:25	/	/	/
24:20	/	/	/
19:16	/	/	/
15	/	/	/ 0: narrow, 1: wide.
14:13	/	/	/
12:8	R/W	0x19	PLL4_FACTOR_N. PLL4 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2; …… Factor=31,N=31
7:6	/	/	/
5:4	R/W	0x1	PLL4_FACTOR_K. PLL4 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	/

1.5.4.7. PLL5-DDR(DEFAULT: 0X11049280)

Offset: 0x20			Register Name: PLL5_CFG_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	PLL5_Enable. 0: Disable, 1: Enable. The PLL5 output for DDR = (24MHz*N*K)/M. The PLL5 output for other module =(24MHz*N*K)/P.

Offset: 0x20			Register Name: PLL5_CFG_REG
Bit	Read/ Write	Default/Hex	Description
			The PLL5 output is for the DDR. Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled.
30	/	/	/
29	R/W	0x0	DDR_CLK_OUT_EN. DDR clock output en.
28:25	/	/	/
24:20	/	/	/
19	/	/	/
18	/	/	/
17:16	R/W	0x0	PLL5_OUT_EXT_DIV_P. PLL5 Output External Divider P. The range is 1/2/4//8.
15:13	/	/	/
12:8	R/W	0x12	PLL5_FACTOR_N. PLL5 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2 …… Factor=31,N=31
7	R/W	0x1	LDO_EN. LDO Enable.
6	R/W	/	/
5:4	R/W	0x0	PLL5_FACTOR_K. PLL5 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	R/W	0x0	PLL5_FACTOR_M1. PLL5 Factor M1.
1:0	R/W	0x0	PLL5_FACTOR_M. PLL5 Factor M.(M = Factor + 1) The range is from 1 to 4.

1.5.4.8. PLL5-TUNING(DEFAULT: 0X14888000)

Offset: 0x24			Register Name: PLL5_TUN_REG
Bit	Read/ Write	Default/Hex	Description
31:29	/	/	/
28	/	/	/
27	/	/	/
26:24	/	/	/
23	/	/	/
22:16	/	/	/
15	/	/	/.
14:8	/	/	/
7	/	/	/
6:0	/	/	/

1.5.4.9. PLL6-SATA(DEFAULT: 0X21009911)

Offset: 0x28			Register Name: PLL6_CFG_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	PLL6_Enable. 0: Disable, 1: Enable. There are two ouputs: For SATA, the output =(24MHz*N*K)/M/6 If the SATA is on, the clock output should be equal to 100MHz; For other module, the clock output = (24MHz*N*K)/2 PLL6*2 = 24MHz*N*K Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled.
30	R/W	0x0	PLL6_BYPASS_EN. PLL6 Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL6 output is 24MHz.

29:25	/	/	/
24:20	/	/	/
19:16	/	/	/
15	/	/	/
14	R/W	0x0	SATA_CLK_EN. Sata clock output enable. 0:Disable;1:enable.
13	/	/	/
12:8	R/W	0x19	PLL6_FACTOR_N. PLL6 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2; …… Factor=31,N=31
7:6	/	/	/
5:4	R/W	0x1	PLL6_FACTOR_K. PLL6 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL6_FACTOR_M. PLL6 Factor M.(M = Factor + 1) The range is from 1 to 4.

1.5.4.10. PLL6-TUNING

Offset: 0x2C			**Register Name: PLL6_TUN_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	/	/	/

1.5.4.11. PLL7-VIDEO 1(DEFAULT: 0X0010D063)

Offset: 0x30			Register Name: PLL7_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL7_Enable. 0: Disable, 1: Enable. In the integer mode, The PLL7 output=3MHz*M. In the fractional mode, the PLL7 output is select by bit 14. The PLL7 output range is 27MHz~381MHz.
30:16	/	/	/.
15	R/W	0x1	PLL7_MODE_SEL. PLL7 mode select. 0: fractional mode, 1: integer mode.
14	R/W	0x1	PLL7_FRAC_SET. PLL7 fractional setting. 0: 270MHz, 1: 297MHz.
13:7	/	/	/.
6:0	R/W	0x63	PLL7_FACTOR_M. PLL7 Factor M. The range is from 9 to 127.

1.5.4.12. PLL1-TUNING2(DEFAULT: 0X00000000)

Offset: 0x38			Register Name: PLL1_TUN2_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.

Offset: 0x38			Register Name: PLL1_TUN2_REG
Bit	Read/ Write	Default/Hex	Description
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

1.5.4.13. PLL5-TUNING2(DEFAULT: 0X00000000)

Offset: 0x3C			Register Name: PLL5_TUN2_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT.

			Wave Bottom.

1.5.4.14. PLL8-GPU(DEFAULT: 0X21009911)

Offset: 0x40			**Register Name: PLL8_CFG_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL8_Enable. 0: Disable, 1: Enable. The output = 24MHz*N*K Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled.
30	R/W	0x0	PLL8_BYPASS_EN. PLL8 Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL8 output is 24MHz.
29:13	/	/	/
12:8	R/W	0x19	PLL8_FACTOR_N. PLL8 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2; …… Factor=31,N=31
7:6	/	/	/
5:4	R/W	0x1	PLL8_FACTOR_K. PLL8 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	/

1.5.4.15. OSC24M (DEFAULT: 0X00138013)

Offset: 0x50	**Register Name: OSC24M_CFG_REG**

Bit	Read/ Write	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD. Key Field for LDO Enable bit. If the key field value is 0xA7, the bit[23:16] can be modified.
23:17	/	/	/
16	R/W	0x1	LDO_EN. LDO Enable. 0: Disable, 1: Enable.
15	R/W	0x1	PLL_BIAS_EN. PLL Bias Enable. 0: disable, 1: enable.
14:2	/	/	/
1	R/W	0x1	OSC24M_GSM. OSC24M GSM.
0	R/W	0x1	OSC24M_EN. OSC24M Enable. 0: Disable, 1: Enable.

1.5.4.16. CPU/AHB/APB0 CLOCK RATIO(DEFAULT: 0X00010010)

Offset: 0x54			Register Name: CPU_AHB_APB0_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	DVFS_START. DVFS start. Set 1 to this bit will start the DVFS. It will be cleared automatically after the DVFS is finished.
30:18	/	/	/
17:16	R/W	0x1	CPU_CLK_SRC_SEL. CPU0/1 Clock Source Select. 00: LOSC 01: OSC24M 10: PLL1 11: 200MHz(source from the PLL6). If the clock source is changed, at most to wait for 8 present running clock cycles.

Offset: 0x54			Register Name: CPU_AHB_APB0_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
15:13	/	/	/
12:11	R/W	0x0	
10	/	/	/
9:8	R/W	0x0	APB0_CLK_RATIO. APB0 Clock divide ratio. APB0 clock source is AHB clock. 00: /2 01: /2 10: /4 11: /8
7:6	R/W	0x0	AHB_CLK_SRC_SEL. 00: AXI 01: PLL6/2 10: PLL6 11: /
5:4	R/W	0x1	AHB_CLK_DIV_RATIO. AHB Clock divide ratio. 00: /1 01: /2 10: /4 11: /8
3:2	/	/	ATB_APB_CLK_DIV. 00: /1 01: /2 1x: /4 Note: System ATB/APB clock source is CPU clock source.
1:0	R/W	0x0	AXI_CLK_DIV_RATIO. AXI Clock divide ratio. AXI Clock source is CPU clock. 00: /1 01: /2 10: /3 11: /4

1.5.4.17. APB1 CLOCK DIVIDE RATIO(DEFAULT: 0X00000000)

Offset: 0x58			Register Name: APB1_CLK_DIV_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	APB1_CLK_SRC_SEL. APB1 Clock Source Select 00: OSC24M 01: PLL6 10: LOSC 11: / This clock is used for some special module apbclk(twi,uart, ps2, can, scr). Because these modules need special clock rate even if the apbclk changed.
23:18	/	/	/
17:16	R/W	0x0	CLK_RAT_N Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:5	/	/	/
4:0	R/W	0x0	CLK_RAT_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

1.5.4.18. AHB MODULE CLOCK GATING REGISTER 0(DEFAULT: 0X00000000)

Offset: 0x60			Register Name: AHB_GATING_REG0
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	STIMER_AHB_GATING Gating AHB Clock for Sync timer(0:mask,1:pass)
27:26	/	/	/
25	R/W	0x0	Gating AHB Clock for SATA(0: mask, 1: pass).
24	/	/	/

Offset: 0x60			Register Name: AHB_GATING_REG0
Bit	**Read/ Write**	**Default/Hex**	**Description**
23	R/W	0x0	Gating AHB Clock for SPI3(0: mask, 1: pass).
22	R/W	0x0	Gating AHB Clock for SPI2(0: mask, 1: pass).
21	R/W	0x0	Gating AHB Clock for SPI1(0: mask, 1: pass).
20	R/W	0x0	Gating AHB Clock for SPI0(0: mask, 1: pass).
19	/	/	/
18	R/W	0x0	Gating AHB Clock for TS(0: mask, 1: pass).
17	R/W	0x0	Gating AHB Clock for EMAC(0: mask, 1: pass).
16	R/W	0x0	Gating AHB Clock for ACE(0: mask, 1: pass).
15	/	/	/
14	R/W	0x0	Gating AHB Clock for SDRAM(0: mask, 1: pass).
13	R/W	0x0	Gating AHB Clock for NAND(0: mask, 1: pass).
12	R/W	0x0	Gating AHB Clock for MS(0: mask, 1: pass).
11	R/W	0x0	Gating AHB Clock for SD/MMC3(0: mask, 1: pass).
10	R/W	0x0	Gating AHB Clock for SD/MMC2(0: mask, 1: pass).
9	R/W	0x0	Gating AHB Clock for SD/MMC1(0: mask, 1: pass).
8	R/W	0x0	Gating AHB Clock for SD/MMC0(0: mask, 1: pass).
7	R/W	0x0	Gating AHB Clock for BIST(0: mask, 1: pass).
6	R/W	0x0	Gating AHB Clock for DMA(0: mask, 1: pass).
5	R/W	0x0	Gating AHB Clock for SS(0: mask, 1: pass).
4	R/W	0x0	Gating AHB Clock for USB OHCI1(0: mask, 1: pass).
3	R/W	0x0	Gating AHB Clock for USB EHCI1 (0: mask, 1: pass).
2	R/W	0x0	Gating AHB Clock for USB OHCI0(0: mask, 1: pass).
1	R/W	0x0	Gating AHB Clock for USB EHCI0 (0: mask, 1: pass).
0	R/W	0x0	Gating AHB Clock for USB0(0: mask, 1: pass).

1.5.4.19. AHB MODULE CLOCK GATING REGISTER 1(DEFAULT: 0X00000000)

Offset: 0x64			Register Name: AHB_GATING_REG1
Bit	**Read/ Write**	**Default/Hex**	**Description**

Offset: 0x64			Register Name: AHB_GATING_REG1
Bit	Read/ Write	Default/Hex	Description
31:21	/	/	/.
20	R/W	0x0	Gating AHB Clock for Mali-400(0: mask, 1: pass).
19	/	/	/
18	R/W	0x0	Gating AHB Clock for MP(0: mask, 1: pass).
17	R/W	0x0	GMAC_AHB_GATING Gating AHB Clock for GMAC(0:mask,1:pass)
16	/	/	/
15	R/W	0x0	Gating AHB Clock for DE-FE1(0: mask, 1: pass).
14	R/W	0x0	Gating AHB Clock for DE-FE0(0: mask, 1: pass).
13	R/W	0x0	Gating AHB Clock for DE-BE1(0: mask, 1: pass).
12	R/W	0x0	Gating AHB Clock for DE-BE0(0: mask, 1: pass).
11	R/W	0x0	Gating AHB Clock for HDMI(0: mask, 1: pass).
10	R/W	0x0	Gating AHB Clock for HDMI1(0: mask, 1: pass).
9	R/W	0x0	Gating AHB Clock for CSI1(0: mask, 1: pass).
8	R/W	0x0	Gating AHB Clock for CSI0(0: mask, 1: pass).
7:6	/	/	
5	R/W	0x0	Gating AHB Clock for LCD1(0: mask, 1: pass).
4	R/W	0x0	Gating AHB Clock for LCD0(0: mask, 1: pass).
3	R/W	0x0	Gating AHB Clock for TVE 1(0: mask, 1: pass).
2	R/W	0x0	Gating AHB Clock for TVE 0(0: mask, 1: pass).
1	R/W	0x0	Gating AHB Clock for TVD(0: mask, 1: pass).
0	R/W	0x0	Gating AHB Clock for VE(0: mask, 1: pass).

1.5.4.20. APB0 MODULE CLOCK GATING(DEFAULT: 0X00000000)

Offset: 0x68			Register Name: APB0_GATING_REG
Bit	Read/ Write	Default/Hex	Description
31:11	/	/	/.
10	R/W	0x0	KEYPAD_APB_GATING. Gating APB Clock for Keypad(0: mask, 1: pass).

Offset: 0x68			Register Name: APB0_GATING_REG
Bit	Read/ Write	Default/Hex	Description
9	/	/	/
8	R/W	0x0	IIS2_APB_GATING. Gating APB Clock for IIS2(0: mask, 1: pass).
7	R/W	0x0	IR1_APB_GATING. Gating APB Clock for IR1(0: mask, 1: pass).
6	R/W	0x0	IR0_APB_GATING. Gating APB Clock for IR0(0: mask, 1: pass).
5	R/W	0x0	PIO_APB_GATING. Gating APB Clock for PIO(0: mask, 1: pass).
4	R/W	0x0	IIS1_APB_GATING. Gating APB Clock for IIS1(0: mask, 1: pass).
3	R/W	0x0	IIS0_APB_GATING. Gating APB Clock for IIS0(0: mask, 1: pass).
2	R/W	0x0	AC97_APB_GATING. Gating APB Clock for AC97(0: mask, 1: pass).
1	R/W	0x0	SPDIF_APB_GATING. Gating APB Clock for SPDIF(0: mask, 1: pass).
0	R/W	0x0	CODEC_APB_GATING. Gating APB Clock for Audio CODEC(0: mask, 1: pass).

1.5.4.21. APB1 MODULE CLOCK GATING(DEFAULT: 0X00000000)

Offset: 0x6C			Register Name: APB1_GATING_REG
Bit	Read/ Write	Default/Hex	Description
31:24	/	/	/.
23	R/W	0x0	UART7_APB_GATING. Gating APB Clock for UART7(0: mask, 1: pass).
22	R/W	0x0	UART6_APB_GATING. Gating APB Clock for UART6(0: mask, 1: pass).
21	R/W	0x0	UART5_APB_GATING. Gating APB Clock for UART5(0: mask, 1: pass).

Offset: 0x6C			Register Name: APB1_GATING_REG
Bit	Read/ Write	Default/Hex	Description
20	R/W	0x0	UART4_APB_GATING. Gating APB Clock for UART4(0: mask, 1: pass).
19	R/W	0x0	UART3_APB_GATING. Gating APB Clock for UART3(0: mask, 1: pass).
18	R/W	0x0	UART2_APB_GATING. Gating APB Clock for UART2(0: mask, 1: pass).
17	R/W	0x0	UART1_APB_GATING. Gating APB Clock for UART1(0: mask, 1: pass).
16	R/W	0x0	UART0_APB_GATING. Gating APB Clock for UART0(0: mask, 1: pass).
15	R/W	0x0	TWI4_APB_GATING. Gating APB Clock for TWI4(0: mask, 1: pass).
14:8	/	/	/
7	R/W	0x0	PS21_APB_GATING. Gating APB Clock for PS2-1(0: mask, 1: pass).
6	R/W	0x0	PS20_APB_GATING. Gating APB Clock for PS2-0(0: mask, 1: pass).
5	R/W	0x0	SCR_APB_GATING. Gating APB Clock for SCR(0: mask, 1: pass).
4	R/W	0x0	CAN_APB_GATING. Gating APB Clock for CAN(0: mask, 1: pass).
3	R/W	0x0	TWI3_APB_GATING. Gating APB Clock for TWI3(0: mask, 1: pass).
2	R/W	0x0	TWI2_APB_GATING. Gating APB Clock for TWI2(0: mask, 1: pass).
1	R/W	0x0	TWI1_APB_GATING. Gating APB Clock for TWI1(0: mask, 1: pass).
0	R/W	0x0	TWI0_APB_GATING. Gating APB Clock for TWI0(0: mask, 1: pass).

1.5.4.22. NAND CLOCK(DEFAULT: 0X00000000)

Offset: 0x80			Register Name: NAND_SCLK_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

Note: In practice, the module clock frequency is always switched off.

1.5.4.23. MS CLOCK(DEFAULT: 0X00000000)

Offset: 0x84			Register Name: MS_SCLK_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz)

Offset: 0x84			Register Name: MS_SCLK_CFG_REG
Bit	Read/ Write	Default/Hex	Description
			0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.24. SD/MMC 0 CLOCK(DEFAULT: 0X00000000)

Offset: 0x88			Register Name: SD0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select

Offset: 0x88			Register Name: SD0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			00: OSC24M 01: PLL6 10: PLL5 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.25. SD/MMC 1 CLOCK(DEFAULT: 0X00000000)

Offset: 0x8C			Register Name: SD1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON

Offset: 0x8C			Register Name: SD1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.26. SD/MMC 2 CLOCK(DEFAULT: 0X00000000)

Offset: 0x90			Register Name: SD2_CLK_REG
Bit	Read/ Write	Default/Hex	Description

Offset: 0x90			Register Name: SD2_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.27. SD/MMC 3 CLOCK(DEFAULT: 0X00000000)

Offset: 0x94			Register Name: SD3_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.28. TS CLOCK(DEFAULT: 0X00000000)

Offset: 0x98			Register Name: TS_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.29. SS CLOCK(DEFAULT: 0X00000000)

Offset: 0x9C			Register Name: SS_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON

Offset: 0x9C			Register Name: SS_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.30. SPI0 CLOCK(DEFAULT: 0X00000000)

Offset: 0xA0			Register Name: SPI0_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M

Offset: 0xA0			Register Name: SPI0_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.31. SPI1 CLOCK(DEFAULT: 0X00000000)

Offset: 0xA4			Register Name: SPI1_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n)

Offset: 0xA4			Register Name: SPI1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.32. SPI2 CLOCK(DEFAULT: 0X00000000)

Offset: 0xA8			Register Name: SPI2_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1

Offset: 0xA8			Register Name: SPI2_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			to 16.

1.5.4.33. IR 0 CLOCK(DEFAULT: 0X00000000)

Offset: 0xB0			Register Name: IR0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: LOSC.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.34. IR 1 CLOCK(DEFAULT: 0X00000000)

Offset: 0xB4	Register Name: IR1_CLK_REG

Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: LOSC.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.35. IIS0 CLOCK(DEFAULT: 0X00000000)

Offset: 0xB8			Register Name: IIS0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL2 (8x)

			01: PLL2(4X) 10: PLL2(2X) 11: PLL2(1X)
15:0	/	/	/.

1.5.4.36. AC97 CLOCK(DEFAULT: 0X00030000)

Offset: 0xBC			Register Name: AC97_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x3	CLK_SRC_SEL. 00: PLL2 (8x) 01: PLL2(4X) 10: PLL2(2X) 11: PLL2(1X)
15:0	/	/	/.

1.5.4.37. KEYPAD CLOCK(DEFAULT: 0X0000001F)

Offset: 0xC4			Register Name: KEYPAD_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: OSC24M

Offset: 0xC4			Register Name: KEYPAD_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			1: / 2: LOSC clock (32KHz) 3: /
23:18	/	/	/
17:16	R/W	0x0	CLK_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:5	/	/	/.
4:0	R/W	0x1f	CLK_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

1.5.4.38. SATA CLOCK(DEFAULT: 0X00000000)

Offset: 0xC8			Register Name: SATA_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON
30:25	/	/	/
24	R/W	0x0	CLK_SRC_GATING. Clock Source Select 0: PLL6 for SATA(100MHz) 1: External Clock
23:0	/	/	/

1.5.4.39. USB CLOCK(DEFAULT: 0X00000000)

Offset: 0xCC	Register Name: USB_CLK_REG

Bit	Read/ Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	SCLK_GATING_USBPHY. Gating Special Clock for USB PHY0/1/2 0: Clock is OFF 1: Clock is ON
7	R/W	0x0	SCLK_GATING_OHCI1. Gating Special Clock for OHCI1 0: Clock is OFF 1: Clock is ON
6	R/W	0x0	SCLK_GATING_OHCI0. Gating Special Clock for OHCI0 0: Clock is OFF 1: Clock is ON
5:3	/	/	/.
2	R/W	0x0	USBPHY2_RST. USB PHY2 Reset Control 0: Reset valid 1: Reset invalid
1	R/W	0x0	USBPHY1_RST. USB PHY1 Reset Control 0: Reset valid 1: Reset invalid
0	R/W	0x0	USBPHY0_RST. USB PHY0 Reset Control 0: Reset valid 1: Reset invalid

1.5.4.40. SPI3 CLOCK(DEFAULT: 0X00000000)

Offset: 0xD4			Register Name: SPI3_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz)

Offset: 0xD4			Register Name: SPI3_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/.
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.41. IIS1 CLOCK(DEFAULT: 0X00000000)

Offset: 0xD8			Register Name: IIS1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL2 (8x) 01: PLL2(4X)

Offset: 0xD8			Register Name: IIS1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			10: PLL2(2X) 11: PLL2(1X)
15:0	/	/	/.

1.5.4.42. IIS2 CLOCK(DEFAULT: 0X00000000)

Offset: 0xDC			Register Name: IIS2_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL2 (8x) 01: PLL2(4X) 10: PLL2(2X) 11: PLL2(1X)
15:0	/	/	/.

1.5.4.43. DRAM CLK(DEFAULT: 0X00000000)

Offset: 0x100			Register Name: DRAM_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	ACE_DCLK_GATING. Gating DRAM Clock for ACE(0: mask, 1: pass).
28	R/W	0x0	DE_MP_DCLK_GATING. Gating DRAM Clock for DE_MP(0: mask, 1: pass).
27	R/W	0x0	BE1_DCLK_GATING. Gating DRAM Clock for DE_BE1(0: mask, 1: pass).

Offset: 0x100			Register Name: DRAM_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
26	R/W	0x0	BE0_DCLK_GATING. Gating DRAM Clock for DE_BE0(0: mask, 1: pass).
25	R/W	0x0	FE0_DCLK_GATING. Gating DRAM Clock for DE_FE1(0: mask, 1: pass).
24	R/W	0x0	FE1_DCLK_GATING. Gating DRAM Clock for DE_FE0(0: mask, 1: pass).
23:16	/	/	/
15	R/W	0x0	DCLK_OUT_EN. DRAM Clock Output Enable(0: disable, 1: enable)
14:7	/	/	/
6	R/W	0x0	TVE1_DCLK_GATING. Gating DRAM Clock for TVE 1(0: mask, 1: pass).
5	R/W	0x0	TVE0_DCLK_GATING. Gating DRAM Clock for TVE 0(0: mask, 1: pass).
4	R/W	0x0	TVD_DCLK_GATING. Gating DRAM Clock for TVD(0: mask, 1: pass).
3	R/W	0x0	TS_DCLK_GATING. Gating DRAM Clock for TS(0: mask, 1: pass).
2	R/W	0x0	CSI1_DCLK_GATING. Gating DRAM Clock for CSI1(0: mask, 1: pass).
1	R/W	0x0	CSI0_DCLK_GATING. Gating DRAM Clock for CSI0(0: mask, 1: pass).
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM Clock for VE(0: mask, 1: pass).

1.5.4.44. DE-BE 0 CLOCK(DEFAULT: 0X00000000)

Offset: 0x104			Register Name: BE0_SCLK_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock

Offset: 0x104			Register Name: BE0_SCLK_CFG_REG
Bit	Read/ Write	Default/Hex	Description
			0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	BE0_RST. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL5 11: /.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

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1.5.4.45. DE-BE 1 CLOCK(DEFAULT: 0X00000000)

Offset: 0x108			Register Name: BE1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	BE1_RST. DE-BE1 Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select

Offset: 0x108			Register Name: BE1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			00: PLL3 01: PLL7 10: PLL5 11: /.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.46. DE-FE 0 CLOCK(DEFAULT: 0X00000000)

Offset: 0x10C			Register Name: FE0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	FE0_RST. DE-FE0 Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL5 11: /.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from

Offset: 0x10C			Register Name: FE0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			1 to 16.

1.5.4.47. DE-FE 1 CLOCK(DEFAULT: 0X00000000)

Offset: 0x110			Register Name: FE1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	FE1_RST. DE-FE1 Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL5 11: /.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.48. DE-MP CLOCK(DEFAULT: 0X00000000)

Offset: 0x114			Register Name: MP_CLK_REG
Bit	Read/ Write	Default/Hex	Description

Offset: 0x114			Register Name: MP_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	MP_RST. DE-MP Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL5 11: /.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.49. LCD 0 CH0 CLOCK(DEFAULT: 0X00000000)

Offset: 0x118			Register Name: LCD0_CH0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source
30	R/W	0x0	LCD0_RST. LCD0 Reset. 0: reset valid, 1: reset invalid.

Offset: 0x118			Register Name: LCD0_CH0_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL6*2
23:0	/	/	/

1.5.4.50. LCD 1 CH0 CLOCK(DEFAULT: 0X00000000)

Offset: 0x11C			Register Name: LCD1_CH0_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source
30	R/W	0x0	LCD1_RST. LCD1 Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:0	/	/	/

1.5.4.51. CSI SPECIAL CLOCK REGITSTER(DEFAULT: 0X00000000)

Offset: 0x120			Register Name: CSI_SCLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK2_SRC_SEL. Special Clock 2 Source Select 00: PLL3(1X) 01: PLL4 10: PLL5 11: PLL6
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.52. TVD CLOCK(DEFAULT: 0X00000000)

Offset: 0x128			Register Name: TVD_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK2_GATING. Gating Special Clock 2 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ CLK_DIV_RATIO1_M. Gating Special Clock 1 should be ON at the same time.
30:20	/	/	/
19:16	R/W	0x0	CLK_DIV_RATIO2_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
15	R/W	0x0	SCLK1_GATING. Gating Special Clock 1

			0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ CLK_DIV_RATIO1_M/CLK_DIV_RATIO2_M.
14:9	/	/	/
8	R/W	0x0	CLK1_SRC_SEL. Clock Source Select 0: PLL3 1: PLL7
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO1_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.53. LCD 0 CH1 CLOCK(DEFAULT: 0X00000000)

Offset: 0x12C			**Register Name: LCD0_CH1_CLK_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK2_GATING. Gating Special Clock 2 0: Clock is OFF 1: Clock is ON This special clock 2= Special Clock 2 Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK2_SEL. Special Clock 2 Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:16	/	/	/
15	R/W	0x0	SCLK1_GATING. Gating Special Clock 1 0: Clock is OFF 1: Clock is ON This special clock 1= Special Clock 1 Source.
14:12	/	/	/
11	R/W	0	SCLK1_SRC_SEL.

Offset: 0x12C			Register Name: LCD0_CH1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			Special Clock 1 Source Select. 0: Special Clock 2 1: Speical Clock 2 divide by 2
10:4	/	/	/.
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.54. LCD 1 CH1 CLOCK(DEFAULT: 0X00000000)

Offset: 0x130			Register Name: LCD1_CH1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK2_GATING. Gating Special Clock 2 0: Clock is OFF 1: Clock is ON This special clock 2= Special Clock 2 Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK2_SRC_SEL. Special Clock 2 Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:16	/	/	/
15	R/W	0x0	SCLK1_GATING. Gating Special Clock 1 0: Clock is OFF 1: Clock is ON This special clock 1= Special Clock 1 Source.
14:12	/	/	/
11	R/W	0x0	SCLK1_SRC_SEL.

Offset: 0x130			Register Name: LCD1_CH1_CLK_REG
Bit	Read/ Write	Default/Hex	Description
			Special Clock 1 Source Select. 0: Special Clock 2 1: Speical Clock 2 divide by 2
10:4	/	/	/.
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.55. CSI 0 CLOCK(DEFAULT: 0X00000000)

Offset: 0x134			Register Name: CSI0_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	CSI0_RST. CSI0 Reset. 0: reset valid, 1: reset invalid.
29:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL3(1X) 010: PLL7(1X) 011: / 100: / 101: PLL3(2X) 110: PLL7(2X) 111: /
23:5	/	/	/

Offset: 0x134			Register Name: CSI0_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
4:0	/	/	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

1.5.4.56. CSI 1 CLOCK(DEFAULT: 0X00000000)

Offset: 0x138			Register Name: CSI1_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	CSI1_RST. CSI1 Reset. 0: reset valid, 1: reset invalid.
29:27	/	/	/
26:24	R/W	0x0	Clock Source Select 000: OSC24M 001: PLL3(1X) 010: PLL7(1X) 011: / 100: / 101: PLL3(2X) 110: PLL7(2X) 111: /
23:5	/	/	/
4:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

1.5.4.57. VE CLOCK(DEFAULT: 0X00000000)

Offset: 0x13C			Register Name: VE_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating the Special clock for VE(0: mask, 1: pass). Its clock source is the PLL4 output. This special clock = Clock Source/Divider N.
30:19	/	/	/.
18:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (N) The select clock source is pre-divided by n+1. The divider is from 1 to 8.
15:1	/	/	/
0	R/W	0x0	VE_RST. VE Reset. 0: reset valid, 1: reset invalid.

1.5.4.58. AUDIO CODEC CLOCK(DEFAULT: 0X00000000)

Offset: 0x140			Register Name: AUDIO_CODEC_CLK_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = PLL2 output.
30:0	/	/	/

1.5.4.59. AVS CLOCK(DEFAULT: 0X00000000)

Offset: 0x144			Register Name: AVS_CLK_REG
Bit	Read/ Write	Default/Hex	Description

Offset: 0x144			Register Name: AVS_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = OSC24M.
30:0	/	/	/

1.5.4.60. ACE CLOCK(DEFAULT: 0X00000000)

Offset: 0x148			Register Name: ACE_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL4 1: PLL5
23:17	/	/	/
16	R/W	0x0	ACE_RST. ACE Reset. 0: reset valid, 1: reset invalid
15:4	/	/	/.
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.61. LVDS CLOCK(DEFAULT: 0X00000000)

Offset: 0x14C			Register Name:LVDS_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R/W	0x0	LVDS_RST. LVDS reset. 0: reset valid, 1: reset invalid.

1.5.4.62. HDMI CLOCK(DEFAULT: 0X00000000)

Offset: 0x150			Register Name: HDMI_CLK_REG.
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ Divider M
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.63. MALI400 CLOCK(DEFAULT: 0X00000000)

Offset: 0x154	Register Name: MALI400_CLK_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 381MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	MALI400_RST. Mali400 Reset. 0: reset valid, 1: reset invalid
29:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3 001: PLL4 010: PLL5 011: PLL7 100: PLL8 101:/ 110:/ 111:/
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.64. MBUS CLOCK CONTROL(DEFAULT: 0X00000000)

Offset: 0x15C			Register Name: MBUS_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS 0: Clock is OFF, 1: Clock is ON;

Offset: 0x15C			Register Name: MBUS_SCLK_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			MBUS_CLOCK = Clock Source/Divider N/Divider M
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select 00: OSC24M 01: PLL6*2 10: PLL5 11: Reserved
23:18	/	/	/
17:16	R/W	0x0	MBUS_SCLK_RATIO_N Clock Pre-divide Ratio (N) The select clock source is pre-divided by 2^N. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (M) The divided clock is divided by (M+1). The divider is from 1 to 16.

1.5.4.65. GMAC CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x164			Register Name: GMAC_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0	TXC_DIV_CFG Clock pre-divide ratio(n) External transmit clock (125MHz) is pre-divided by as follows for RGMII. 00:/1, generate 125MHz; 01:/5,generate 25 MHz; 10: /50,generate 2.5 MHz 11: Reserved

Offset: 0x164			Register Name: GMAC_CLK_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
7:5	R/W	0	GRXDC Configure GMAC Receive Clock Delay Chian. 000: 001: … 111:
4	R/W	0	GRXIE Enable GMAC Receive Clock Invertor. 0: Disable; 1: Enable;
3	R/W	0	GTXIE Enable GMAC Transmit Clock Invertor. 0: Disable; 1: Enable;
2	R/W	0	GPIT GMAC PHY Interface Type 0: MII; 1: RGMII;
1:0	R/W	0	GTCS GMAC Transmit Clock Source 00: Transmit clock source for MII; 01: External transmit clock source(125MHz) for RGMII; 10: Internal transmit clock source for RGMII; 11: Reserved;

1.5.4.66. HDMI1 RESET REGISTER (DEFAULT: 0X00000000)

Offset: 0x170			Register Name: HDMI1_RST_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	AUDIO_DMA_RST Audio_dma reset.

Offset: 0x170			**Register Name: HDMI1_RST_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
			0: assert. 1:de-assert.
1	R/W	0x0	SYSRST. HDMI1 system reset 0: assert. 1:de-assert.
0	R/W	0x0	HRST hreset 0: assert. 1:de-assert.

1.5.4.67. HDMI1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x174			Register Name: HDMI1_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	HDMI1 System Control Register

1.5.4.68. HDMI1 SLOW CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x178			**Register Name: HDMI1_SLOW_CLK_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock is OSC24M.
30:0	/	/	/

1.5.4.69. HDMI1 REPEAT CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x17C	**Register Name: HDMI1_REPEAT_CLK_REG**

Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10:/ 11:/
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

1.5.4.70. CLK_OUTA_REG (DEFAULT: 0X00000000)

Offset: 0x1F0			Register Name: CLK_OUTA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUT_EN Clock Output Enable 0: disable 1: Clock Output Enable OutputA = Clock Source / DIVIDOR-N / DIVIDOR-M.
30:26	/	/	/
25:24	R/W	0x0	CLK_OUT_SRC_SEL 00: OSC24MHz/750=32KHz 01: Losc 10: OSC24MHz 11: /

Offset: 0x1F0			Register Name: CLK_OUTA_REG
Bit	Read/ Write	Default/Hex	Description
23:22	/	/	/
21:20	R/W	0x0	DIVIDOR_N Clock Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:13	/	/	/
12:8	R/W	0x0	DIVIDOR_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

1.5.4.71. CLK_OUTB_REG (DEFAULT: 0X00000000)

Offset: 0x1F4			Register Name: CLK_OUTB_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	CLK_OUT_EN Clock Output Enable 0: disable 1: Clock Output Enable OutputB = Clock Source / DIVIDOR-N / DIVIDOR-M.
30:26	/	/	/
25:24	R/W	0x0	CLK_OUT_SRC_SEL 00: OSC24MHz/750=32KHz 01: Losc 10: OSC24MHz 11: /

Offset: 0x1F4			Register Name: CLK_OUTB_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
23:22	/	/	/
21:20	R/W	0x0	DIVIDOR_N Clock Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:13	/	/	/
12:8	R/W	0x0	DIVIDOR_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

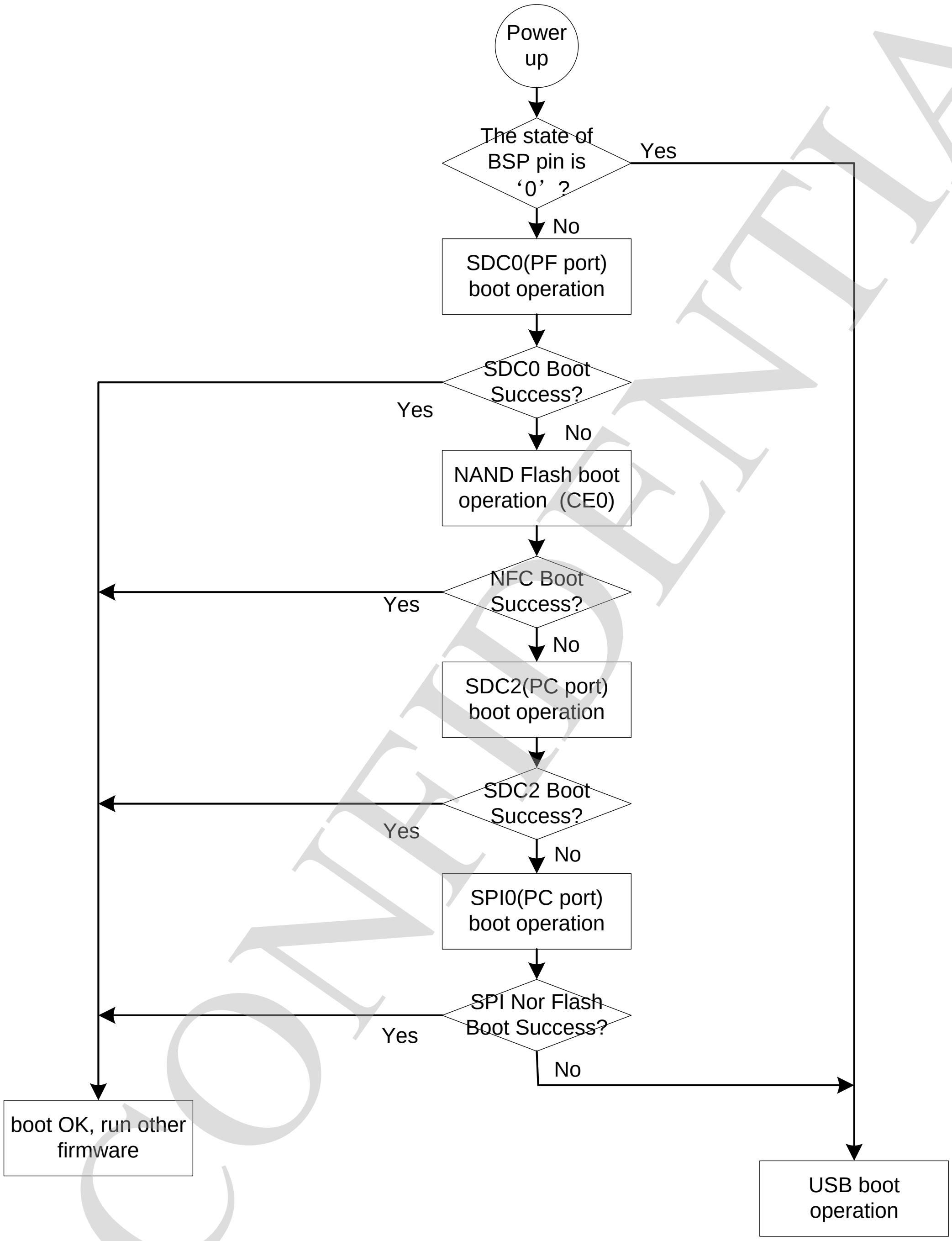
1.6. System Boot

1.6.1. Overview

A20 supports system boot from NAND Flash, SPI NOR Flash (SPI0), SD card (SDC 0/2), and USB.

After power on, the system will try to boot from SDC0, NAND Flash, SDC2, SPI0, and USB successively, but if the Boot Select Pin, or BSP, an external pin that is used to select system boot method, is checked to be in low level state, the system will direclty boot from USB. In normal state, this pin is pulled up by an internal 50K resistor.

1.6.2. System Boot Diagram



1.7. System Control

1.7.1. Overview

The chip embeds a high-speed SRAM. This internal SRAM is split into five areas, and its memory mapping can be seen below:

Area	Address	Size(Bytes)
A1	0x00000000--0x00003FFF	16K
A2	0x00004000--0x00007FFF	16K
A3	0x00008000--0x0000B3FF	13K
A4	0x0000B400--0x0000BFFF	3K
C1	0x01D00000-0x01D7FFFF	VE
NAND		2K
D(USB)	0x00010000—0x00010FFF	4K
B(Secure RAM)	0x00020000--0x0002FFFF	64K
CPU0 I-Cache		32K
CPU0 D-Cache		32K
CPU1 I-Cache		32K
CPU1 D-Cache		32K
CPU L2 Cache		256K
Total		502K

1.7.2. System Control Register List

Module Name	Base Address
SYS_CTRL	0x01C00000

Register Name	Offset	Description
SRAM_CTRL_REG0	0x0	SRAM Control Register 0
SRAM_CTRL_REG1	0x4	SRAM Control Register 1
VER_REG	0x24	Version Register
NMI_IRQ_CTRL_REG	0x30	NMI Interrupt Control Register
NMI_IRQ_PEND_REG	0x34	NMI Interrupt Pending Register
NMI_IRQ_ENABLE_REG	0x38	NMI Interrupt Enable Register

1.7.3. System Control Register

1.7.3.1. SRAM CONTROL REGISTER 0(DEFAULT: 0X7FFFFFFF)

Offset: 0x0			Register Name: SRAM_CTRL_REG0
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	/	/	/
30:0	R/W	0x7fffffff	SRAM_C1_MAP. SRAM Area C1 50K Bytes Configuration by AHB. 0: map to CPU/DMA 1: map to VE

1.7.3.2. SRAM CONTROL REGISTER 1(DEFAULT: 0X00001300)

Offset: 0x4	Register Name: SRAM_CTRL_REG1

Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	BIST_NDMA_CTRL_SEL. Bist and Normal DMA control select. 0: N-DMA, 1: Bist.
30:13	/	/	/.
12	R/W	0x1	SRAM_C3_MAP. SRAM C3 map config. 0: map to CPU/BIST 1: map to ISP
11:10	/	/	/
9:8	R/W	0x3	SRAM_C2_MAP. SRAM C2 map config. 0: map to CPU/BIST 1: map to AE 2: map to CE 3: map to ACE
7:6	/	/	/.
5:4	R/W	0x0	SRAM_A3_A4_MAP. SRAM Area A3/A4 Configuration by AHB. 00: map to CPU/DMA 01: map to EMAC 10: / 11: /
3:1	/	/	/.
0	R/W	0x0	SRAMD_MAP. SRAM D Area Config. 0: map to CPU/DMA 1: map to USB0

1.7.3.3. VERSION REGISTER(DEFAULT: 0X00000000)

Offset: 0x24			Register Name: VER_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	KEY_FIELD.

Offset: 0x24			Register Name: VER_REG
Bit	Read/ Write	Default/Hex	Description
			The bit[31:16] will be 0x1651 if bit15 is set, otherwise it will be 0.
15	R/W	0x0	VER_R_EN. Version Reg Bit[31:16] Read Option Enable. 0: Disable, 1: Enable.
14:9	/	/	/.
8	R	x	BOOT_SEL_PAD_STA. BootSelect Pin Status 0: Low Level 1: High Level The bit indicates current status of external BootSelect pin. In default state, this pin is pull high by internal register and normal boot is running. When this pin is drived to low level, normal boot is bypassed and it would jump to USB for special application, such as firmware update etc. The status of BootSelect pin should be sampled by APB clock. The debounce work is left for software.
7:0	R	0x0	VER_BITS. This read-only bit field always reads back the mask revision level of the chip.

1.7.3.4. NMI INTERRUPT CONTROL REGISTER(DEFAULT: 0X00000000)

Offset:0x30			Register Name: NMI_IRQ_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	NMI_IRQ_SRC_TYPE. External NMI Interrupt Source Type. External NMI pin will be changed to alarm output if the power of I/O is switched off, and it’s power source is RTCVDD. 00: Low level sensitive 01: Negative edge trigged 10: High level sensitive 11: Positive edge sensitive

1.7.3.5. NMI INTERRUPT PENDING REGISTER(DEFAULT: 0X00000000)

Offset:0x34			Register Name: NMI_IRQ_PEND_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	NMI_IRQ_SRC_PEND. NMI Source Pending and Clear Bit. 0: NMI interrupt is not pending. 1: NMI interrupt is pending

1.7.3.6. NMI INTERRUPT ENABLE REGISTER(DEFAULT: 0X00000000)

Offset:0x38			Register Name: NMI_IRQ_ENABLE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	NMI_IRQ_SRC_ENABLE. NMI Source Enable and Disable Bit. 0: NMI interrupt is disable. 1: NMI interrupt is enable

1.8. PWM

1.8.1. Overview

The PWM signals can be used for LCD contrast and brightness control.

The PWM outputs a toggling signal, whose frequency and duty cycle can be modulated in its programmable registers. Each channel has a dedicated internal 16-bit up counter, which will be reset if it reaches the value stored in the channel period register. At the beginning of a count period cycle, the PWMOUT is set to active state and counts from 0x0000.

The PWM divider divides the clock (24MHz) by 1~4096 according to the pre-scalar bits in PWM control register.

PWM has two modes: in PWM cycle mode, the output will be a square waveform, and the frequency is set to the period register; in PWM pulse mode, the output will be a positive pulse or a negative pulse.

1.8.2. PWM Register List

Module Name	Base Address
PWM	0x01C20C00

Register Name	Offset	Description
PWM_CTRL_REG	0x200	PWM Control Register
PWM_CH0_PERIOD	0x204	PWM Channel 0 Period Register
PWM_CH1_PERIOD	0x208	PWM Channel 1 Period Register

1.8.3. PWM Register Description

1.8.3.1. PWM CONTROL REGISTER(DEFAULT: 0X00000000)

Offset: 0x200			Register Name: PWM_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/.
29	RO	0x0	PWM1_RDY. PWM1 period register ready. 0: PWM1 period register is ready to write, 1: PWM1 period register is busy.
28	RO	0x0	PWM0_RDY. PWM0 period register ready. 0: PWM0 period register is ready to write, 1: PWM0 period register is busy.
27:25	/	/	/
24	R/W	0x0	PWM1_BYPASS. PWM CH1 bypass enable. If the bit is set to 1, PWM1’s output is OSC24MHz. 0: disable

Offset: 0x200			Register Name: PWM_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			1: enable
23	R/W	0x0	PWM_CH1_PULSE_OUT_START. PWM Channel 1 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 1 register[15:0],and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.
22	R/W	0x0	PWM_CH1_MODE. PWM Channel 1 mode. 0: cycle mode, 1: pulse mode.
21	R/W	0x0	PWM_CH1_CLK_GATING Gating the Special Clock for PWM1(0: mask, 1: pass).
20	R/W	0x0	PWM_CH1_ACT_STATE. PWM Channel 1 Active State. 0: Low Level, 1: High Level.
19	R/W	0x0	PWM_CH1_EN. PWM Channel 1 Enable. 0: Disable, 1: Enable.
18:15	R/W	0x0	PWM_CH1_PRESCAL. PWM Channel 1 Prescalar. These bits should be setting before the PWM Channel 1 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k

Offset: 0x200			Register Name: PWM_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			1100: /72k 1101: / 1110: / 1111: /1
14:10	/	/	/
9	R/W	0x0	PWM0_BYPASS. PWM CH0 bypass enable. If the bit is set to 1, PWM0's output is OSC24MHz. 0: disable, 1: enable.
8	R/W	0x0	PWM_CH0_PUL_START. PWM Channel 0 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 0 register[15:0],and the pulse state should be according to the active state. After the pulse is finished,the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL0_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH0_GATING. Gating the Special Clock for PWM0(0: mask, 1: pass).
5	R/W	0x0	PWM_CH0_ACT_STA. PWM Channel 0 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH0_PRESCAL. PWM Channel 0 Prescalar. These bits should be setting before the PWM Channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360

Offset: 0x200			Register Name: PWM_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1

1.8.3.2. PWM CHANNEL 0 PERIOD REGISTER

Offset: 0x204			Register Name: PWM_CH0_PERIOD
Bit	Read/ Write	Default/Hex	Description
31:16	R/W	x	PWM_CH0_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register needs to be modified dynamically, the PCLK should be faster than the PWM CLK(PWM CLK = 24MHz/prescale).
15:0	R/W	x	PWM_CH0_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Note: the active cycles should be no larger than the period cycles.

1.8.3.3. PWM CHANNEL 1 PERIOD REGISTER

Offset: 0x208			Register Name: PWM_CH1_PERIOD
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R/W	x	PWM_CH1_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 If the register needs to be modified dynamically, the PCLK should be faster than the PWM CLK(PWM CLK = 24MHz/prescale).
15:0	R/W	x	PWM_CH1_ENTIRE_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

1.9. Timer

1.9.1. Overview

A20 implements 6 timers.

Timer 0 and Timer 1 can take their inputs from internal RC oscillator, external 32768Hz crystal or OSC24M. They provide scheduler interrupt for OS to offer maximum accuracy and efficient management for systems with long or short response time. A 24-bit programmable overflow counter is supported, which can work in auto-reload mode or no-reload mode.

Timer 2 is used for OS to generate a periodic interrupt.

The watchdog is used to resume the controller operation when it is disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds. It can generate a general reset or a interrupt request.

The real time clock is there for calendar usage It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system is power off. It has a built-in leap year generator and a independent power pin(RTCVDD).

The alarm is used to generate an alarm signal at a specified time in power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated while in power-off mode, only the power management wakeup signal is activated.

1.9.2. Timer Register List

Module Name	Base Address
Timer	0x01C20C00

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x4	Timer Status Register
TMR0_CTRL_REG	0x10	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x14	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x18	Timer 0 Current Value Register
TMR1_CTRL_REG	0x20	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x24	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x28	Timer 1 Current Value Register
TMR2_CTRL_REG	0x30	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x34	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x38	Timer 2 Current Value Register
TMR3_CTRL_REG	0x40	Timer 3 Control Register
TMR3_INTV_VALUE_REG	0x44	Timer 3 Interval Value Register
TMR4_CTRL_REG	0x50	Timer 4 Control Register
TMR4_INTV_VALUE_REG	0x54	Timer 4 Interval Value Register
TMR4_CUR_VALUE_REG	0x58	Timer 4 Current Value Register
TMR5_CTRL_REG	0x60	Timer 5 Control Register
TMR5_INTV_VALUE_REG	0x64	Timer 5 Interval Value Register
TMR5_CUR_VALUE_REG	0x68	Timer 5 Current Value Register
AVS_CNT_CTL_REG	0x80	AVS Control Register
AVS_CNT0_REG	0x84	AVS Counter 0 Register
AVS_CNT1_REG	0x88	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x8C	AVS Divisor Register
WDOG_CTRL_REG	0x90	Watchdog Control Register
WDOG_MODE_REG	0x94	Watchdog Mode Register
LOSC_CTRL_REG	0x100	Low Oscillator Control Register

Register Name	Offset	Description
RTC_YY_MM_DD_REG	0x104	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x108	RTC Hour-Minute-Second Register
DD_HH_MM_SS_REG	0x10C	Alarm Day-Hour-Minute-Second Register
ALARM_WK_HH_MM-SS	0x110	Alarm Week HMS Register
ALARM_EN_REG	0x114	Alarm Enable Register
ALARM_IRQ_EN	0x118	Alarm IRQ Enable Register
ALARM_IRQ_STA_REG	0x11C	Alarm IRQ Status Register
TMR_GP_DATA_REG	0x120 + N*0x4	Timer General Purpose Register (N=0~15)
ALARM_CONFIG_REG	0x170	Alarm Config Register

1.9.3. Timer Register Description

1.9.3.1. TIMER IRQ ENABLE REGISTER(DEFAULT: 0X00000000)

Offset: 0x0			**Register Name: TMR_IRQ_EN_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:9	/	/	/.
8	R/W	0x0	WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: No effect, 1: watchdog Interval Value reached interrupt enable.
7:6	/	/	/
5	R/W	0x0	TMR5_IRQ_EN. Timer 5 Interrupt Enable. 0: No effect, 1: Timer 5 Interval Value reached interrupt enable.
4	R/W	0x0	TMR4_IRQ_EN. Timer 4 Interrupt Enable. 0: No effect, 1: Timer 4 Interval Value reached interrupt enable.
3	R/W	0x0	TMR3_IRQ_EN. Timer 3 Interrupt Enable.

Offset: 0x0			Register Name: TMR_IRQ_EN_REG
Bit	Read/ Write	Default/Hex	Description
			0: No effect, 1: Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: No effect, 1: Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect, 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect, 1: Timer 0 Interval Value reached interrupt enable.

1.9.3.2. TIMER IRQ STATUS REGISTER(DEFAULT: 0X00000000)

Offset: 0x4			Register Name: TMR_IRQ_STA_REG
Bit	Read/ Write	Default/Hex	Description
31:9	/	/	/.
8	R/W	0x0	WDOG_IRQ_PEND. Watchdog IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog counter value is reached.
7:6	/	/	/
5	R/W	0x0	TMR5_IRQ_PEND. Timer 5 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 5 counter value is reached.
4	R/W	0x0	TMR4_IRQ_PEND. Timer 4 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 4 counter value is reached.
3	R/W	0x0	TMR3_IRQ_PEND. Timer 3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 3 counter value is reached.
2	R/W	0x0	TMR2_IRQ_PEND. Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 2 counter value is reached.

Offset: 0x4			Register Name: TMR_IRQ_STA_REG
Bit	Read/ Write	Default/Hex	Description
1	R/W	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 1 interval value is reached.
0	R/W	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 0 interval value is reached.

1.9.3.3. TIMER 0 CONTROL REGISTER(DEFAULT: 0X00000004)

Offset: 0x10			Register Name: TMR0_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:8	/	/	/.
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer 0 Clock Source. 00: Low speed OSC, 01: OSC24M. 10: PLL6/6

Offset: 0x10			Register Name: TMR0_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			11: /.
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect, 1: Reload timer 0 Interval value.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note: the time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

1.9.3.4. TIMER 0 INTERVAL VALUE REGISTER

Offset: 0x14			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	TMR0_INTV_VALUE. Timer 0 Interval Value.

Note: when you set the value, please take into consideration the system clock and the timer clock source.

1.9.3.5. TIMER 0 CURRENT VALUE REGISTER

Offset: 0x18			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**

Offset: 0x18			Register Name: TMR0_CUR_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

Note: Timer 0 current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).

1.9.3.6. TIMER 1 CONTROL REGISTER(DEFAULT: 0X00000004)

Offset: 0x20			Register Name: TMR1_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:8	/	/	/.
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer 1 Clock Source. 00: Low speed OSC, 01: OSC24M. 10: PLL6/6 11: /.
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload.

Offset: 0x20			Register Name: TMR1_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			0: No effect, 1: Reload timer 1 Interval value.
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note: the time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

1.9.3.7. TIMER 1 INTERVAL VALUE REGISTER

Offset: 0x24			Register Name: TMR1_INTV_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	TMR1_INTV_VALUE. Timer 1 Interval Value.

Note: the value setting should take into consideration the system clock and the timer clock source.

1.9.3.8. TIMER 1 CURRENT VALUE REGISTER

Offset: 0x28			Register Name: TMR1_CUR_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

Note: Timer 1 current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).

1.9.3.9. TIMER 2 CONTROL REGISTER(DEFAULT: 0X00000004)

Offset: 0x30			Register Name: TMR2_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7	R/W	0x0	TMR2_MODE. Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR2_CLK_PRES. Select the pre-scale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer 2 Clock Source. 00: Low speed OSC, 01: OSC24M. 1x: /.
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect, 1: Reload timer 2 Interval value.
0	R/W	0x0	TMR2_EN. Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be

Offset: 0x30			Register Name: TMR2_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note: the time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

1.9.3.10. TIMER 2 INTERVAL VALUE REGISTER

Offset: 0x34			Register Name: TMR2_INTV_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	TMR2_INTV_VALUE. Timer 2 Interval Value.

Note: the value setting should consider the system clock and the timer clock source.

1.9.3.11. TIMER 2 CURRENT VALUE REGISTER

Offset: 0x38			Register Name: TMR2_CUR_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_CUR_VALUE. Timer 2 Current Value.

Note: Timer current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).

1.9.3.12. TIMER 3 CONTROL REGISTER(DEFAULT: 0X00000000)

Offset: 0x40			Register Name: TMR3_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:5	/	/	/.
4	R/W	0x0	TMR3_MODE. Timer 3 mode. 0: Continuous mode. When interval value reached, the

Offset: 0x40			Register Name: TMR3_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
3:2	R/W	0x0	TMR3_CLK_PRES. Select the pre-scale of timer 3 clock source. Timer 3 clock source is the LOSC. 00: /16 01: /32 10: /64 11: /
1	/	/	/
0	R/W	0x0	TMR3_EN. Timer 3 Enable. 0: Disable, 1: Enable.

Note: the time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

1.9.3.13. TIMER 3 INTERVAL VALUE REGISTER

Offset: 0x44			Register Name: TMR3_INTV_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	TMR3_INTV_VALUE. Timer 3 Interval Value.

1.9.3.14. TIMER 4 CONTROL REGISTER(DEFAULT: 0X00000004)

Offset: 0x50			Register Name: TMR4_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:8	/	/	/.
7	R/W	0x0	TMR4_MODE. Timer 4 mode. 0: Continuous mode. When interval value reached, the

Offset: 0x50			Register Name: TMR4_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR4_CLK_PRES. Select the pre-scale of timer 4 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR4_CLK_SRC. Timer 4 Clock Source. 00: Low speed OSC, 01: OSC24M. 10: External CLKIN0 11: /.
1	R/W	0x0	TMR4_RELOAD. Timer 4 Reload. 0: No effect, 1: Reload timer 4 Interval value.
0	R/W	0x0	TMR4_EN. Timer 4 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note:

1) if the clock source is external CLKIN, the interval value register is not used, the current value register is an up counter that counting from 0;

2) the time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

1.9.3.15. TIMER 4 INTERVAL VALUE REGISTER

Offset: 0x54			Register Name: TMR4_INTV_VALUE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	TMR4_INTV_VALUE. Timer 4 Interval Value.

Note: the value setting should take the system clock and the timer clock source into consideration.

1.9.3.16. TIMER 4 CURRENT VALUE REGISTER

Offset: 0x58			Register Name: TMR4_CUR_VALUE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	TMR4_CUR_VALUE. Timer 4 Current Value.

Note:
1) Timer current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale);
2) Before the timer 4 is enabled, the timer 4 current value register needs to be written with zero.

1.9.3.17. TIMER 5 CONTROL REGISTER(DEFAULT: 0X00000004)

Offset: 0x60			Register Name: TMR5_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7	R/W	0x0	TMR5_MODE. Timer 5 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR5_CLK_PRES.

Offset: 0x60			Register Name: TMR5_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			Select the pre-scale of timer 5 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR5_CLK_SRC. Timer 5 Clock Source. 00: Low speed OSC, 01: OSC24M. 10: External CLKIN1 11: /.
1	R/W	0x0	TMR5_RELOAD. Timer 5 Reload. 0: No effect, 1: Reload timer 5 Interval value.
0	R/W	0x0	TMR5_EN. Timer 5 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note:

1) If the clock source is External CLKIN, the interval value register is not used, the current value register is an up counter that counts from 0;

2) The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

1.9.3.18. TIMER 5 INTERVAL VALUE REGISTER

Offset: 0x64			Register Name: TMR5_INTV_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	TMR5_INTV_VALUE. Timer 5 Interval Value.

Note: When you set the value, please take into consideration the system clock and the timer clock source.

1.9.3.19. TIMER 5 CURRENT VALUE REGISTER

Offset: 0x68			Register Name: TMR5_CUR_VALUE_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	TMR5_CUR_VALUE. Timer 5 Current Value.

Note:

1) Timer 1 current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale);

2) Before timer 5 is enabled, timer 5 current value register needs to be written with zero.

1.9.3.20. AVS COUNTER CONTROL REGISTER(DEFAULT: 0X00000000)

Offset: 0x80			Register Name: AVS_CNT_CTL_REG
Bit	Read /Write	Default	Description
31:10	/	/	/
9	R	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0

Offset: 0x80			Register Name: AVS_CNT_CTL_REG
Bit	**Read /Write**	**Default**	**Description**
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable

1.9.3.21. AVS COUNTER 0 REGISTER(DEFAULT: 0X00000000)

Offset: 0x84			Register Name: AVS_CNT0_REG
Bit	**Read /Write**	**Default**	**Description**
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to ‘1’. When it is paused, the counter won’t increase.

1.9.3.22. AVS COUNTER 1 REGISTER(DEFAULT: 0X00000000)

Offset: 0x88			Register Name: AVS_CNT1_REG
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set

Offset: 0x88			Register Name: AVS_CNT1_REG
Bit	Read/Write	Default	Description
			by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter won't increase.

1.9.3.23. AVS COUNTER DIVISOR REGISTER(DEFAULT: 0X05DB05DB)

Offset: 0x8C			Register Name: AVS_CNT_DIV_REG
Bit	Read /Write	Default	Description
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit[27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. Notes: It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit[11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. Notes: It can be configured by software at any time.

1.9.3.24. WATCHDOG CONTROL REGISTER

Offset: 0x90			Register Name: WDOG_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R/W	0x0	WDOG_RSTART. Watchdog Restart. 0: No effect, 1: Restart the Watchdog.

1.9.3.25. WATCHDOG MODE REGISTER(DEFAULT: 0X00000000)

Offset: 0x94			Register Name: WDOG_MODE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:7	/	/	/.
6:3	R/W	0x0	WDOG_INTV_VALUE. Watchdog Interval Value Watchdog clock source is OSC24M. if the OSC24M is turned off, the watchdog will not work. 0000: 0.5sec 0001: 1sec 0010: 2sec 0011: 3sec 0100: 4sec 0101: 5sec 0110: 6sec 0111: 8sec 1000: 10sec 1001: 12sec 1010: 14sec 1011: 16sec 1100: / 1101: / 1110: / 1111: /

Offset: 0x94			Register Name: WDOG_MODE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
2	/	/	/
1	R/W	0x0	WDOG_RST_EN. Watchdog Reset Enable. 0: No effect on the resets, 1: Enables the Watchdog to activate the system reset.
0	R/W	0x0	WDOG_EN. Watchdog Enable. 0: No effect, 1: Enable the Watchdog.

1.9.3.26. LOSC CONTROL REGISTER (DEFAULT: 0X00004000)

Offset: 0x100			Register Name: LOSC_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, then the bit 0 can be written with the new value.
15	R/W	0x0	CLK32K_AUTO_SWT_PEND. CLK32K auto switch pending. 0: no effect, 1: auto switch pending.
14	R/W	0x1	CLK32K_AUTO_SWT_EN. CLK32K auto switch enable. 0: Disable, 1: Enable.
13:10	/	/	/.
9	R/W	0x0	ALM_DDHHMMSS_ACCE. ALARM DD-HH-MM-SS access. After writing the ALARM DD-HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second.

Offset: 0x100			Register Name: LOSC_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
7	R/W	0x0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the RTC YY-MM-DD register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second.
6:4	/	/	/
3:2	R/W	0x0	EXT_LOSC_GSM. External 32768Hz Crystal GSM. 00 low 01 10 11 high
1	/	/	/
0	R/W	0x0	OSC32K_SRC_SEL. OSC32KHz Clock source Select. 0: Internal 32khz, 1: External 32.768KHz OSC.

Note: If any bit of [9:7] is set, the RTC HH-MM-SS, YY-MM-DD and ALARM DD-HH-MM-SS register can't be written.

1.9.3.27. RTC YY-MM-DD REGISTER (DEFAULT: 0X00000000)

Offset: 0x104			Register Name: RTC_YY_MM_DD_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30	R/W	0x0	RTC_SIM_CTRL. RTC Simulation Control bit.
29:25	/	/	/.
24	R/W	0x0	LEAP. Leap Year. 0: not, 1: Leap year. This bit can not set by hardware. It should be set or clear by software.

Offset: 0x104			Register Name: RTC_YY_MM_DD_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
23:16	R/W	x	YEAR. Year. Range from 0~255.
15:12	/	/	/.
11:8	R/W	x	MONTH. Month. Range from 1~12.
7:5	/	/	/.
4:0	R/W	x	DAY. Day. Range from 1~31.

1.9.3.28. RTC HH-MM-SS REGISTER

Offset: 0x108			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
28:21	/	/	/.
20:16	R/W	x	HOUR. Range from 0~23
15:14	/	/	/.
13:8	R/W	x	MINUTE. Range from 0~59

Offset: 0x108			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
7:6	/	/	/.
5:0	R/W	x	SECOND. Range from 0~59

1.9.3.29. ALARM COUNTER DD-HH-MM-SS REGISTER

Offset: 0x10C			Register Name: DD_HH_MM_SS_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	x	DAY. Range from 0~255.
23:22	/	/	/
20:16	R/W	x	HOUR. Range from 0~23.
15:14	/	/	/.
13:8	R/W	x	MINUTE. Range from 0~59.
7:6	/	/	/.
5:0	R/W	x	SECOND. Range from 0~59.

1.9.3.30. ALARM WEEK HH-MM-SS REGISTER

Offset: 0x110			Register Name: ALARM_WK_HH_MM-SS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	x	HOUR. Range from 0~23.
15:14	/	/	/.
13:8	R/W	x	MINUTE.

Offset: 0x110			Register Name: ALARM_WK_HH_MM-SS
Bit	**Read/ Write**	**Default/Hex**	**Description**
			Range from 0~59.
7:6	/	/	/.
5:0	R/W	x	SECOND. Range from 0~59.

1.9.3.31. ALARM ENABLE REGISTER

Offset: 0x114			Register Name: ALARM_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:9	/	/	/.
8	R/W	0x0	ALM_CNT_EN. Alarm Counter Enable. If this bit is set to “1”, the Alarm Counter DD-HH-MM-SS register’s valid bits will down count to zero, and the the alarm pending bit will be set to “1”. 0:disable, 1:enable.
7	/	/	/
6	R/W	0x0	WK6_ALM_EN. Week 6(Sunday) Alarm Enable. 0: Disable, 1: Enable. If this bit is set to “1”, only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 6, the week 6 alarm irq pending bit will be set to “1”.
5	R/W	0x0	WK5_ALM_EN. Week 5(Saturday) Alarm Enable. 0: Disable, 1: Enable. If this bit is set to “1”, only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 5, the week 5 alarm irq pending bit will be set to “1”.
4	R/W	0x0	WK4_ALM_EN. Week 4(Friday) Alarm Enable. 0: Disable, 1: Enable.

Offset: 0x114			Register Name: ALARM_EN_REG
Bit	Read/ Write	Default/Hex	Description
			If this bit is set to "1", only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 4, the week 4 alarm irq pending bit will be set to "1".
3	R/W	0x0	WK3_ALM_EN. Week 3(Thursday) Alarm Enable. 0: Disable, 1: Enable. If this bit is set to "1", only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 3, the week 3 alarm irq pending bit will be set to "1".
2	R/W	0x0	WK2_ALM_EN. Week 2(Wednesday) Alarm Enable. 0: Disable, 1: Enable. If this bit is set to "1", only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 2, the week 2 alarm irq pending bit will be set to "1".
1	R/W	0x0	WK1_ALM_EN. Week 1(Tuesday) Alarm Enable. 0: Disable, 1: Enable. If this bit is set to "1", only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 1, the week 1 alarm irq pending bit will be set to "1".
0	R/W	0x0	WK0_ALM_EN. Week 0(Monday) Alarm Enable. 0: Disable, 1: Enable. If this bit is set to "1", only when the Alarm Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit[31:29] is 0, the week 0 alarm irq pending bit will be set to "1".

1.9.3.32. ALARM IRQ ENABLE REGISTER

Offset: 0x118	Register Name: ALARM_IRQ_EN

Bit	Read/ Write	Default/Hex	Description
31:2	/	/	/.
1	R/W	0x0	ALARM_WK_IRQ_EN. Alarm Week IRQ Enable. 0:disable, 1:enable.
0	R/W	0x0	ALARM_CNT_IRQ_EN. Alarm Counter IRQ Enable. 0:disable, 1:enable.

1.9.3.33. ALARM IRQ STATUS REGISTER

Offset: 0x11C			Register Name: ALARM_IRQ_STA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x0	WEEK_IRQ_PEND. Alarm Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect, 1: Pending, week counter value is reached. If alarm week irq enable is set to 1, the pending bit will be sent to the interrupt controller.
0	R/W	0x0	CNT_IRQ_PEND. Alarm Counter IRQ Pending bit. 0: No effect, 1: Pending, alarm counter value is reached. If alarm counter irq enable is set to 1, the pending bit will be sent to the interrupt controller.

1.9.3.34. TIMER GENERAL PURPOSE REGISTER

Offset: 0x120+N*0x4 (N=0~15)			Register Name: TMR_GP_DATA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	TMR_GP_DATA. Data[31:0].

Note: Timer general purpose register value can be stored if the RTCVDD is above 1.0V.

1.9.3.35. ALARM CONFIG REGISTER (DEFAULT: 0X00000000)

Offset:0x170			Register Name: ALARM_CONFIG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: disable alarm wake up output; 1: enable alarm wake up output.

1.10. High Speed Timer

1.10.1. Overview

The A20 supports four high speed timers, whose clock sources are fixed to AHBCLK.

1.10.2. High Speed Timer Register List

Module Name	Base Address
High Speed Timer	0x01C60000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x4	HS Timer Status Register
HS_TMR0_CTRL_REG	0x10	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x14	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x18	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x1C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x20	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x30	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x34	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x38	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x3C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x40	HS Timer 1 Current Value High Register
HS_TMR2_CTRL_REG	0x50	HS Timer 2 Control Register
HS_TMR2_INTV_LO_REG	0x54	HS Timer 2 Interval Value Low Register
HS_TMR2_INTV_HI_REG	0x58	HS Timer 2 Interval Value High Register
HS_TMR2_CURNT_LO_REG	0x5C	HS Timer 2 Current Value Low Register
HS_TMR2_CURNT_HI_REG	0x60	HS Timer 2 Current Value High Register
HS_TMR3_CTRL_REG	0x70	HS Timer 3 Control Register
HS_TMR3_INTV_LO_REG	0x74	HS Timer 3 Interval Value Low Register
HS_TMR3_INTV_HI_REG	0x78	HS Timer 3 Interval Value High Register
HS_TMR3_CURNT_LO_REG	0x7C	HS Timer 3 Current Value Low Register
HS_TMR3_CURNT_HI_REG	0x80	HS Timer 3 Current Value High Register

1.10.3. High Speed Timer Controller Register

1.10.3.1. HS TIMER IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x0			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	HS_TMR3_INT_EN. High Speed Timer 3 Interrupt Enable. 0: No effect; 1: High Speed Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	HS_TMR2_INT_EN. High Speed Timer 2 Interrupt Enable. 0: No effect; 1: High Speed Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	HS_TMR1_INT_EN. High Speed Timer 1 Interrupt Enable. 0: No effect; 1: High Speed Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	HS_TMR0_INT_EN. High Speed Timer 0 Interrupt Enable. 0: No effect; 1: High Speed Timer 0 Interval Value reached interrupt enable.

1.10.3.2. HS TIMER IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	HS_TMR3_IRQ_PEND. High Speed Timer 3 IRQ Pending. Set 1 to the bit will clear it.

Offset:0x4			Register Name: HS_TMR_IRQ_STAS_REG
Bit	Read/ Write	Default/Hex	Description
			0: No effect; 1: Pending, High speed timer 3 interval value is reached.
2	R/W	0x0	HS_TMR2_IRQ_PEND. High Speed Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 2 interval value is reached.
1	R/W	0x0	HS_TMR1_IRQ_PEND. High Speed Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 1 interval value is reached.
0	R/W	0x0	HS_TMR0_IRQ_PEND. High Speed Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 0 interval value is reached.

1.10.3.3. HS TIMER 0 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: HS_TMR0_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	/
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE. High Speed Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8

Offset:0x10			Register Name: HS_TMR0_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR0_RELOAD. High Speed Timer 0 Reload. 0: No effect, 1: Reload High Speed Timer 0 Interval Value.
0	R/W	0x0	HS_TMR0_EN. High Speed Timer 0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

1.10.3.4. HS TIMER 0 INTERVAL VALUE LO REGISTER

Offset:0x14			Register Name: HS_TMR0_INTV_LO_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	HS_TMR0_INTV_VALUE_LO. High Speed Timer 0 Interval Value [31:0].

1.10.3.5. HS TIMER 0 INTERVAL VALUE HI REGISTER

Offset:0x18	Register Name: HS_TMR0_INTV_HI_REG

Bit	Read/ Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	HS_TMR0_INTV_VALUE_HI. High Speed Timer 0 Interval Value [55:32].

Note: The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the Hi register should be written after the Lo register.

1.10.3.6. HS TIMER 0 CURRENT VALUE LO REGISTER

Offset:0x1C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	HS_TMR0_CUR_VALUE_LO. High Speed Timer 0 Current Value [31:0].

1.10.3.7. HS TIMER 0 CURRENT VALUE HI REGISTER

Offset:0x20			Register Name: HS_TMR0_CURNT_HI_REG
Bit	Read/ Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	HS_TMR0_CUR_VALUE_HI. High Speed Timer 0 Current Value [55:32].

Note:

1) HS timer 0 current value is a 56-bit down-counter (from interval value to 0);

2) The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or written first.

1.10.3.8. HS TIMER 1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name:HS_TMR1_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	/
30:8	/	/	/

Offset:0x30			Register Name:HS_TMR1_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
7	R/W	0x0	HS_TMR1_MODE. High Speed Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK_SRC. Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR1_RELOAD. High Speed Timer 1 Reload. 0: No effect, 1: Reload High Speed Timer 1 Interval Value.
0	R/W	0x0	HS_TMR1_EN. High Speed Timer 1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

1.10.3.9. HS TIMER 1 INTERVAL VALUE LO REGISTER

Offset:0x34			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR1_INTV_VALUE_LO. High Speed Timer 1 Interval Value [31:0].

1.10.3.10. HS TIMER 1 INTERVAL VALUE HI REGISTER

Offset:0x38			Register Name: HS_TMR1_INTV_HI_REG
Bit	Read/ Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	HS_TMR1_INTV_VALUE_HI. High Speed Timer 1 Interval Value [55:32].

Note: the interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the Hi register should be written after the Lo register.

1.10.3.11. HS TIMER 1 CURRENT VALUE LO REGISTER

Offset:0x3C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR1_CUR_VALUE_LO. High Speed Timer 1 Current Value [31:0].

1.10.3.12. HS TIMER 1 CURRENT VALUE HI REGISTER

Offset:0x40			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR1_CUR_VALUE_HI. High Speed Timer 1 Current Value [55:32].

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Note:

1) HS timer 1 current value is a 56-bit down-counter (from interval value to 0).

2) The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

1.10.3.13. HS TIMER 2 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x50			Register Name: HS_TMR2_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30:8	/	/	/
7	R/W	0x0	HS_TMR2_MODE. High Speed Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR2_RELOAD. High Speed Timer 2 Reload. 0: No effect, 1: Reload High Speed Timer 2 Interval Value.
0	R/W	0x0	HS_TMR2_EN. High Speed Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable

Offset:0x50			Register Name: HS_TMR2_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

1.10.3.14. HS TIMER 2 INTERVAL VALUE LO REGISTER

Offset:0x54			Register Name: HS_TMR2_INTV_LO_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR2_INTV_VALUE_LO. High Speed Timer 2 Interval Value [31:0].

1.10.3.15. HS TIMER 2 INTERVAL VALUE HI REGISTER

Offset:0x58			Register Name: HS_TMR2_INTV_HI_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR2_INTV_VALUE_HI. High Speed Timer 2 Interval Value [55:32].

Note: the interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the Hi register should be written after the Lo register.

1.10.3.16. HS TIMER 2 CURRENT VALUE LO REGISTER

Offset: 0x5C			Register Name: HS_TMR2_CURNT_LO_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	x	HS_TMR2_CUR_VALUE_LO. High Speed Timer 2 Current Value [31:0].

1.10.3.17. HS TIMER 2 CURRENT VALUE HI REGISTER

Offset: 0x60			Register Name: HS_TMR2_CURNT_HI_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR2_CUR_VALUE_HI. High Speed Timer 2 Current Value [55:32].

Note:

1) High speed timer 2 current value is a 56-bit down-counter (from interval value to 0);

2) The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or written first.

1.10.3.18. HS TIMER 3 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x70			Register Name:HS_TMR3_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30:8	/	/	/
7	R/W	0x0	HS_TMR3_MODE. High Speed Timer 3 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR3_CLK_SRC. Select the pre-scale of the high speed timer 3 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR3_RELOAD.

Offset: 0x70			Register Name:HS_TMR3_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			High Speed Timer 3 Reload. 0: No effect, 1: Reload High Speed Timer 3 Interval Value.
0	R/W	0x0	HS_TMR3_EN. High Speed Timer 3 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

1.10.3.19. HS TIMER 3 INTERVAL VALUE LO REGISTER

Offset: 0x74			Register Name: HS_TMR3_INTV_LO_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	x	HS_TMR3_INTV_VALUE_LO. High Speed Timer 3 Interval Value [31:0].

1.10.3.20. HS TIMER 3 INTERVAL VALUE HI REGISTER

Offset: 0x78			Register Name: HS_TMR3_INTV_HI_REG
Bit	Read/ Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	HS_TMR3_INTV_VALUE_HI. High Speed Timer 3 Interval Value [55:32].

Note: the interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the Hi register should be written after the Lo register.

1.10.3.21. HS TIMER 3 CURRENT VALUE LO REGISTER

Offset: 0x7C			Register Name: HS_TMR3_CURNT_LO_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR3_CUR_VALUE_LO. High Speed Timer 3 Current Value [31:0].

1.10.3.22. HS TIMER 3 CURRENT VALUE HI REGISTER

Offset: 0x80			Register Name: HS_TMR3_CURNT_HI_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR3_CUR_VALUE_HI. High Speed Timer 3 Current Value [55:32].

Note:

1) High speed timer 1 current value is a 56-bit down-counter (from interval value to 0).

2) The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

1.11. GIC

For details about GIC, please refer to the GIC PL400 technical reference manual and ARM GIC Architecture Specification V2.0.

1.11.1. Interrupt Source

Interrupt Source	SRC	Vector	FIQ	Description
SGI 0	0			SGI 0 interrupt
SGI 1	1			SGI 1 interrupt
SGI 2	2			SGI 2 interrupt
SGI 3	3			SGI 3 interrupt
SGI 4	4			SGI 4 interrupt
SGI 5	5			SGI 5 interrupt
SGI 6	6			SGI 6 interrupt
SGI 7	7			SGI 7 interrupt
SGI 8	8			SGI 8 interrupt
SGI 9	9			SGI 9 interrupt
SGI 10	10			SGI 10 interrupt
SGI 11	11			SGI 11 interrupt
SGI 12	12			SGI 12 interrupt
SGI 13	13			SGI 13 interrupt
SGI 14	14			SGI 14 interrupt
SGI 15	15			SGI 15 interrupt
PPI 0	16			PPI 0 interrupt
PPI 1	17			PPI 1 interrupt
PPI 2	18			PPI 2 interrupt
PPI 3	19			PPI 3 interrupt
PPI 4	20			PPI 4 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
PPI 5	21			PPI 5 interrupt
PPI 6	22			PPI 6 interrupt
PPI 7	23			PPI 7 interrupt
PPI 8	24			PPI 8 interrupt
PPI 9	25			PPI 9 interrupt
PPI 10	26			PPI 10 interrupt
PPI 11	27			PPI 11 interrupt
PPI 12	28			PPI 12 interrupt
PPI 13	29			PPI 13 interrupt
PPI 14	30			PPI 14 interrupt
PPI 15	31			PPI 15 interrupt
NMI	32			NMI interrupt.
UART 0	33			UART 0 interrupt
UART 1	34			UART 1 interrupt
UART 2	35			UART 2 interrupt
UART 3	36			UART 3 interrupt
IR 0	37			IR 0 interrupt
IR 1	38			IR 1 interrupt
TWI 0	39			TWI 0 interrupt
TWI 1	40			TWI 1 interrupt
TWI 2	41			TWI 2 interrupt
SPI 0	42			SPI 0 interrupt
SPI 1	43			SPI 1 interrupt
SPI 2	44			SPI 2 interrupt
SPDIF	45			SPDIF interrupt
AC97	46			AC97 interrupt
TS	47			TS interrupt
IIS0	48			Digital Audio Controller 0 interrupt
UART 4	49			UART 4 interrupt
UART 5	50			UART 5 interrupt
UART 6	51			UART 6 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
UART 7	52			UART 7 interrupt
Keypad	53			Keypad interrupt.
Timer 0	54			Timer 0 interrupt
Timer 1	55			Timer 1interrupt
Timer 2/Alarm/WD	56			Timer 2 , Alarm, Watchdog interrupt
Timer 3	57			Timer 3 interrupt.
CAN	58			CAN interrupt.
DMA	59			DMA interrupt
PIO	60			PIO interrupt
Touch Panel.	61			Touch Panel interrupt.
Audio Codec	62			Audio Codec interrupt
LRADC	63			LRADC interrupt
SD/MMC 0	64			SD/MMC Host Controller 0 interrupt
SD/MMC 1	65			SD/MMC Host Controller 1 interrupt
SD/MMC 2	66			SD/MMC Host Controller 2 interrupt
SD/MMC 3	67			SD/MMC Host Controller 3 interrupt
MS	68			Memory Stick Host Controller interrupt
NAND	69			NAND Flash Controller (NFC) interrupt
USB 0	70			USB 0 interrupt
USB 1	71			USB 1 interrupt
USB 2	72			USB 2 interrupt
SCR	73			SCR interrupt.
CSI 0	74			CSI 0 interrupt
CSI 1	75			CSI 1 interrupt
LCD Controller 0	76			LCD Controller 0 interrupt
LCD Controller 1	77			LCD Controller 1 interrupt
MP	78			MP interrupt.
DE-FE0/DE-BE0	79			DE-FE0/DE-BE0 interrupt
DE-FE1/DE-BE1	80			DE-FE1/DE-BE1 interrupt
PMU	81			PMU interrupt
SPI3	82			SPI3 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
	83			
	84			
VE	85			VE interrupt
SS	86			Security System interrupt.
EMAC	87			EMAC interrupt
SATA	88			SATA interrupt
	89			
HDMI 0	90			HDMI 0 interrupt
TVE 0/1	91			TV encoder 0/1 interrupt
ACE	92			ACE interrupt
TVD	93			TV decoder interrupt
PS2-0	94			PS2-0 interrupt
PS2-1	95			PS2-1 interrupt
USB 3	96			USB 3 wakeup, connect, disconnect interrupt
USB 4	97			USB 4 wakeup, connect, disconnect interrupt
PLE/PERFMU	98			PLE on non-secure transfers interrupt PLE on secure transfer interrupt PLE error interrupt Performance monitor interrupt
Timer 4	99			Timer 4 interrupt
Timer 5	100			Timer 5 interrupt
GPU-GP	101			GPU-GP interrupt
GPU-GPMMU	102			GPU-GPMMU interrupt
GPU-PP0	103			GPU-PP0 interrupt
GPU-PPMMU0	104			GPU-PPMMU0 interrupt
GPU-PMU	105			GPU-PMU interrupt
GPU-PP1	106			GPU-PP1 interrupt
GPU-PPMMU1	107			GPU-PPMMU1 interrupt
GPU-RSV0	108			
GPU-RSV1	109			
GPU-RSV2	110			
GPU-RSV3	111			

Interrupt Source	SRC	Vector	FIQ	Description
GPU-RSV4	112			
HS Timer 0	113			HS Timer 0 interrupt
HS Timer 1	114			HS Timer 1 interrupt
HS Timer 2	115			HS Timer 2 interrupt
HS Timer 3	116			HS Timer 3 interrupt
GMAC	117			GMAC interrupt
HDMI 1	118			HDMI 1 interrupt
IIS1	119			Digital Audio Controller 1 interrupt
TWI 3	120			TWI 3 interrupt
TWI 4	121			TWI 4 interrupt
IIS 2	122			Digital Audio Controller 2 interrupt

1.12. DMA

1.12.1. Overview

There are two kinds of DMA in the chip. One is Normal DMA with 8 channels, the other is Dedicated DMA with 8 channels .

For normal DMA, only one channel can be active and the sequence is in line with the priority level. While for the dedicated DMA, at most 8-channel can be active at the same time if their source or destination has no conflict. The dedicated DMA can only transfer data between the DRAM and the module.

DMA can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned.

Although the increase mode of NDMA should be address aligned, but its byte counter should not be multiple.

The DMA Source Address, Destination Address, Byte Counter Registers can be modified even if the DMA is started.

1.12.2. DMA Register List

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_IRQ_EN_REG	0x0	DMA IRQ Enable
DMA_IRQ_PEND_STA_REG	0x4	DMA IRQ Pending Status
NDMA_AUTO_GAT_REG	0x8	NDMA Auto Gating
NDMA_CTRL_REG	0x100+N*0x20	Normal DMA Configuration (N=0,1,2,3,4,5,6,7)
NDMA_SRC_ADDR_REG	0x100+N*0x20+0x4	Normal DMA Source Address (N=0,1,2,3,4,5,6,7)
NDMA_DEST_ADDR_REG	0x100+N*0x20+0x8	Normal DMA Destination Address (N=0,1,2,3,4,5,6,7)
NDMA_BC_REG	0x100+N*0x20+0xC	Normal DMA Byte Counter (N=0,1,2,3,4,5,6,7)
DDMA_CFG_REG	0x300+N*0x20	Dedicated DMA Configuration (N=0,1,2,3,4,5,6,7)
DDMA_SRC_START_ADDR_REG	0x300+N*0x20+0x4	Dedicated DMA Source Start Address (N=0,1,2,3,4,5,6,7)
DDMA_DEST_START_ADDR_REG	0x300+N*0x20+0x8	Dedicated DMA Destination Start Address (N=0,1,2,3,4,5,6,7)
DDMA_BC_REG	0x300+N*0x20+0xC	Dedicated DMA Byte Counter (N=0,1,2,3,4,5,6,7)
DDMA_PARA_REG	0x300+N*0x20+0x18	Dedicated DMA Parameter (N=0,1,2,3,4,5,6,7)

1.12.3. DMA Controller Register Description

1.12.3.1. DMA IRQ ENABLE REGISTER(DEFAULT: 0X00000000)

Offset: 0x0			Register Name: DMA_IRQ_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDMA7_END_IRQ_EN. Dedicated DMA 7 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
30	R/W	0x0	DDMA7_HF_IRQ_EN. Dedicated DMA 7 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
29	R/W	0x0	DDMA6_END_IRQ_EN. Dedicated DMA 6 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
28	R/W	0x0	DDMA6_HF_IRQ_EN. Dedicated DMA 6 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
27	R/W	0x0	DDMA5_END_IRQ_EN. Dedicated DMA 5 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
26	R/W	0x0	DDMA5_HF_IRQ_EN Dedicated DMA 5 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
25	R/W	0x0	DDMA4_END_IRQ_EN Dedicated DMA 4 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
24	R/W	0x0	DDMA4_HF_IRQ_EN Dedicated DMA 4 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
23	R/W	0x0	DDMA3_END_IRQ_EN Dedicated DMA 3 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
22	R/W	0x0	DDMA3_HF_IRQ_EN Dedicated DMA 3 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.

Offset: 0x0			Register Name: DMA_IRQ_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
21	R/W	0x0	DDMA2_END_IRQ_EN Dedicated DMA 2 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
20	R/W	0x0	DDMA2_HF_IRQ_EN Dedicated DMA 2 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
19	R/W	0x0	DDMA1_END_IRQ_EN Dedicated DMA 1 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
18	R/W	0x0	DDMA1_HF_IRQ_EN Dedicated DMA 1 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
17	R/W	0x0	DDMA0_END_IRQ_EN Dedicated DMA 0 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
16	R/W	0x0	DDMA0_HF_IRQ_EN Dedicated DMA 0 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
15	R/W	0x0	NDMA7_END_IRQ_EN. Normal DMA 7 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
14	R/W	0x0	NDMA7_HF_IRQ_EN Normal DMA 7 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
13	R/W	0x0	NDMA6_END_IRQ_EN Normal DMA 6 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
12	R/W	0x0	NDMA6_HF_IRQ_EN Normal DMA 6 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
11	R/W	0x0	NDMA5_END_IRQ_EN Normal DMA 5 End Transfer Interrupt Enable. 0: Disable, 1: Enable.

Offset: 0x0			Register Name: DMA_IRQ_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
10	R/W	0x0	NDMA5_HF_IRQ_EN Normal DMA 5 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
9	R/W	0x0	NDMA4_END_IRQ_EN Normal DMA 4 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
8	R/W	0x0	NDMA4_HF_IRQ_EN Normal DMA 4 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
7	R/W	0x0	NDMA3_END_IRQ_EN Normal DMA 3 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
6	R/W	0x0	NDMA3_HF_IRQ_EN Normal DMA 3 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
5	R/W	0x0	NDMA2_END_IRQ_EN Normal DMA 2 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
4	R/W	0x0	NDMA2_HF_IRQ_EN Normal DMA 2 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
3	R/W	0x0	NDMA1_END_IRQ_EN Normal DMA 1 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
2	R/W	0x0	NDMA1_HF_IRQ_EN Normal DMA 1 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	NDMA0_END_IRQ_EN Normal DMA 0 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	NDMA0_HF_IRQ_EN Normal DMA 0 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.

1.12.3.2. DMA IRQ PENDING STATUS REGISTER(DEFAULT: 0X00000000)

Offset: 0x4			Register Name: DMA_IRQ_PEND_STA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDMA7_END_IRQ_PEND. Dedicated DMA 7 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
30	R/W	0x0	DDMA7_HF_IRQ_PEND Dedicated DMA 7 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
29	R/W	0x0	DDMA6_END_IRQ_PEND Dedicated DMA 6 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
28	R/W	0x0	DDMA6_HF_IRQ_PEND Dedicated DMA 6 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
27	R/W	0x0	DDMA5_END_IRQ_PEND Dedicated DMA 5 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
26	R/W	0x0	DDMA5_HF_IRQ_PEND Dedicated DMA 5 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
25	R/W	0x0	DDMA4_END_IRQ_PEND Dedicated DMA 4 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
24	R/W	0x0	DDMA4_HF_IRQ_PEND Dedicated DMA 4 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
23	R/W	0x0	DDMA3_END_IRQ_PEND

Offset: 0x4			Register Name: DMA_IRQ_PEND_STA_REG
Bit	Read/ Write	Default/Hex	Description
			Dedicated DMA 3 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
22	R/W	0x0	DDMA3_HF_IRQ_PEND Dedicated DMA 3 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
21	R/W	0x0	DDMA2_END_IRQ_PEND Dedicated DMA 2 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
20	R/W	0x0	DDMA2_HF_IRQ_PEND Dedicated DMA 2 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
19	R/W	0x0	DDMA1_END_IRQ_PEND Dedicated DMA 1 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
18	R/W	0x0	DDMA1_HF_IRQ_PEND Dedicated DMA 1 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
17	R/W	0x0	DDMA0_END_IRQ_PEND Dedicated DMA 0 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
16	R/W	0x0	DDMA0_HF_IRQ_PEND Dedicated DMA 0 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
15	R/W	0x0	NDMA7_END_IRQ_PEND. Normal DMA 7 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
14	R/W	0x0	NDMA7_HF_IRQ_PEND. Normal DMA 7 Half Transfer Interrupt Pending. Set 1 to the bit

Offset: 0x4			Register Name: DMA_IRQ_PEND_STA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			will clear it. 0: No effect, 1: Pending.
13	R/W	0x0	NDMA6_END_IRQ_PEND. Normal DMA 6 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
12	R/W	0x0	NDMA6_HF_IRQ_PEND. Normal DMA 6 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
11	R/W	0x0	NDMA5_END_IRQ_PEND. Normal DMA 5 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
10	R/W	0x0	NDMA5_HF_IRQ_PEND. Normal DMA 5 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
9	R/W	0x0	NDMA4_END_IRQ_PEND. Normal DMA 4 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
8	R/W	0x0	NDMA4_HF_IRQ_PEND. Normal DMA 4 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
7	R/W	0x0	NDMA3_END_IRQ_PEND. Normal DMA 3 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
6	R/W	0x0	NDMA3_HF_IRQ_PEND. Normal DMA 3 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
5	R/W	0x0	NDMA2_END_IRQ_PEND. Normal DMA 2 End Transfer Interrupt Pending. Set 1 to the bit

Offset: 0x4			Register Name: DMA_IRQ_PEND_STA_REG
Bit	Read/ Write	Default/Hex	Description
			will clear it. 0: No effect, 1: Pending.
4	R/W	0x0	NDMA2_HF_IRQ_PEND. Normal DMA 2 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
3	R/W	0x0	NDMA1_END_IRQ_PEND. Normal DMA 1 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
2	R/W	0x0	NDMA1_HF_IRQ_PEND. Normal DMA 1 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W	0x0	NDMA0_END_IRQ_PEND. Normal DMA 0 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W	0x0	NDMA0_HF_IRQ_PEND. Normal DMA 0 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

1.12.3.3. NDMA AUTO GATING REGISTER(DEFAULT: 0X00000000)

Offset: 0x8			Register Name: NDMA_AUTO_GAT_REG Default Value: 0x0000_0000
Bit	Read/ Write	Default/Hex	Description
31:17	/	/	/.
16	R/W	0x0	NDMA Auto Clock Gating bit 0: NDMA auto clock gating enable 1: NDMA auto clock gating disable If NDMA works in Continuous mode, this bit should be set to 1.

Offset: 0x8			Register Name: NDMA_AUTO_GAT_REG Default Value: 0x0000_0000
Bit	**Read/ Write**	**Default/Hex**	**Description**
15:0	/	/	/.

1.12.3.4. NORMAL DMA CONFIGURATION REGISTER(DEFAULT: 0X00000000)

Offset: 0x100+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	R/W	0x0	DMA_LOADING. DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to the bit will reset the corresponding DMA channel.
30	R/W	0x0	DMA_CONTI_MODE_EN. DMA Continuous Mode Enable. 0: Disable, 1: Enable.
29:27	R/W	0x0	DMA_WAIT_STATE. DMA Wait State. 0: wait for 0 DMA clock to request, … 7: wait for $2^{(n+1)}$ DMA clock to request.
26:25	R/W	0x0	NDMA_DEST_DATA_WIDTH. Normal DMA Destination Data Width. 00: 8-bit 01: / 10: 32-bit 11: /
24:23	R/W	0x0	DMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1 01: /

Offset: 0x100+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			10: 8 11: /
22	R/W	0x0	DMA_DEST_SEC. DMA Destination Security 0: secure, 1: non-secure.
21	R/W	0x0	NDMA_DEST_ADDR_TYPE. Normal DMA Destination Address Type. 0: Increment 1: No Change.
20:16	R/W	0x0	NDMA_DEST_DRQ_TYPE. Normal DMA Destination DRQ Type. 00000 : IR0-TX 00001 : IR1-TX 00010 : SPDIF-TX 00011 : IIS0-TX 00100 : IIS1-TX 00101 : AC97-TX 00110 : IIS2-TX 00111 : 01000 : UART0 TX 01001 : UART1 TX 01010 : UART2 TX 01011 : UART3 TX 01100 : UART4 TX 01101 : UART5 TX 01110 : UART6 TX 01111 : UART7 TX 10000 : HDMI DDC TX 10001 : USB EP1 10010 : / 10011 : Audio Codec D/A 10100 : / 10101 : SRAM(range :) 10110 : SDRAM

Offset: 0x100+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			10111 : / 11000 : SPI0 TX 11001 : SPI1 TX 11010 : SPI2 TX 11011 : SPI3 TX 11100 : USB EP2 11101 : USB EP3 11110 : USB EP4 11111 : USB EP5
15	R/W	0x0	BC_MODE_SEL. BC mode select. 0 : normal mode(the value read back is equal to the value that is written) 1 : remain mode(the value read back is equal to the remain counter to be transfered).
14:11	/	/	/.
10:9	R/W	0x0	NDMA_SRC_DATA_WIDTH. Normal DMA Source Data Width. 00: 8-bit 01: / 10: 32-bit 11: /
8:7	R/W	0x0	DMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: / 10: 8 11: /.
6	R/W	0x0	DMA_SRC_SEC. DMA Source Security. 0 : secure, 1 : non-secure.
5	R/W	0x0	NDMA_SRC_ADDR_TYPE. Normal DMA Source Address Type.

Offset: 0x100+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			0: Increment 1: No Change
4:0	R/W	0x0	NDMA_SRC_DRQ_TYPE. Normal DMA Source DRQ Type. 00000 : IR0-RX 00001 : IR1-RX 00010 : SPDIF-RX 00011 : IIS0-RX 00100 : IIS1-RX 00101 : AC97-RX 00110 : IIS2-RX 00111 : / 01000 : UART0 RX 01001 : UART1 RX 01010 : UART2 RX 01011 : UART3 RX 01100 : UART4 RX 01101 : UART5 RX 01110 : UART6 RX 01111 : UART7 RX 10000 : HDMI DDC RX 10001 : USB EP1 10010 : / 10011 : Audio Codec A/D 10100 : / 10101 : SRAM(range :) 10110 : SDRAM 10111 : TP A/D 11000 : SPI0 RX 11001 : SPI1 RX 11010 : SPI2 RX 11011 : SPI3 RX 11100 : USB EP2 11101 : USB EP3 11110 : USB EP4 11111 : USB EP5

1.12.3.5. NORMAL DMA SOURCE ADDRESS REGISTER(DEFAULT: 0X00000000)

Offset: 0x100+N*0x20+0x4 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_SRC_ADDR_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDMA_SRC_ADDR. Normal DMA Source Address.

1.12.3.6. NORMAL DMA DESTINATION ADDRESS REGISTER(DEFAULT: 0X00000000)

Offset: 0x100+N*0x20+0x8 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_DEST_ADDR_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDMA_DEST_ADDR. Normal DMA Destination Address.

1.12.3.7. NORMAL DMA BYTE COUNTER REGISTER(DEFAULT: 0X00000000)

Offset: 0x100+N*0x20+0xC (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_BC_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:18	/	/	/.
17:0	R/W	0x0	NDMA_BC. Normal DMA Byte Counter.

Note: If ByteCounter=0, DMA will transfer no byte. The maximum value is 128k.

1.12.3.8. DEDICATED DMA CONFIGURATION REGISTER(DEFAULT: 0X00000000)

Offset: 0x300+N*0x20 (N=0,1,2,3,4,5,6,7)	Register Name: DDMA_CFG_REG

Bit	Read /Write	Default/Hex	Description
31	R/W	0x0	DMA_LOADING. DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to the bit will stop the corresponding DMA channel and reset its state machine.
30	R	0x0	DMA_BSY_STA. DMA Busy Status. 0: DMA idle, 1: DMA busy.
29	R/W	0x0	DMA_CONT_MODE_EN. DMA Continuous Mode Enable. 0: Disable, 1: Enable.
28	R/W	0x0	DMA_DEST_SEC. DMA Destination Security. 0: secure, 1: non-secure
27	/	/	/.
26:25	R/W	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: / 10: 32-bit 11: /
24:23	R/W	0x0	DMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1 01: / 10: 8 11: /.
22:21	R/W	0x0	DMA_ADDR_MODE. DMA Destination Address Mode DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: Horizontal Page Mode 0x3: Vertical Page Mode
20:16	R/W	0x0	DDMA_DEST_DRQ_TYPE.

Offset: 0x300+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_CFG_REG
Bit	**Read /Write**	**Default/Hex**	**Description**
			Dedicated DMA Destination DRQ Type 0x0: SRAM memory 0x1: SDRAM memory 0x2: 0x3: NAND Flash Controller (NFC) 0x4: USB0 0x5: / 0x6: Ethernet MAC Tx 0x7: / 0x8: SPI1 TX 0x9: / 0xA: Security System Tx 0xB: / 0xC: / 0xD: / 0xE: TCON0 0xF: TCON1 0x10: / 0x11: / 0x12: / 0x13: / 0x14: / 0x15: / 0x16: / 0x17: Memory Stick Controller (MSC) 0x18: HDMI Audio 0x19: / 0x1A: SPI0 TX 0x1B: / 0x1C: SPI2 TX 0x1D: / 0x1E: SPI3 TX 0x1F: /
15	R/W	0x0	BC_MODE_SEL. BC mode select. 0 : normal mode(the value read back is equal to the value that is written) 1 : remain mode(the value read back is equal to the remain counter to be transfered).

Offset: 0x300+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_CFG_REG
Bit	**Read /Write**	**Default/Hex**	**Description**
14:13	/	/	/.
12	R/W	0x0	DMA_SRC_SEC. DMA Source Security. 0: secure, 1: non-secure.
11	/	/	/
10:9	R/W	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: / 10: 32-bit 11: /
8:7	R/W	0x0	DMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: / 10: 8 11: /..
6:5	R/W	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: Horizontal Page Mode 0x3: Vertical Page Mode
4:0	R/W	0x0	DDMA_SRC_DRQ_TYPE. Dedicated DMA Source DRQ Type 0x0: SRAM memory 0x1: SDRAM memory 0x2: 0x3: NAND Flash Controller (NFC) 0x4: USB0 0x5: / 0x6: / 0x7: Ethernet MAC Rx 0x8: / 0x9: SPI1 RX

Offset: 0x300+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_CFG_REG
Bit	**Read /Write**	**Default/Hex**	**Description**
			0xA: / 0xB: Security System Rx 0xC: / 0xD: / 0xE: / 0xF: / 0x10: / 0x11: / 0x12: / 0x13: / 0x14: / 0x15: / 0x16: / 0x17: Memory Stick Controller (MSC) 0x18: / 0x19: / 0x1A: / 0x1B: SPI0 RX. 0x1C: / 0x1D: SPI2 RX 0x1E: / 0x1F: SPI3 RX

1.12.3.9. DEDICATED DMA SOURCE START ADDRESS REGISTER

Offset: 0x300+N*0x20+0x4 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_SRC_START_ADDR_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	DDMA_SRC_START_ADDR. Dedicated DMA Source Start Address.

1.12.3.10. DEDICATED DMA DESTINATION START ADDRESS REGISTER

Offset: 0x300+N*0x20+0x8 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_DEST_START_ADDR_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	x	DDMA_DEST_START_ADDR. Dedicated DMA Destination Start Address.

1.12.3.11. DEDICATED DMA BYTE COUNTER REGISTER

Offset: 0x300+N*0x20+0xC (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_BC_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:25	/	/	/.
24:0	R/W	x	DDMA_BC. Dedicated DMA Byte Counter.

Note: If ByteCounter=0, DMA will transfer no byte. The maximum value is 16M.

1.12.3.12. DEDICATED DMA PARAMETER REGISTER

Offset: 0x300+N*0x20+0x18 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_PARA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	DEST_DATA_BLK_SIZE. Destination Data Block Size n.
23:16	R/W	0x0	DEST_WAIT_CYC. Destination Wait Clock Cycles n
15:8	R/W	0x0	SRC_DATA_BLK_SIZE. Source Data Block Size n.
7:0	R/W	0x0	SRC_WAIT_CYC. Source Wait Clock Cycles n.

Note: If the counter=N, the value is N+1.

1.13. Audio Codec

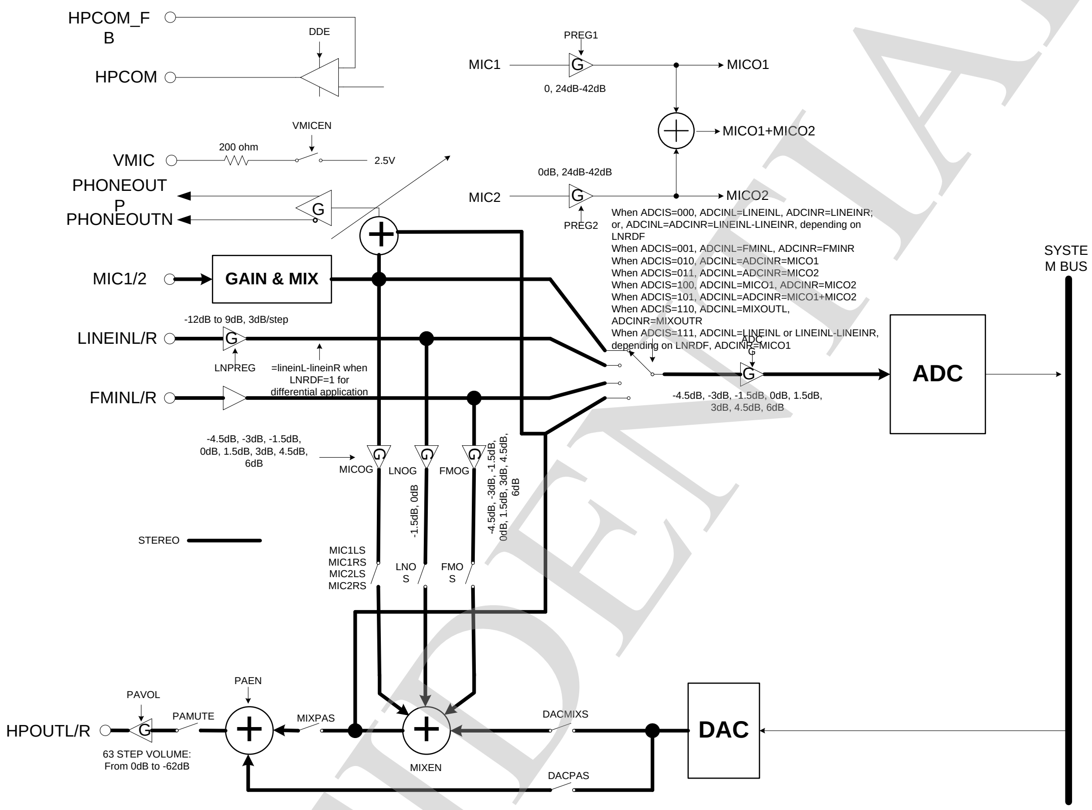
1.13.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplifier.

It features:

- On-chip 24-bit DAC for playback
- On-chip 24-bit ADC for recorder
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- Support 192K and 96K sample
- Support FM/ Line-in/ Microphone recorder
- Stereo headphone amplifier that can be operated in capless headphone mode
- Support Virtual Ground to automatic change to True Ground to protect headphone amplifier and make function work normal mode

1.13.2. Audio Codec Block Diagram



1.13.3. Audio Codec Register List

Module Name	Base Address
AC	0x01C22C00

Register Name	Offset	Description
AC_DAC_DPC	0x00	DAC Digital Part Control Register
AC_DAC_FIFOC	0x04	DAC FIFO Control Register

Register Name	Offset	Description
AC_DAC_FIFOS	0x08	DAC FIFO Status Register
AC_DAC_TXDATA	0x0C	DAC TX Data Register
AC_DAC_ACTL	0x10	DAC Analog Control Register
AC_DAC_TUNE	0x14	DAC/ ADC Performance Tuning Register
AC_ADC_FIFOC	0x1C	ADC FIFO Control Register
AC_ADC_FIFOS	0x20	ADC FIFO Status Register
AC_ADC_RXDATA	0x24	ADC RX Data Register
AC_ADC_ACTL	0x28	ADC Analog Control Register
AC_DAC_CNT	0x30	DAC TX FIFO Counter Register
AC_ADC_CNT	0x34	ADC RX FIFO Counter Register
AC_SYS_VERI	0x38	System Calibration Verify Register
AC_MIC_PHONE_CAL	0x3c	MIC gain & Phone out Control Register

1.13.4. Audio Codec Register Description

1.13.4.1. DAC DIGITAL PART CONTROL REGISTER

Offset: 0x00			**Register Name: AC_DAC_DPC**
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0x0	EN_DA. DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU. Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA. DWA Function Disable

Offset: 0x00			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default**	**Description**
			0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN. High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL. Digital volume control: dvc, ATT=(DVC[5:0]-2)*(-1.16dB) 62 steps, -1.16dB/step
11:0	/	/	/

1.13.4.2. DAC FIFO CONTROL REGISTER

Offset: 0x4			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default**	**Description**
31:29	R/W	0x0	DAC_FS. Sample Rate of DAC 000: 48KHz 010: 24KHz 100: 12KHz 110: 192KHz 001: 32KHz 011: 16KHz 101: 8KHz 111: 96KHz 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT.

Offset: 0x4			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default**	**Description**
			Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE. For 24-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:8]} 01/11: Reserved For 16-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 01/11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT. When TX FIFO available room less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: IRQ/DRQ Deasserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x10	TX_TRIG_LEVEL. TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL≤TXTL Notes: WLEVEL represents the number of valid samples in the TX FIFO
7	R/W	0x0	ADDA_LOOP_EN. ADDA loop Enable, adda 0: Disable 1: Enable
6	R/W	0x0	DAC_MONO_EN. DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data
5	R/W	0x0	TX_SAMPLE_BITS.

Offset: 0x4			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default	Description
			Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN. DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN. DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN. DAC FIFO Under Run IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN. DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_FLUSH. DAC FIFO Flush Write ‘1’ to flush TX FIFO, self clear to ‘0’

1.13.4.3. DAC FIFO STATUS REGISTER

Offset: 0x8			Register Name: AC_DAC_FIFOS
Bit	Read/Write	Default	Description
31:24	/	/	/
23	R	0x1	TX_EMPTY. TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT.

Offset: 0x8			Register Name: AC_DAC_FIFOS
Bit	**Read/Write**	**Default**	**Description**
			TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W	0x1	TXE_INT. TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	R/W	0x0	TXU_INT. TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/W	0x0	TXO_INT. TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

1.13.4.4. DAC TX DATA REGISTER

Offset: 0xC			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0x0	TX_DATA. Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

1.13.4.5. DAC ANALOG CONTROL REGISTER

Offset:0x10			Register Name: AC_DAC_ACTRL
Bit	**R/W**	**Default**	**Description**

Offset:0x10			Register Name: AC_DAC_ACTRL
Bit	**R/W**	**Default**	**Description**
31	R/W	0x0	DACAREN. Internal DAC Analog Right channel Enable 0:Disable 1:Enable
30	R/W	0x0	DACALEN. Internal DAC Analog Left channel Enable 0:Disable 1:Enable
29	R/W	0x0	MIXEN. Analog Output Mixer Enable 0:Disable 1:Enable
28:27	/	/	/
26	R/W	0x1	LNG. Line-in gain stage to output mixer Gain Control 0: -1.5dB 1: 0dB
25:23	R/W	0x3	FMG. FM Input to output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
22:20	R/W	0x3	MICG. MIC1/2 gain stage to output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
19	R/W	0x0	LLNS. Left LINEIN gain stage to left output mixer mute 0-mute; 1-Not mute When LNRDF is 0, left select LINEINL When LNRDF is 1, left select LINEINL-LINEINR
18	R/W	0x0	RLNS. Right LINEIN gain stage to right output mixer mute 0-mute; 1-Not mute When LNRDF is 0, right select LINEINR When LNRDF is 1, right select LINEINL-LINEINR
17	R/W	0x0	LFMS. Left FM to left output mixer mute

Offset:0x10			Register Name: AC_DAC_ACTRL
Bit	**R/W**	**Default**	**Description**
			0:mute 1:Not mute
16	R/W	0x0	RFMS. right FM to right output mixer mute 0:mute 1:Not mute
15	R/W	0x0	LDACLMIXS. Left DAC to left output mixer Mute 0:Mute 1:Not mute
14	R/W	0x0	RDACRMIXS. Right DAC to right output mixer Mute 0:Mute 1:Not mute
13	R/W	0x0	LDACRMIXS. Left DAC to right output mixer Mute, 0:Mute 1:Not mute
12	R/W	0x0	MIC1LS. MIC1 to output mixer left channel mute 0: mute 1: Not mute
11	R/W	0x0	MIC1RS. MIC1 to output mixer right channel mute 0: mute 1: Not mute
10	R/W	0x0	MIC2LS. MIC2 to output mixer left channel mute 0: mute 1: Not mute
9	R/W	0x0	MIC2RS. MIC2 to output mixer right channel mute 0: mute 1: Not mute
8	R/W	0x0	DACPAS.

Offset:0x10			Register Name: AC_DAC_ACTRL
Bit	R/W	Default	Description
			DAC to PA Mute 0-Mute 1-Not mute
7	R/W	0x0	MIXPAS. Output Mixer to PA mute 0: Mute 1: Not mute
6	R/W	0x0	PAMUTE. All input source to PA mute, including Output mixer and Internal DAC, (): 0:Mute 1: Not mute
5:0	R/W	0x0	PAVOL. PA Volume Control, (PAVOL): Total 64 level, from 0dB to -62dB, 1dB/step,mute when 000000

1.13.4.6. DAC/ADC ANALOG PERFORMANCE TUNING REGISTER

Offset:0x14			Register Name: AC_ADDA_BIAS_CTRL
Bit	R/W	Default	Description
31:0	/	/	/

1.13.4.7. ADC FIFO CONTROL REGISTER

Offset: 0x1C			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default	Description
31:29	R/W	0x0	ADFS. Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz

Offset: 0x1C			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default**	**Description**
			011: 16KHz 101: 8KHz 111: Reserved
28	R/W	0x0	EN_AD. ADC Digital Part Enable, en_ad 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE. RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:13	/	/	/
12:8	R/W	0xF	RX_FIFO_TRG_LEVEL. RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for TX FIFO normal condition IRQ/DRQ Generated when WLEVEL 」ｔ RXTL[4:0] **Notes:** WLEVEL represents the number of valid samples in the RX FIFO
7	R/W	0x0	ADC_MONO_EN. ADC Mono Enable. 0: Stereo, 16 levels FIFO 1: mono, 32 levels FIFO When set to '1', Only left channel samples are recorded
6	R/W	0x0	RX_SAMPLE_BITS. Receiving Audio Sample Resolution 0: 16 bits

Offset: 0x1C			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default**	**Description**
			1: 24 bits
5	/	/	/
4	R/W	0x0	ADC_DRQ_EN. ADC FIFO Data Available DRQ Enable. 0: Disable 1: Enable
3	R/W	0x0	ADC_IRQ_EN. ADC FIFO Data Available IRQ Enable. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	ADC_OVERRUN_IRQ_EN. ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	ADC_FIFO_FLUSH. ADC FIFO Flush. Write ‘1’ to flush TX FIFO, self clear to ‘0’.

1.13.4.8. ADC FIFO STATUS REGISTER

Offset: 0x20			Register Name: AC_ADC_FIFOS
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R	0x0	RXA. RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:14	/	/	/
13:8	R	0x0	RXA_CNT. RX FIFO Available Sample Word Counter
7:4	/	/	/

Offset: 0x20			Register Name: AC_ADC_FIFOS
Bit	**Read/Write**	**Default**	**Description**
3	R/W	0x0	RXA_INT. RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/W	0x0	RXO_INT. RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

1.13.4.9. ADC RX DATA REGISTER

Offset: 0x24			Register Name: AC_ADC_RXDATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0x0	RX_DATA. RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

1.13.4.10. ADC ANALOG CONTROL REGISTER

Offset:0x28			Register Name: AC_PA_ADC_ACTRL
Bit	**R/W**	**Default**	**Description**
31	R/W	0x0	ADCREN. ADC Right Channel Enable 0-Disable 1-Enable

Offset:0x28			Register Name: AC_PA_ADC_ACTRL
Bit	**R/W**	**Default**	**Description**
30	R/W	0x0	ADCLEN. ADC Left Channel Enable 0-Disable 1-Enable
29	R/W	0x0	PREG1EN. MIC1 pre-amplifier Enable 0-Disable 1-Enable
28	R/W	0x0	PREG2EN. MIC2 pre-amplifier Enable 0-Disable 1-Enable
27	R/W	0x0	VMICEN. VMIC pin voltage enable 0: disable 1: enable
26:23	/	/	/
22:20	R/W	0x3	ADCG. ADC Input Gain Control 000: -4.5dB 001: -3dB 010: -1.5dB 011: 0dB 100: 1.5dB 101: 3dB 110: 4.5dB 111: 6dB
19:17	R/W	0x2	ADCIS. ADC input source select 000: left select LINEINL, right select LINEINR; or, both select LINEINL-LINEINR, depending on LNRDF (bit 16) 001: left channel select FMINL & right channel select FMINR 010: left and right channel both select MIC1 gain stage output 011: left and right channel both select MIC2 gain stage output 100: left select MIC1 gain stage output & right select MIC2 gain stage output

Offset:0x28			Register Name: AC_PA_ADC_ACTRL
Bit	R/W	Default	Description
			101: left and right both select MIC1 gain stage plus MIC2 gain stage output 110: left select output mixer L & right select output Mixer right 111: left select LINEINL or LINEINL-LINEINR, depending on LNRDF (bit 16), right select MIC1 gain stage
16	R/W	0x0	LNRDF. Line-in-r function define 0: Line-in right channel which is independent of line-in left channel 1: negative input of line-in left channel for fully differential application
15:13	R/W	0x4	LNPREG. Line-in pre-amplifier Gain Control From -12dB to 9dB, 3dB/step, default is 0dB
12	/	/	/
11	R/W	0	LHPOUTN Left Headphone Amplifier Output Negative To Right HPOUT Mute 0: mute 1: Not-mute
10	R/W	0	RHPOUTN Right Headphone Amplifier Output Negative To Left HPOUT Mute 0: mute 1: Not-mute
9	/	/	/
8	R/W	0x1	DITHER. ADC dither on/off control 0: dither off 1: dither on
7:6	R/W	0x1	DITHER_CLK_SELECT. ADC dither clock select 00: about 43KHz 01: about 51KHz 10: about 64KHz 11: about 85KHz
5	/	/	/
4	R/W	0x0	PA_EN.

Offset:0x28			Register Name: AC_PA_ADC_ACTRL
Bit	R/W	Default	Description
			PA Enable 0-disable 1-enable
3	R/W	0x1	DDE. Headphone direct-drive enable, (DDE): 0-disable 1-enable
2	R/W	0x1	COMPTEN. HPCOM output protection enable 0: protection disable 1: protection enable
1:0	R/W	0x0	PTDBS. HPCOM protect de-bounce time setting 00: 2-3ms 01: 4-6ms 10: 8-12ms 11: 16-24ms

1.13.4.11. DAC TX COUNTER REGISTER

Offset: 0x30			Register Name: AC_DAC_CNT
Bit	Read/Write	Default	Description
31:0	R/W	0x0	TX_CNT. TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

1.13.4.12. ADC RX COUNTER REGISTER

Offset: 0x34			Register Name: AC_ADC_CNT
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	RX_CNT. RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

1.13.4.13. BIAS & DA16 CALIBRATION VERIFY REGISTER

Offset: 0x38			Register Name: AC_DAC_CAL
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R/W	0x0	BIASCALIVERIFY. Bias Calibration Verify 0 0: Calibration 1: Register setting
22:17	R/W	0x20	BIASVERIFY. Bias Register Setting Data 101101
16:11	R	0x20	BIASCALI. Bias Calibration Data 100000
10	R/W	0x0	DA16CALIVERIFY. DA16 Calibration Verify 0: Calibration 1: Register setting 0
9:5	R/W	0x10	DA16VERIFY. DA16 Register Setting Data 10010
4:0	R	0x10	DA16CALI. DA16 Calibration Date 10000

1.13.4.14. MIC GAIN & PHONE OUT CONTROL REGISTER

Offset: 0x3c			Register Name: AC_MIC_PHONE_CAL
Bit	**R/W**	**Default**	**Description**
31:29	R/W	0x4	PREG1. MIC1 pre-amplifier Gain Control 000: 0dB 001: 24dB 010: 27dB 011: 30dB 100: 33dB 101: 36dB 110: 39dB 111: 42dB
28:26	R/W	0x4	PREG2. MIC2 pre-amplifier Gain Control 000: 0dB 001: 24dB 010: 27dB 011: 30dB 100: 33dB 101: 36dB 110: 39dB 111: 42dB
25:8	/	/	/
7:5	R/W	0x3	PHONEOUTG. PHONEOUT Gain Control 000: -4.5dB 001: -3.0dB 010: -1.5dB 011: 0dB 100: 1.5dB 101: 3dB 110: 4.5dB 111: 6dB
4	R/W	0	PHONEOUTEN. PHONEOUT enable 0: disable

Offset: 0x3c			Register Name: AC_MIC_PHONE_CAL
Bit	R/W	Default	Description
			1: enable
3	R/W	0	PHONEOUTS3. MIC1 Boost stage to Phone out mute 0: Mute 1: Not mute
2	R/W	0	PHONEOUTS2. MIC2 Boost stage to Phone out mute 0: Mute 1: Not mute
1	R/W	0	PHONEOUTS1. Right Output mixer to Phone out mute 0: Mute 1: Not mute
0	R/W	0	PHONEOUTS0 Left Output mixer to Phone out mute 0: Mute 1: Not mute

1.14. LRADC

1.14.1. Overview

LRADC is of 6-bit resolution for key application.

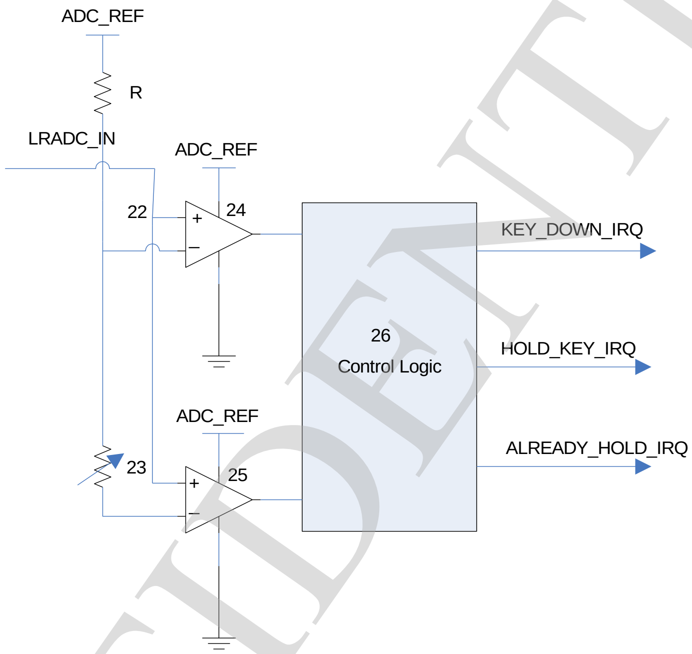
It features:

- Support APB 32-bits bus width
- Support interrupt
- Support Hold Key and General Key
- Support Single Key and Continue key mode
- 6-bit resolution
- Support voltage input range from 0V to 2V

1.14.2. LRADC Block Diagram

The LRADC converted data can by accessed by interrupt and polling method. If software can't access the last converted data instantly, the new converted data would update the old one at new sampling data.

Hold Key and General Key Function Introduction



When ADC_IN Signal change from ADC_REF to 2/3 ADC_REF (Level A), the comparator24 sends first interrupt to control logic; When ADC_IN Signal changes from 2/3 ADC_REF to certain level (configurable), the comparator25 gives the second interrupt. If the control Logic gets the first interrupt, in a certain time range (program can set), doesn't get second interrupt, it will send hold key interrupt to the host; If the control Logic get the first interrupt, In a certain time range (program can set), get second interrupt, it will send key down interrupt to the host; If the control logic only get the second interrupt, doesn't get the first interrupt, it will send already hold interrupt to the host.

1.14.3. LRADC Register List

Module Name	Base Address

Module Name	Base Address
LRADC	0x01C22800

Register Name	Offset	Description
LRADC_CTRL	0x00	LRADC Control Register
LRADC_INTC	0x04	LRADC Interrupt Control Register
LRADC_INTS	0x08	LRADC Interrupt Status Register
LRADC_DATA0	0x0c	LRADC Data Register 0
LRADC_DATA1	0x10	LRADC Data Register 1

1.14.4. LRADC Register Description

1.14.4.1. LRADC CONTROL REGISTER

Offset: 0x00			Register Name: LRADC_CTRL
Bit	**Read/ Write**	**Default/Hex**	**Description**
31: 24	R/W	0x1	FIRST_CONCERT_DLY. ADC First Convert Delay setting, ADC conversion is delayed by n samples
23:22	R/W	0x0	ADC_CHAN_SELECT. ADC channel select 00: ADC0 channel 01: ADC1 channel 1x: ADC0&ADC1 channel
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode time select, one of 8*(N+1) sample as a valuable sample data
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select: 00: Normal Mode

Offset: 0x00			Register Name: LRADC_CTRL
Bit	**Read/ Write**	**Default/Hex**	**Description**
			01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples
7	/	/	/
6	R/W	0x1	LRADC_HOLD_EN. LRADC Sample hold Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (~1.9v) 01: 0x39 (~1.8v) 10: 0x36 (~1.7v) 11: 0x33 (~1.6v)
3: 2	R/W	0x2	LRADC_SAMPLE_RATE. LRADC Sample Rate 00: 250 Hz 01: 125 Hz 10: 62.5 Hz 11: 32.25 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN. LRADC enable 0: Disable 1: Enable

1.14.4.2. LRADC INTERRUPT CONTROL REGISTER

Offset: 0x04			Register Name: LRADC_INTC
Bit	**Read/ Write**	**Default/Hex**	**Description**

Offset: 0x04			Register Name: LRADC_INTC
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
12	R/W	0x0	ADC1_KEYUP_IRQ_EN. ADC 1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN. ADC 1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC 1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYIRQ_EN. ADC 1 Key IRQ Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN. ADC 1 DATA IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN. ADC 0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN. ADC 0 Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN. ADC 0 Hold Key IRQ Enable 0: Disable 1: Enable

Offset: 0x04			Register Name: LRADC_INTC
Bit	Read/ Write	Default/Hex	Description
1	R/W	0x0	ADC0_KEYDOWN_EN ADC 0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN. ADC 0 Data IRQ Enable 0: Disable 1: Enable

1.14.4.3. LRADC INTERRUPT STATUS REGISTER

Offset: 0x08			Register Name: LRADC_INT
Bit	Read/ Write	Default/Hex	Description
31:8	/	/	/
12		0x0	ADC1_KEYUP_PENDING. ADC 1 Key up pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
11	R/W	0x0	ADC1_ALRDY_HOLD_PENDING. ADC 1 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
10	R/W	0x0	ADC1_HOLDKEY_PENDING. ADC 1 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt

Offset: 0x08			Register Name: LRADC_INT
Bit	**Read/ Write**	**Default/Hex**	**Description**
			line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
9	R/W	0x0	ADC1_KEYDOWN_IRQ_PENDING. ADC 1 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
8	R/W	0x0	ADC1_DATA_IRQ_PENDING. ADC 1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_PENDING. ADC 0 Key up pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
3	R/W	0x0	ADC0_ALRDY_HOLD_PENDING. ADC 0 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled
2	R/W	0x0	ADC0_HOLDKEY_PENDING.

Offset: 0x08			Register Name: LRADC_INT
Bit	**Read/ Write**	**Default/Hex**	**Description**
			ADC 0 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W	0x0	ADC0_KEYDOWN_PENDING. ADC 0 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W	0x0	ADC0_DATA_PENDING. ADC 0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

1.14.4.4. LRADC DATA 0 REGISTER

Offset: 0x0c			Register Name: LRADC_DATA
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x0	LRADC0_DATA. LRADC 0 Data

1.14.4.5. LRADC DATA 1 REGISTER

Offset: 0x10			Register Name: LRADC_DATA
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x0	LRADC1_DATA. LRADC 1 Data

1.15. TP

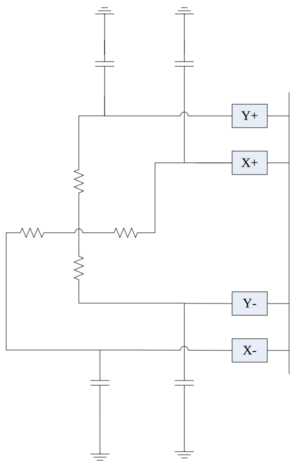
1.15.1. Overview

The TP controller is a 4-wire resistive touch screen controller, including 12-bit resolution A/D converter. Especially, it provides the ability of dual touch detection. The controller through the implementation of the two A/D conversion has been identified by the location of the screen of single touch, in addition to measurable increase in pressure on the touch screen.

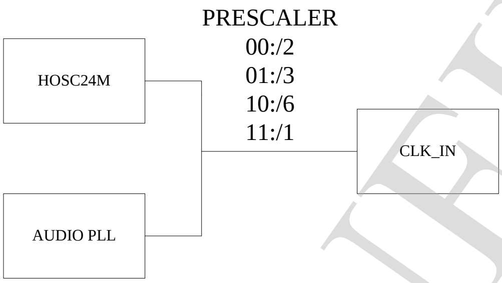
It features:

- 12-bit SAR type A/D converter
- 4-wire I/F
- Dual touch detection
- Touch-pressure measurement (Support programmable threshold)
- Sampling frequency up to 2MHz
- Single-Ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change

1.15.2. Typical Application Circuit



1.15.3. TP Clock Tree



1.15.4. A/D Conversion Time

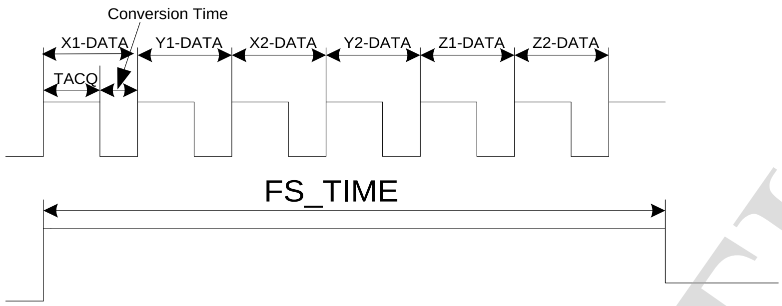
When the clock source is 24MHz and the prescaler value is 6, total 12-bit conversion time is as following:

CLK_IN = 24MHz/6 = 4MHz

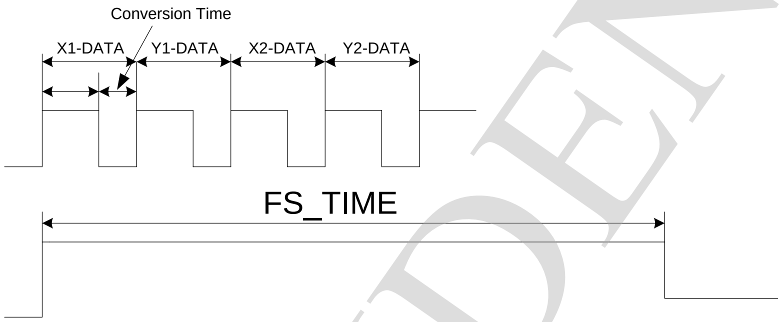
Conversion Time = 1/(4MHz/13Cycles) = 3.25us

FS_TIME (Frequency Scan Time) bases on TACQ and Touch Mode, they must meet the following inequation: FS_TIME >= M*(TACQ + Conversion Time)

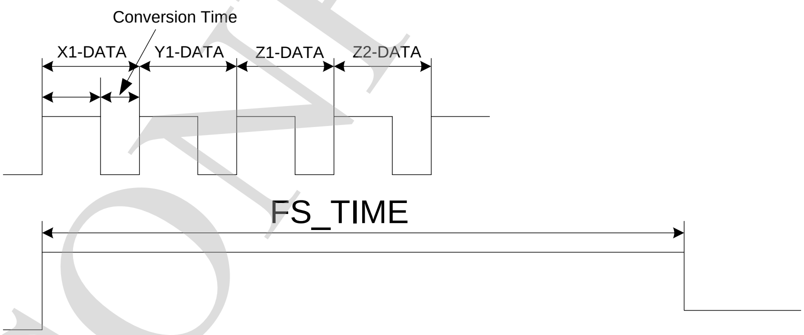
For example, if touch acquire time divider is 15, then TACQ = 4MHz /(16*(15+1)) = 64us. When TP mode is dual and pressure measurement mode, then M=6, and the FS_TIME must be no less than 6*(64 + 3.25) us.



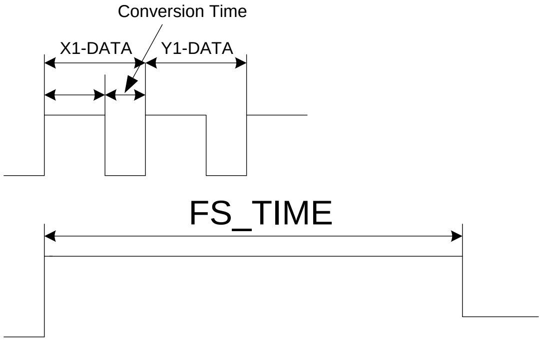
Dual Touch and Pressure Measurement



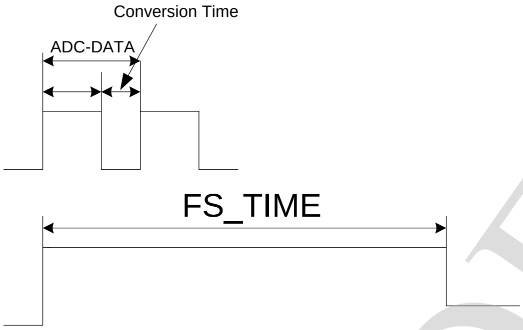
Dual Touch No Pressure Measurement



Single Touch and Pressure Measurement Mode



Single Touch No Pressure Measurement Mode



General ADC Mode

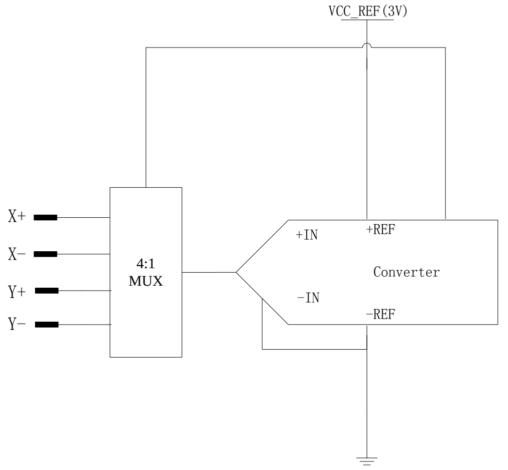
1.15.5. Principle of Operation

BASIC PRINCIPLE

The controller is a typical type of successive approximation ADC (SAR ADC), contains a sample/hold, analog-to-digital conversion, serial data output functions. The analog inputs (X+,X-,Y+,Y-) via control register enter the ADC, ADC can work in single-ended or differential mode. Selecting Aux ADC or temperature should work in single-ended mode; as a touch screen application, it works in a differential mode, which can effectively eliminate the impact on conversion accuracy caused by the parasitic resistance of the driver switch and external interference.

SINGLE-ENDED MODE

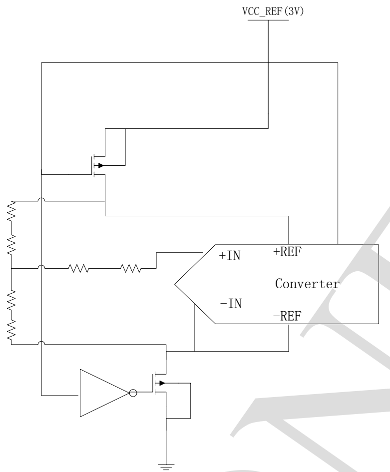
When the TP controller is in the measurement mode of AUX or Temp, the internal ADC is in single-ended mode, using the 3V reference source as the ADC reference voltage, application of the principle of single-ended mode is shown below:



Simplified Diagram of Single-Ended Reference

DIFFERENTIAL MODE

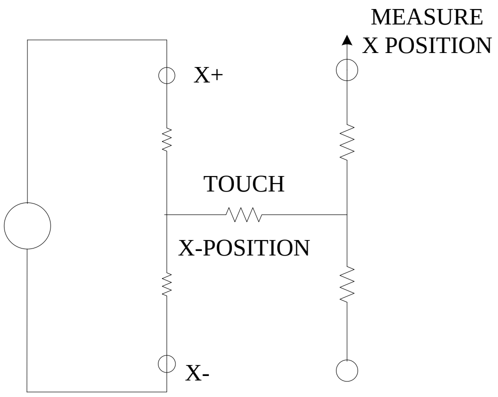
When the TP controller is in the measurement mode of X,Y,Z, the internal ADC is in differential mode. The advantage of differential mode is that +REF and –REF can input directly to the Y+, Y-, which can eliminate measurement error because of the switch on resistance. The disadvantage is that during both the sample and conversion process, the driver will need to be on, which will increase the power consumption.



Simplified Diagram of Differential Reference

SINGLE TOUCH DETECTION

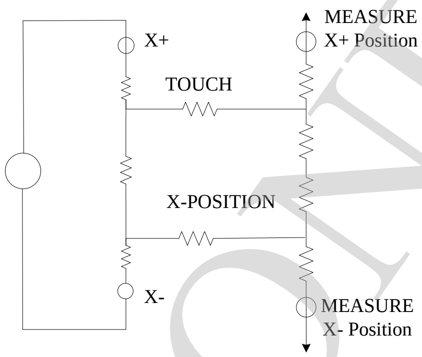
The principle of operation is illustrated below, For an X coordinate measurement, the X+ pin is internally switched to VCC_REF and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the Y+, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. Y coordinate measurements are similar to X coordinate measurements, with the X and Y plates interchanged. In Single Touch mode, only need to test X+, Y+ signal. But In Dual Touch mode, it need to test X+, X-,Y+,Y- signal.



Single Touch X-Position Measurement

DUAL TOUCH DETECTION

The principle of operation is illustrated below, For an X coordinate measurement, the X+ pin is internally switched to 3V and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X coordinate. This voltage is measured on the Y+ and Y-, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. the controller will need to test X+,X-,Y+,Y- , and record ΔX=|X+ - X-|, ΔY= | Y+ - Y-|. In practice, we can set a threshold. If ΔX or ΔY greater than the threshold, we consider it as a dual touch, otherwise as a single touch.



Dual Touch X-Position Measurements

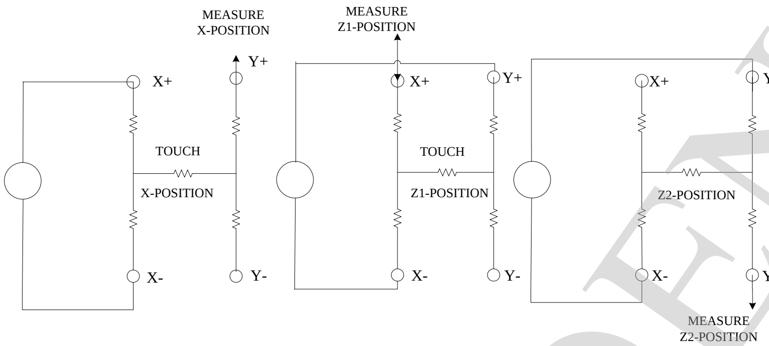
TOUCH-PRESSURE MEASUREMENT

The pressure applied to the touch screen by a pen or finger to filter unavailable can also be measured by the controller using some simple calculations. The contact resistance between the X and Y plates is measured, provide a good indication of the size of the depressed area and the applied pressure. The area of the touch spot t is proportional to the size of the object touching it. And the value of this resistance (R_{touch}) can be calculated using two different methods.

First Method

The first method requires the user to know the total resistance of the X plate tablet (R_{XPLATE}). Three touch screen conversions are required: measurement of the X position, $X_{POSITION}$(Y+ input); measurement of the X+ input with the excitation voltage applied to Y+ and X− (Z1 measurement); and measurement of the Y− input with the excitation voltage applied to Y+ and X− (Z2 measurement). These three measurements are illustrated in Figure 12. The controller have two special ADC channel settings to configure the X and Y switches for the Z1 and Z2 measurements and store the results in the Z1 and Z2 result registers. The touch resistance (R_{TOUCH}) can then be calculated using the following equation:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION} /4096) \times [(Z2/Z1) - 1] \quad (1)$$



Pressure Measurement Block Diagram

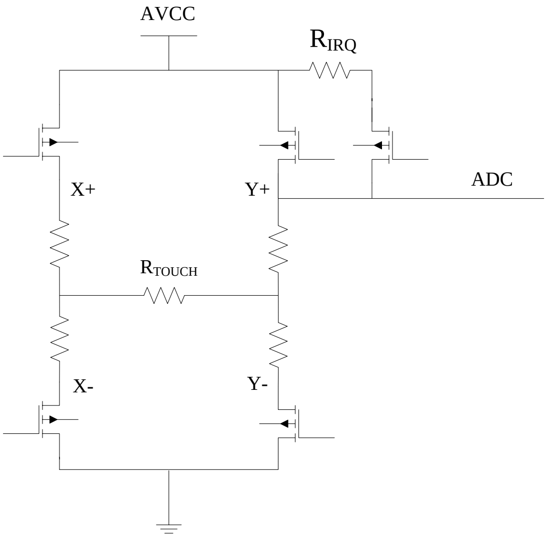
Second Method

The second method requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position. The following equation also calculates the touch resistance (R_{TOUCH}):

$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times [(4096/Z1) - 1] - R_{YPLATE} \times [1 - (Y_{POSITION}/4096)]$ (2)

PEN DOWN DETECTION, WITH PROGRAMMABLE SENSITIVITY

Pen down detection is used as an interrupt to the host. R_{IRQ} is an internal pull-up resistor with a programmable value of 6~96 kΩ (default 48kΩ). The pen down IRQ output is pulled high by an internal pull-up. In the pen down detection, the Y– driver is on and connected to GND, and the pen down IRQ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the pen down IRQ output goes low because of the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-position, the X+ input is disconnected from the pen down IRQ pull-down transistor to eliminate any pull-up resistor leakage current from flowing through the touch screen, thus causing no errors.



Example of Pen touch Interrupt via Pen Down IRQ

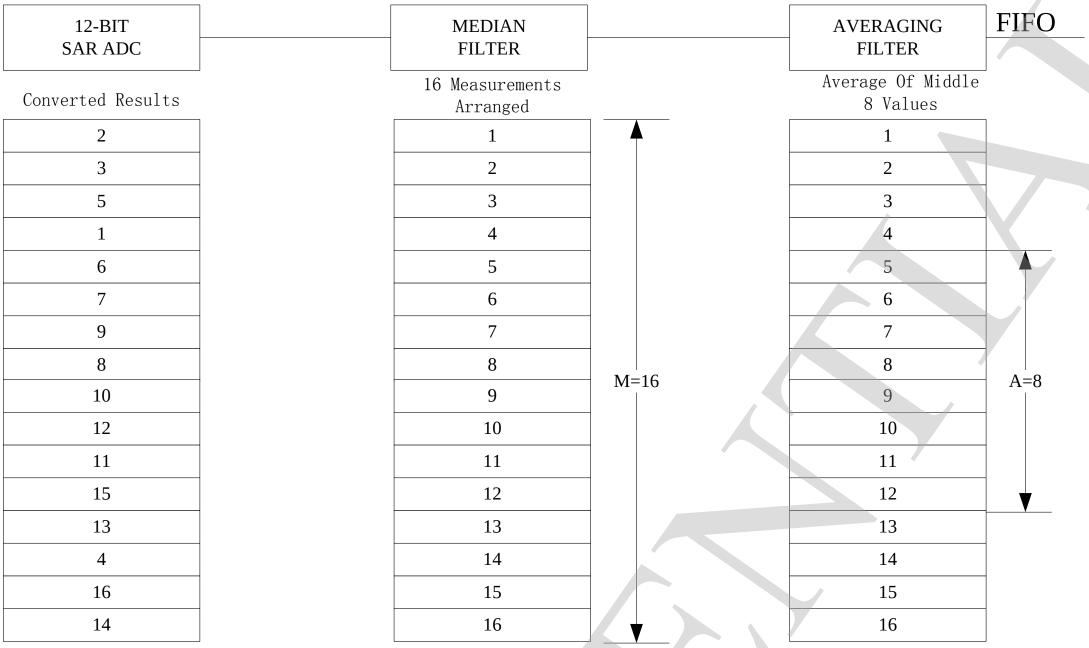
MEDIAN AND AVERAGING FILTER

As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements. The controller contain a filtering block to process the data and discard the spurious noise before sending the information to the host. The purpose of this block is not only the suppression of noise; the on-chip filtering also greatly reduces the host processing loading. The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter. The median filter suppresses the isolated out-of-range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Then the averaging filter size determines the number of values to average. There are four choises which is configured by TP_CTRL3 register (bit 1 and bit 0) to filtrate the ADC sampling data. It is showed in following table.

Median and averaging Filter Size (TP_CTRL3)

bit1	bit0	Averaging Filter Size	Median Filter Size
0	0	2	4
0	1	3	5
1	0	4	8
1	1	8	16

In this example, the TP_CTRL3 register bit 1 and bit 0 is configured as 2’b11. So the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array. The averaging window size in this example is 8. The output is the average of the middle eight values of the 16 measurements taken with the median filter.



Median and Averaging Filter Example

1.15.6. TP Register List

Module Name	Base Address
TP	0x01C25000

Register Name	Offset	Description
TP_CTRL0	0x00	TP Control Register0
TP_CTRL1	0x04	TP Control Register1
TP_CTRL2	0x08	TP Pressure Measurement and touch sensitive Control Register
TP_CTRL3	0x0c	Median and averaging filter Controller Register
TP_INT_FIFOC	0x10	TP Interrupt FIFO Control Register
TP_INT_FIFOS	0x14	TP Interrupt FIFO Status Register

Register Name	Offset	Description
TP_TPR	0x18	TP Temperature Period Register
TP_CDAT	0x1c	TP Common Data
TEMP_DATA	0x20	Temperature Data Register
TP_DATA	0x24	TP Data Register
TP_IO_CONFIG	0x28	TP IO Configuration
TP_PORT_DATA	0x2c	TP IO Port Data

1.15.7. TP Register Description

1.15.7.1. TP CONTROL REGISTER 0

Offset: 0x00			Register Name: TP_CTRL0
Bit	**Read/ Write**	**Default /Hex**	**Description**
31:24	R/W	0xF	ADC_FIRST_DLY. ADC First Convert Delay Time(T_FCDT)setting Based on ADC First Convert Delay Mode select (Bit 23) T_FCDT = ADC_FIRST_DLY * ADC_FIRST_DLY_MODE
23	R/W	0x1	ADC_FIRST_DLY_MODE. ADC First Convert Delay Mode Select 0: CLK_IN/16 1: CLK_IN/16*256
22	R/W	0x0	ADC_CLK_SELECT. ADC Clock Source Select: 0: HOSC(24MHZ) 1: Audio PLL
21:20	R/W	0x0	ADC_CLK_DIVIDER. ADC Clock Divider(CLK_IN) 00: CLK/2 01: CLK/3 10: CLK/6 11: CLK/1

Offset: 0x00			Register Name: TP_CTRL0
Bit	**Read/ Write**	**Default /Hex**	**Description**
19:16	R/W	0x0	FS_DIV. ADC Sample Frequency Divider 0000: CLK_IN/$2^{(20-n)}$ 0001: CLK_IN/$2^{(20-n)}$ 0010: CLK_IN/$2^{(20-n)}$ …. 1111: CLK_IN/32
15:0	R/W	0x0	TACQ. Touch panel ADC acquire time CLK_IN/(16*(N+1))

1.15.7.2. TP CONTROL REGISTER 1

Offset: 0x04			Register Name: TP_CTRL1
Bit	**Read/ Write**	**Default /Hex**	**Description**
31:20	/	/	/
19:12	R/W	0x0	STYLUS_UP_DEBOUNCE. Stylus Up De-bounce Time setting 0x00: 0 …. 0xff: 2N*(CLK_IN/16*256)
11:10	/	/	/
9	R/W	0x0	STYLUS_UP_DEBOUCE_EN. Stylus Up De-bounce Function Select 0: Disable 1: Enable
8	/	/	/
7	R/W	0x1	CHOP_TEMP_EN Chop temperature calibration enable 0: Disable 1: Enable
6	R/W	0x0	TOUCH_PAN_CALI_EN.

Offset: 0x04			Register Name: TP_CTRL1
Bit	**Read/ Write**	**Default /Hex**	**Description**
			Touch Panel Calibration 1: start Calibration, it is clear to 0 after calibration
5	R/W	0x0	TP_DUAL_EN. Touch Panel Double Point Enable 0: Disable 1: Enable
4	R/W	0x0	TP_MODE_EN. Tp Mode Function Enable 0: Disable 1: Enable
3	R/W	0x1	TP_ADC_SELECT. Touch Panel and ADC Select 0: TP 1: ADC
2:0	R/W	0x0	ADC_CHAN_SELECT. Analog input channel Select In Normal mode: 000: X1 channel 001: X2 Channel 010: Y1 Channel 011: Y2 Channel 1xx : 4-channel robin-round FIFO Access Mode,based on this setting. Selecting one channel, FIFO will access that channel data; Selecting four channels FIFO will access each channel data in successive turn, first is X1 data.

1.15.7.3. TP CONTROL REGISTER 2

Offset: 0x08			Register Name: TP_CNT2
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:28	R/W	0x8	TP_SENSITIVE_ADJUST. Internal Pull-up Resistor Control 0000 least sensitive 0011

Offset: 0x08			Register Name: TP_CNT2
Bit	Read/ Write	Default/Hex	Description
			…… 1111 most sensitive Notes: Used to adjust sensitivity of pen down detection
27:26	R/W	0x0	TP_FIFO_MODE_SELECT. TP FIFO Access Data Mode Select 00: FIFO store X1,Y1 data for single touch no pressure mode 01: FIFO store X1,Y1, △X, △Y data for dual touch no pressure mode 10: FIFO store X1,Y1, X2,Y2 data for dual touch no pressure mode 11: FIFO store X1,Y1, X2,Y2,Z1,Z2 data for dual touch and pressure mode Notes: The ADC output data in single touch mode can store in FIFO with TP_FIFO_MODE_SELECT configured as 01,10,11. But the data △X, △Y is theoretically equal to zero and X2,Y2 is equal to X1,Y1.
25	/	/	/
24	R/W	0x0	PRE_MEA_EN. TP Pressure Measurement Enable Control 0: Disable 1: Enable
23:0	R/W	0xFFF	PRE_MEA_THRE_CNT. TP Pressure Measurement threshold Control Notes: 0x000000: least sensitive 0xFFFFFF: most sensitive Notes: used to adjust sensitivity of touch

1.15.7.4. MEDIAN AND AVERAGING FILTER CONTROL REGISTER

Offset: 0x0c			Register Name: TP_CTRL3
Bit	Read/ Write	Default/ Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN.

			Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Filter Type 00: 4/2 01: 5/3 10: 8/4 11: 16/8

1.15.7.5. TP INTERRUPT& FIFO CONTROL REGISTER

Offset: 0x10			**Register Name: TP_INT**
Bit	**Read/ Write**	**Default/ Hex**	**Description** **0x0000_0F00**
31:19	/	/	/
18	R/W	0x0	TEMP_IRQ_EN. Temperature IRQ Enable 0: Disable 1: Enable
17	R/W	0x0	TP_OVERRUN_IRQ_EN. TP FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	TP_DATA_IRQ_EN. TP FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13	R/W	0x0	TP_DATA_XY_CHANGE. TP FIFO X,Y Data interchange Function Select 0: Disable 1: Enable
12:8	R/W	0xF	TP_FIFO_TRIG_LEVEL. TP FIFO Data Available Trigger Level

Offset: 0x10			Register Name: TP_INT
Bit	**Read/ Write**	**Default/ Hex**	**Description** **0x0000_0F00**
			Interrupt and DMA request trigger level for TP or Auxiliary ADC Trigger Level = TXTL + 1
7	R/W	0x0	TP_DATA_DRQ_EN. TP FIFO Data Available DRQ Enable 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	TP_FIFO_FLUSH. TP FIFO Flush Write '1' to flush TX FIFO, self clear to '0'
3:2	/	/	/
1	R/W	0x0	TP_UP_IRQ_EN. Touch Panel Last Touch (Stylus Up) IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	TP_DOWN_IRQ_EN. Touch Panel First Touch (Stylus Down) IRQ Enable 0: Disable 1: Enable

1.15.7.6. TP INTERRUPT& FIFO STATUS REGISTER

Offset: 0x14			Register Name: TP_FIFOCS
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	TEMP_IRQ_PENDING. Temperature IRQ Pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
17	R/W	0x0	FIFO_OVERRUN_PENDING.

			TP FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
16	R/W	0x0	FIFO_DATA_PENDING. TP FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
15:13	/	/	/
12:8	R	0x0	RXA_CNT. TP FIFO available Sample Word Counter
7:3	/	/	/
2	R	0x0	TP_IDLE_FLG. Touch Panel Idle Flag 0: idle 1: not idle
1	R/W	0x0	TP_UP_PENDING. Touch Panel Last Touch (Stylus Up) IRQ Pending bit 0: No IRQ 1: IRQ Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
0	R/W	0x0	TP_DOWN_PENDING. Touch Panel First Touch (Stylus Down) IRQ Pending bit 0: No IRQ 1: IRQ Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.

1.15.7.7. TP TEMPERATURE PERIOD REGISTER

Offset: 0x18			**Register Name: TP_TPR**
Bit	**Read/ Write**	**Default/ Hex**	**Description**

Offset: 0x18			Register Name: TP_TPR
Bit	Read/ Write	Default/ Hex	Description
31:16	/	/	/
16	R/W	0x0	TEMP_EN. Temperature enable
15:0	R/W	0x0	TEMP_PER. Temperature Period 4096*(1/clk_in)

1.15.7.8. COMMON DATA REGISTER

Offset: 0x1c			Register Name: TP_CDAT
Bit	Read/ Write	Default/ Hex	Description
31:12	/	/	/
11:0	R/W	0x800	TP_CDAT. TP Common Data Notes: used to adjust the tolerance of the internal ADC

1.15.7.9. TEMPERATURE DATA REGISTER

Offset: 0x20			Register Name: TEMP_DATA
Bit	Read/ Write	Default/Hex	Description Default: 0x0000_0000
31:12	/	/	/
11:0	R	0x0	TEMP_DATA. Temperature Data Value

1.15.7.10. TP DATA REGISTER

Offset: 0x24	Register Name: TP_DATA

Bit	Read/ Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TP_DATA. Touch Panel X ,Ydata or Auxiliary analog input data converted by the internal ADC

1.15.7.11. 3.6.11 TP PORT IO CONFIGURE REGISTER

Offset: 0x28			Register Name: TP_IO_CONFIG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x2	TY_N_SELECT TY_N Port Function Select: 000:Input 001:Output 010: TP_YN 011:/ 100: / 101:/ 110: / 111:/
11	/	/	/
10:8	R/W	0x2	TY_P_SELECT TY_P Port Function Select: 000:Input 001:Output 010: TP_YP 011:/ 100: / 101:/ 110: / 111:/
7	/	/	/
6:4	R/W	0x2	TX_N_SELECT TX_P Port Function Select: 000:Input 001:Output 010: TP_XN 011:/ 100: / 101:/ 110: / 111:/
3	/	/	/
2:0	R/W	0x2	TX_P_SELECT TX_P Port Function Select:

Offset: 0x28			Register Name: TP_IO_CONFIG
Bit	Read/ Write	Default/Hex	Description
			000:Input 001:Output 010: TP_XP 011:/ 100: / 101:/ 110: / 111:/

1.15.7.12. TP PORT DATA REGISTER

Offset: 0x2c			Register Name: TP_PORT_DATA
Bit	Read/ Write	Default/ Hex	Description
31:12	/	/	/
3:0	R/W	0x0	TP_PORT_DATA TP Port Data Value, TP_YN,TP_YP, TP_XN, TP_XP(y2/y1/x2/x1)

1.16. Security System

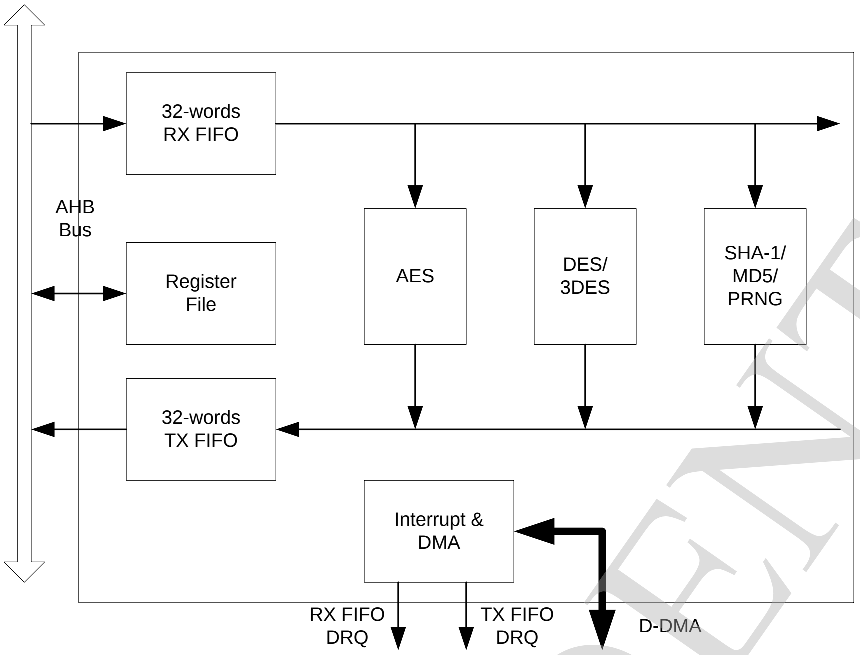
1.16.1. Overview

The Security System (SS) is one encrypt/ decrypt function accelerator that is suitable for a variety of applications. It supports both encryption and decryption. Several modes are supported by the SS module.

It features:

- AES, DES, 3DES, SHA-1, MD5 are supported by this system
- ECB, CBC, CNT modes for AES/DES/3DES
- 128-bit, 192-bit and 256-bit key size for AES
- 160-bit hardware PRNG with 192-bit seed
- 32-word RX FIFO and 32-word TX FIFO for high speed application
- Support CPU mode and DMA mode
- Interrupt support

1.16.2. Security System Block Diagram



1.16.3. Security System Register List

Module Name	Base Address	
SS	0x01C15000	

Register Name	Offset	Description
SS_CTL	0x00	Security Control Register
SS_KEY0	0x04	Security Input Key 0/ PRNG Seed 0
SS_KEY1	0x08	Security Input Key 1/ PRNG Seed 1
…	…	…
SS_KEY7	0x20	Security Input Key 7
SS_IV0	0x24	Security Initialization Vector 0

Register Name	Offset	Description
SS_IV1	0x28	Security Initialization Vector 1
SS_IV2	0x2C	Security Initialization Vector 2
SS_IV3	0x30	Security Initialization Vector 3
SS_CNT0	0x34	Security Preload Counter 0
SS_CNT1	0x38	Security Preload Counter 1
SS_CNT2	0x3C	Security Preload Counter 2
SS_CNT3	0x40	Security Preload Counter 3
SS_FCSR	0x44	Security FIFO Control/ Status Register
SS_ICSR	0x48	Security Interrupt Control/ Status Register
SS_MD0	0x4C	SHA1/MD5 Message Digest 0/PRNG Data0
SS_MD1	0x50	SHA1/MD5 Message Digest 1/PRNG Data1
SS_MD2	0x54	SHA1/MD5 Message Digest 2/PRNG Data2
SS_MD3	0x58	SHA1/MD5 Message Digest 3/PRNG Data3
SS_MD4	0x5C	SHA1/MD5 Message Digest 4/PRNG Data4
SS_CTS_LEN	0x60	AES-CTS ciphertext length
SS_RXFIFO	0x200	RX FIFO input port
SS_TXFIFO	0x204	TX FIFO output port

1.16.4. Security System Register Description

1.16.4.1. SECURITY SYSTEM CONTROL REGISTER

Offset: 0x00			**Register Name: SS_CTL** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:24	R/W	0	SKEY_SELECT AES/DES/3DES key select 0: Select input SS_KEYx (Normal Mode) 1: Select SID_RKEYx from Security ID 2: Select SID_BKEYx from Security ID

Offset: 0x00			Register Name: SS_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			3-10: Select internal Key n (n from 0 to 7) Others: Reserved
18:16	R	x	DIE_ID Die Bonding ID
15	R/W	0	PRNG_MODE PRNG generator mode 0: One-shot mode 1: Continue mode
14	R/W	0	IV_MODE IV Steady of SHA-1/MD5 constants 0: Constants 1: Arbitrary IV Notes: It is only used for SHA-1/MD5 engine. If the number of IV word is beyond of 4, Counter 0 register is used for IV4.
13:12	R/W	0	SS_OP_MODE SS Operation Mode 00: Electronic Code Book (ECB) mode 01: Cipher Block Chaining (CBC) mode 10: Counter (CNT) mode 11: AES Ciphertext Stealing (CTS) mode
11:10	R/W	0	CNT_WIDTH Counter Width for CNT Mode 00: 16-bits Counter 01: 32-bits Counter 10: 64-bits Counter 11: Reserved
9:8	R/W	0	AES_KEY_SIZE Key Size for AES 00: 128-bits 01: 192-bits 10: 256-bits 11: Reserved
7	R/W	0	SS_OP_DIR SS Operation Direction

Offset: 0x00			Register Name: SS_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			0: Encryption 1: Decryption
6:4	R/W	0	SS_METHOD SS Method 000: AES 001: DES 010: Triple DES (3DES) 011: SHA-1 100: MD5 101: PRNG Others: Reserved
3	/	/	/
2	R/W	0	SHA1_MD5_END_BIT SHA-1/MD5 Data End bit Write '1' to tell SHA-1/MD5 engine that the text data is end. If there is some data in FIFO, the engine would fetch these data and process them. After finishing message digest, this bit is clear to '0' by hardware and message digest can be read out from digest registers. Notes: It is only used for SHA-1/MD5 engine.
1	R/W	0	PRNG_START PRNG start bit In PRNG one-shot mode, write '1' to start PRNG. After generating one group random data (5 words), this bit is clear to '0' by hardware.
0	R/W	0	SS_ENABLE SS Enable A disable on this bit overrides any other block and flushes all FIFOs. 0: Disable 1: Enable

1.16.4.2. SECURITY SYSTEM KEY [N] REGISTER

Offset: 0x04 +4*n			Register Name: SS_KEY[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	SS_KEY Key[n] Input Value (n= 0~7)/ PRNG Seed[n] (n= 0~5)

1.16.4.3. SECURITY SYSTEM IV[N] REGISTER

Offset: 0x24 +4*n			Register Name: SS_IV[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	SS_IV_VALUE Initialization Vector (IV[n]) Input Value (n= 0~3)

1.16.4.4. SECURITY SYSTEM COUNTER[N] REGISTER

Offset: 0x34 +4*n			Register Name: SS_CNT[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	SS_CNT_VALUE Counter mode preload Counter Input Value (n= 0~3)

1.16.4.5. SECURITY SYSTEM FIFO CONTROL/ STATUS REGISTER

Offset: 0x44			Register Name: SS_FCSR Default Value: 0x6000_0F0F
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30	R	0x1	RXFIFO_STATUS RX FIFO Empty 0: No room for new word in RX FIFO

Offset: 0x44			Register Name: SS_FCSR Default Value: 0x6000_0F0F
Bit	**Read/Write**	**Default**	**Description**
			1: More than one room for new word in RX FIFO (>= 1 word)
29:24	R	0x20	RXFIFO_EMP_CNT RX FIFO Empty Space Word Counter
23	/	/	/
22	R	0	TXFIFO_STATUS TX FIFO Data Available Flag 0: No available data in TX FIFO 1: More than one data in TX FIFO (>= 1 word)
21:16	R	0	TXFIFO_AVA_CNT TX FIFO Available Word Counter
15:13	/	/	/
12:8	R/W	0xF	RXFIFO_INT_TRIG_LEVEL RX FIFO Empty Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1 Notes: RX FIFO is used for input the data.
7:5	/	/	/
4:0	R/W	0xF	TXFIFO_INT_TRIG_LEVEL TX FIFO Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL + 1 Notes: TX FIFO is used for output the result data.

1.16.4.6. SECURITY SYSTEM INTERRUPT CONTROL/ STATUS REGISTER

Offset: 0x48			Register Name: SS_ICSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:11	/	/	/
10	R/W	0	RXFIFO_EMP_PENDING_BIT

Offset: 0x48			Register Name: SS_ICSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			RX FIFO Empty Pending bit 0: No pending 1: RX FIFO Empty pending Notes: Write ‘1’ to clear or automatic clear if interrupt condition fails.
9	/	/	/
8	R/W	0	TXFIFO_AVA_PENDING_BIT TX FIFO Data Available Pending bit 0: No TX FIFO pending 1: TX FIFO pending Notes: Write ‘1’ to clear or automatic clear if interrupt condition fails.
7:5	/	/	/
4	R/W	0	DRA_ENABLE DRQ Enable 0: Disable DRQ (CPU polling mode) 1: Enable DRQ (DMA mode)
3	/	/	/
2	R/W	0	RXFIFO_EMP_INT_ENABLE RX FIFO Empty Interrupt Enable 0: Disable 1: Enable Notes: If it is set to ‘1’, when the number of empty room is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set.
1	/	/	/
0	R/W	0	TXFIFO_AVA_INT_ENABLE TX FIFO Data Available Interrupt Enable 0: Disable 1: Enable Notes: If it is set to ‘1’, when available data number is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set.

1.16.4.7. SECURITY SYSTEM MESSAGE DIGEST[N] REGISTER

Offset: 0x4C +4*n			Register Name: SS_MD[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	SS_MID_DATA SHA1/ MD5 Message digest MD[n] for SHA1/MD5 (n= 0~4)

1.16.4.8. SECURITY SYSTEM CTS LENGTH REGISTER

Offset: 0x60			Register Name: SS_CTS_LEN Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	AES-CTS ciphertext length in byte unit The value of ‘0’ means no data.

1.16.4.9. SECURITY SYSTEM RX FIFO REGISTER

Offset: 0x200			Register Name: SS_RX Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0	SS_RX_FIFO 32-bits RX FIFO for Input

1.16.4.10. SECURITY SYSTEM TX FIFO REGISTER

Offset: 0x204			Register Name: SS_TX Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	SS_TX_FIFO 32-bits TX FIFO for Output

1.16.4.11. SECURITY SYSTEM CLOCK REQUIREMENT

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	>=24MHz
ss_clk	SS serial clock	<= 150MHz

1.17. Security JTAG

1.17.1. Overview

This is authentication module for security JTAG. There are two bits in EFUSE field. The two bits can be program before ship. One bit is used for enable/disable JTAG function and another bit is used for whether JTAG authentication function is ON. When JTAG function and JTAG authentication function is ON, the user must provide JTAG password before using JTAG function.

1.17.2. Security JTAG Register List

Module Name	Base Address
SJTAG	0x01C23C00

1.17.3. Security JTAG Register Description

1.17.3.1. SJTAG PASSWORD 0 REGISTER

Offset: 0x00			**Register Name: SJTAG_PWD0** **Default Value: 0xXXXX_XXXX**
Bit	**Read/Write**	**Default**	**Description**
31:0	W	x	JTAG_PWD SJTAG Password [31:0]

1.17.3.2. SJTAG PASSWORD 1 REGISTER

Offset: 0x04			**Register Name: SJTAG_PWD1** **Default Value: 0xXXXX_XXXX**
Bit	**Read/Write**	**Default**	**Description**
31:0	W	x	JTAG_PWD SJTAG Password [63:32]

1.17.3.3. SJTAG STATUS REGISTER

Offset: 0x08			**Register Name: SJTAG_STATUS** **Default Value: 0xXXXX_XXXX**
Bit	**Read/Write**	**Default**	**Description**
31:1	/	/	/

Offset: 0x08			Register Name: SJTAG_STATUS Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
0	R	x	JTAG_ONOFF_FLAG JTAG function ON/OFF flag 0: JTAG function is ON 1: JTAG function is OFF

1.18. Security ID

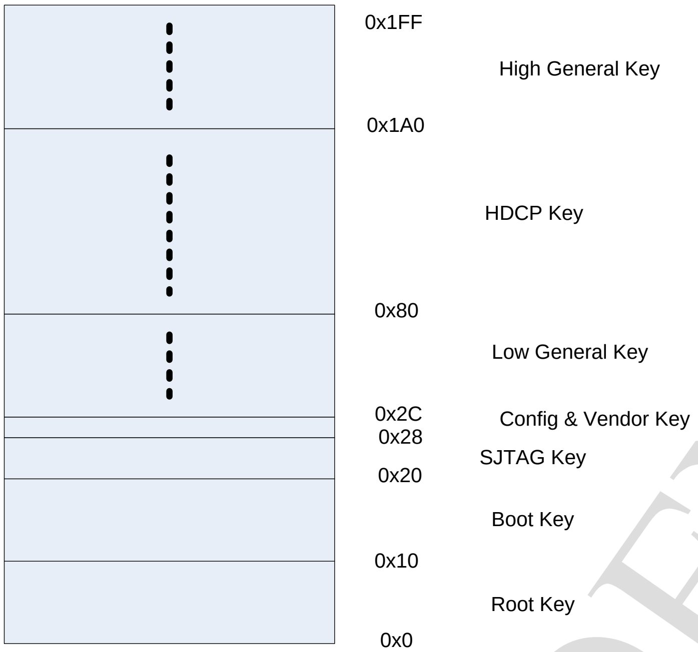
1.18.1. Overview

There is one on chip EFUSE, which provides 128-bit, 64-bit and one 32-bit electrical fuses for security application.

It features:

- 128-bit electrical fuses for root key
- 128-bit electrical fuses for boot key
- 64-bit electrical fuses for securiy JTAG
- 16-bit electrical fuses for chip configure application
- 16-bit electrical fues for vendors application

1.18.2. SID Block Diagram



1.18.3. Security System Register List

Module Name	Base Address	
SID	0x01C23800	

Register Name	Offset	Description
SID_RKEY0	0x00	Root Key[31:0]
SID_RKEY1	0x04	Root Key[63:32]
SID_RKEY2	0x08	Root Key[95:64]
SID_RKEY3	0x0c	Root Key[127:96]
SID_BKEY0	0x10	Boot Key[31:0]
SID_BKEY1	0x14	Boot Key[63:32]

Register Name	Offset	Description
SID_BKEY2	0x18	Boot Key[95:64]
SID_BKEY3	0x1c	Boot Key[127:96]
SID_JKEY0	0x20	Security JTAG key[31:0]
SID_JKEY1	0x24	Security JTAG key[63:32]
SID_CKEY	0x28	16-bit key for configuration and 16-bit for vendor application
SID_PRCTL	0x40	SID Program/Read Control Register
SID_PKEY	0x50	SID Program Key Value Register
SID_RKEY	0x60	SID Read Key Value Register

1.18.4. Security ID Register Description

1.18.4.1. SID ROOT KEY 0 REGISTER

Offset: 0x00			Register Name: SID_RKEY0 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	ROOT_KEY Securiy root key[31:0]

1.18.4.2. SID ROOT KEY 1 REGISTER

Offset: 0x04			Register Name: SID_RKEY1 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	ROOT_KEY Securiy root key[63:32]

1.18.4.3. SID ROOT KEY 2 REGISTER

Offset: 0x08			Register Name: SID_RKEY2 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	ROOT_KEY Securiy root key[95:64]

1.18.4.4. SID ROOT KEY 3 REGISTER

Offset: 0x0c			Register Name: SID_RKEY3 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	ROOT_KEY Securiy root key[127:96]

1.18.4.5. SID BOOT KEY 0 REGISTER

Offset: 0x10			Register Name: SID_BKEY0 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	BOOT_KEY Securiy boot key[31:0]

1.18.4.6. SID BOOT KEY 1 REGISTER

Offset: 0x14			Register Name: SID_BKEY1 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	BOOT_KRY Securiy boot key[63:32]

1.18.4.7. SID BOOT KEY 2 REGISTER

Offset: 0x18			Register Name: SID_BKEY2 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	BOOT_KRY Securiy boot key[95:64]

1.18.4.8. SID BOOT KEY 3 REGISTER

Offset: 0x1c			Register Name: SID_BKEY3 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	BOOT_KRY Securiy boot key[127:96]

1.18.4.9. SID SJTAG KEY 0 REGISTER

Offset: 0x20			Register Name: SID_JKEY0 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	JTAG_KEY Securiy JTAG key [31:0]

1.18.4.10. SID SJTAG KEY 1 REGISTER

Offset: 0x24			Register Name: SID_JKEY1 Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:0	R	x	JTAG_KEY Securiy JTAG key [63:31] When JTAG key read lock flag is off, the 64-bits JKEY value can be read out by CPU, else it is undefined.

1.18.4.11. SID COMMON KEY REGISTER

Offset: 0x28			Register Name: SID_CKEY Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
31:16	R	x	VENDOR_FIELD 16-bit key for vendor application
15:13	/	/	/
12	R	x	HDMI_KEY_LOCK HDMI HDCP key read lock flag 0: key value can be read out by CPU 1: key value can't be read out by CPU HDCP Data Address 0x80~0x19F.
11:6	R	x	/
5	R	x	BKEY_VALID_FLAG Boot key valid flag 0: Boot key invalid 1: Boot key valid When this field is '1', CPU would perform security boot after power up. This bit would be checked by bootrom.
4	R	x	BKEY_READ_LOCK Boot key read lock flag 0: key value can be read out by CPU 1: key value can't be read out by CPU
3	R	x	RKEY_READ_LOCK Root key read lock flag 0: key value can be read out by CPU 1: key value can't be read out by CPU
2	R	x	JKEY_READ_LOCK JTAG key read lock flag 0: key value can be read out by CPU 1: key value can't be read out by CPU
1	R	x	JTAG_AUTH_ONOFF JTAG Authentication on/off bit 0: JTAG security password check off

Offset: 0x28			Register Name: SID_CKEY Default Value: 0xXXXX_XXXX
Bit	**Read/Write**	**Default**	**Description**
			1: JTAG security password check on This bit is active only when JTAG function is enabled.
0	R	x	JTAG_ENA JTAG function enable/disable bit 0: JTAG function enable 1: JTAG function is closed and user can't use JTAG to debug

1.18.4.12. SID PROGRAM/READ CONTROL REGISTER

Offset: 0x40			Register Name: SID_PRCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:25	/	/	/
24:16	R/W	0	PG_INDEX Program index The index value of 8-bits electrical fuses hardware macrocell, and the lowest two bit must bt zero.
15:8	R/W	0	OP_LOCK Efuse Operation Lock The Read Start (Bit1) and Program Start (Bit0) only can be write when these bits (Bit[15:8]) set to 0xAC.
7:3	/	/	
2	R	x	HW_READ_STATUS Hardware Read Status 0: No Hardware Operation 1: Hardware Reading
1	R/W	0	READ_START Software Read Start Write '1' to start software read and automatically clear to '0' after read.
0	R/W	0	PG_START Software program start Write '1' to start software program and automatically clear to

Offset: 0x40			Register Name: SID_PRCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			‘0’ after program.

1.18.4.13. SID PROGRAM KEY VALUE REGISTER

Offset: 0x50			Register Name: SID_PKEY Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	PG_KEY_VALUE Program key value The CPU can write 32-bits value into this register for fuse by software.

1.18.4.14. SID READ KEY VALUE REGISTER

Offset: 0x60			Register Name: SID_RKEY Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	PG_KEY_VALUE Program key value The CPU can write 32-bits value into this register for fuse by software.

1.19. Port Controller

1.19.1. Port Description

The chip has several ports for multi-functional input/out pins. They are shown below:

Port A(PA): 18 input/output port
Port B(PB): 24 input/output port
Port C(PC): 25 input/output port
Port D(PD): 28 input/output port
Port E(PE) : 12 input/output port
Port F(PF) : 6 input/output port
Port G(PG) : 12 input/output port
Port H(PH) : 28 input/output port
Port I(PI) : 22 input/output port
Port S(PS) : 84 input/output port for DRAM controller

For various system configurations, these ports can be easily configured by software. All these ports (except PS) can be configured as GPIO if multiplexed functions not used. 32 external PIO interrupt sources are supported and interrupt mode can be configured by software.

1.19.2. Port Configuration Table

Port A(PA)	Multiplex Function Select				
PA0	ERXD3	SPI1_CS0	UART2_RTS	GRXD3	
PA1	ERXD2	SPI1_CLK	UART2_CTS	GRXD2	
PA2	ERXD1	SPI1_MOSI	UART2_TX	GRXD1	
PA3	ERXD0	SPI1_MISO	UART2_RX	GRXD0	
PA4	ETXD3	SPI1_CS1		GTXD3	
PA5	ETXD2	SPI3_CS0		GTXD2	
PA6	ETXD1	SPI3_CLK		GTXD1	
PA7	ETXD0	SPI3_MOSI		GTXD0	
PA8	ERXCK	SPI3_MISO		GRXCK	
PA9	ERXERR	SPI3_CS1		GNULL/ERXERR	I2S1_MCLK
PA10	ERXDV		UART1_TX	GRXCTL/RXDV	
PA11	EMDC		UART1_RX	GMDC	
PA12	EMDIO	UART6_TX	UART1_RTS	GMDIO	
PA13	ETXEN	UART6_RX	UART1_CTS	GTXCTL/ETXEN	
PA14	ETXCK	UART7_TX	UART1_DTR	GNULL/ETXCK	I2S1_BCLK
PA15	ECRS	UART7_RX	UART1_DSR	GTXCK/ECRS	I2S1_LRCK
PA16	ECOL	CAN_TX	UART1_DCD	GCLKIN/ECOL	I2S1_DO
PA17	ETXERR	CAN_RX	UART1_RING	GNULL/ETXERR	I2S1_DI

Port A(PA) Multiplex Function Select Table

Port B(PB)	Multiplex Function Select				
PB0	TWI0_SCK				
PB1	TWI0_SDA				
PB2	PWM0				
PB3	IR0_TX		SPDIF_MCLK		STANBYWFI
PB4	IR0_RX				
PB5	I2S_MCLK	AC97_MCLK			

Port B(PB)	Multiplex Function Select				
PB6	I2S_BCLK	AC97_BCLK			
PB7	I2S_LRCK	AC97_SYNC			
PB8	I2S_DO0	AC97_DO			
PB9	I2S_DO1				
PB10	I2S_DO2				
PB11	I2S_DO3				
PB12	I2S_DI	AC97_DI	SPDIF_DI		
PB13	SPI2_CS1		SPDIF_DO		
PB14	SPI2_CS0	JTAG_MS0			
PB15	SPI2_CLK	JTAG_CK0			
PB16	SPI2_MOSI	JTAG_DO0			
PB17	SPI2_MISO	JTAG_DI0			
PB18	TWI1_SCK				
PB19	TWI1_SDA				
PB20	TWI2_SCK				
PB21	TWI2_SDA				
PB22	UART0_TX	IR1_TX			
PB23	UART0_RX	IR1_RX			

Port B(PB) Multiplex Function Select Table

Port C(PC)	Multiplex Function Select				
PC0	NWE#	SPI0_MOSI			
PC1	NALE	SPI0_MISO			
PC2	NCLE	SPI0_CLK			
PC3	NCE1				
PC4	NCE0				
PC5	NRE#				
PC6	NRB0	SDC2_CMD			
PC7	NRB1	SDC2_CLK			
PC8	NDQ0	SDC2_D0			
PC9	NDQ1	SDC2_D1			
PC10	NDQ2	SDC2_D2			

Port C(PC)	Multiplex Function Select				
PC11	NDQ3	SDC2_D3			
PC12	NDQ4				
PC13	NDQ5				
PC14	NDQ6				
PC15	NDQ7				
PC16	NWP				
PC17	NCE2				
PC18	NCE3				
PC19	NCE4	SPI2_CS0			EINT12
PC20	NCE5	SPI2_CLK			EINT13
PC21	NCE6	SPI2_MOSI			EINT14
PC22	NCE7	SPI2_MISO			EINT15
PC23		SPI0_CS0			
PC24	NDQS				

Port C(PC) Multiplex Function Select Table

Port D(PD)	Multiplex Function Select				
PD0	LCD0_D0	LVDS0_VP0			
PD1	LCD0_D1	LVDS0_VN0			
PD2	LCD0_D2	LVDS0_VP1			
PD3	LCD0_D3	LVDS0_VN1			
PD4	LCD0_D4	LVDS0_VP2			
PD5	LCD0_D5	LVDS0_VN2			
PD6	LCD0_D6	LVDS0_VPC			
PD7	LCD0_D7	LVDS0_VNC			
PD8	LCD0_D8	LVDS0_VP3			
PD9	LCD0_D9	LVDS0_VN3			
PD10	LCD0_D10	LVDS1_VP0			
PD11	LCD0_D11	LVDS1_VN0			
PD12	LCD0_D12	LVDS1_VP1			
PD13	LCD0_D13	LVDS1_VN1			
PD14	LCD0_D14	LVDS1_VP2			

Port D(PD)	Multiplex Function Select				
PD15	LCD0_D15	LVDS1_VN2			
PD16	LCD0_D16	LVDS1_VPC			
PD17	LCD0_D17	LVDS1_VNC			
PD18	LCD0_D18	LVDS1_VP3			
PD19	LCD0_D19	LVDS1_VN3			
PD20	LCD0_D20	CSI1_MCLK			
PD21	LCD0_D21	SMC_VPPEN			
PD22	LCD0_D22	SMC_VPPPP			
PD23	LCD0_D23	SMC_DET			
PD24	LCD0_CLK	SMC_VCCEN			
PD25	LCD0_DE	SMC_RST			
PD26	LCD0_HSYNC	SMC_SLK			
PD27	LCD0_VSYNC	SMC_SDA			

Port D(PD) Multiplex Function Select Table

Port E(PE)	Multiplex Function Select				
PE0	TS0_CLK	CSI0_PCLK			
PE1	TS0_ERR	CSI0_MCLK			
PE2	TS0_SYNC	CSI0_HSYNC			
PE3	TS0_DLVD	CSI0_VSYNC			
PE4	TS0_D0	CSI0_D0			
PE5	TS0_D1	CSI0_D1			
PE6	TS0_D2	CSI0_D2			
PE7	TS0_D3	CSI0_D3			
PE8	TS0_D4	CSI0_D4			
PE9	TS0_D5	CSI0_D5			
PE10	TS0_D6	CSI0_D6			
PE11	TS0_D7	CSI0_D7			

Port E(PE) Multiplex Function Select Table

Port F(PF)	Multiplex Function Select				
PF0	SDC0_D1		JTAG_MS1		

Port F(PF)	Multiplex Function Select				
PF1	SDC0_D0		JTAG_DI1		
PF2	SDC0_CLK		UART0_TX		
PF3	SDC0_CMD		JTAG_DO1		
PF4	SDC0_D3		UART0_RX		
PF5	SDC0_D2		JTAG_CK1		

Port F(PF) Multiplex Function Select Table

Port G(PG)	Multiplex Function Select				
PG0	TS1_CLK	CSI1_PCLK	SDC1_CMD		
PG1	TS1_ERR	CSI1_MLCK	SDC1_CLK		
PG2	TS1_SYNC	CSI1_HSYNC	SDC1_D0		
PG3	TS1_DVLD	CSI1_VSYNC	SDC1_D1		
PG4	TS1_D0	CSI1_D0	SDC1_D2	CSI0_D8	
PG5	TS1_D1	CSI1_D1	SDC1_D3	CSI0_D9	
PG6	TS1_D2	CSI1_D2	UART3_TX	CSI0_D10	
PG7	TS1_D3	CSI1_D3	UART3_RX	CSI0_D11	
PG8	TS1_D4	CSI1_D4	UART3_RTS	CSI0_D12	
PG9	TS1_D5	CSI1_D5	UART3_CTS	CSI0_D13	
PG10	TS1_D6	CSI1_D6	UART4_TX	CSI0_D14	
PG11	TS1_D7	CSI1_D7	UART4_RX	CSI0_D15	

Port G(PG) Multiplex Function Select Table

Port H(PH)	Multiplex Function Select					
PH0	LCD1_D0		UART3_TX		EINT0	CSI1_D0
PH1	LCD1_D1		UART3_RX		EINT1	CSI1_D1
PH2	LCD1_D2		UART3_RTS		EINT2	CSI1_D2
PH3	LCD1_D3		UART3_CTS		EINT3	CSI1_D3
PH4	LCD1_D4		UART4_TX		EINT4	CSI1_D4
PH5	LCD1_D5		UART4_RX		EINT5	CSI1_D5
PH6	LCD1_D6		UART5_TX	MS_BS	EINT6	CSI1_D6

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Port H(PH)	Multiplex Function Select					
PH7	LCD1_D7		UART5_RX	MS_CLK	EINT7	CSI1_D7
PH8	LCD1_D8	ERXD3	KP_IN0	MS_D0	EINT8	CSI1_D8
PH9	LCD1_D9	ERXD2	KP_IN1	MS_D1	EINT9	CSI1_D9
PH10	LCD1_D10	ERXD1	KP_IN2	MS_D2	EINT10	CSI1_D10
PH11	LCD1_D11	ERXD0	KP_IN3	MS_D3	EINT11	CSI1_D11
PH12	LCD1_D12		PS2_SCK1		EINT12	CSI1_D12
PH13	LCD1_D13		PS2_SDA1	SMC_RST	EINT13	CSI1_D13
PH14	LCD1_D14	ETXD3	KP_IN4	SMC_VPPEN	EINT14	CSI1_D14
PH15	LCD1_D15	ETXD2	KP_IN5	SMC_VPPPP	EINT15	CSI1_D15
PH16	LCD1_D16	ETXD1	KP_IN6	SMC_DET	EINT16	CSI1_D16
PH17	LCD1_D17	ETXD0	KP_IN7	SMC_VCCEN	EINT17	CSI1_D17
PH18	LCD1_D18	ERXCK	KP_OUT0	SMC_SLK	EINT18	CSI1_D18
PH19	LCD1_D19	ERXERR	KP_OUT1	SMC_SDA	EINT19	CSI1_D19
PH20	LCD1_D20	ERXDV	CAN_TX		EINT20	CSI1_D20
PH21	LCD1_D21	EMDC	CAN_RX		EINT21	CSI1_D21
PH22	LCD1_D22	EMDIO	KP_OUT2	SDC1_CMD		CSI1_D22
PH23	LCD1_D23	ETXEN	KP_OUT3	SDC1_CLK		CSI1_D23
PH24	LCD1_CLK	ETXCK	KP_OUT4	SDC1_D0		CSI1_PCLK
PH25	LCD1_DE	ECRS	KP_OUT5	SDC1_D1		CSI1_FIELD
PH26	LCD1_HSYNC	ECOL	KP_OUT6	SDC1_D2		CSI1_HSYNC
PH27	LCD1_VSYNC	ETXERR	KP_OUT7	SDC1_D3		CSI1_VSYNC

Port H(PH) Multiplex Function Select Table

Port I(PI)	Multiplex Function Select				
PI0		TWI3_SCK			
PI1		TWI3_SDA			
PI2		TWI4_SCK			
PI3	PWM1	TWI4_SDA			
PI4	SDC3_CMD				
PI5	SDC3_CLK				

Port I(PI)	Multiplex Function Select				
PI6	SDC3_D0				
PI7	SDC3_D1				
PI18	SDC3_D2				
PI19	SDC3_D3				
PI10	SPI0_CS0	UART5_TX		EINT22	
PI11	SPI0_CLK	UART5_RX		EINT23	
PI12	SPI0_MOSI	UART6_TX	CLK_OUT_A	EINT24	
PI13	SPI0_MISO	UART6_RX	CLK_OUT_B	EINT25	
PI14	SPI0_CS1	PS2_SCK1	TCLKIN0	EINT26	
PI15	SPI1_CS1	PS2_SDA1	TCLKIN1	EINT27	
PI16	SPI1_CS0	UART2_RTS		EINT28	
PI17	SPI1_CLK	UART2_CTS		EINT29	
PI18	SPI1_MOSI	UART2_TX		EINT30	
PI19	SPI1_MISO	UART2_RX		EINT31	
PI20	PS2_SCK0	UART7_TX	HSCL		
PI21	PS2_SDA0	UART7_RX	HSDA		

Port I(PI) Multiplex Function Select Table

1.19.3. Port Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 9)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 9)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 9)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 9)

Register Name	Offset	Description
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 9)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 9)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 9)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 9)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 9)
PIO_INT_CFG0	0x200	PIO Interrrupt Configure Register 0
PIO_INT_CFG1	0x204	PIO Interrrupt Configure Register 1
PIO_INT_CFG2	0x208	PIO Interrrupt Configure Register 2
PIO_INT_CFG3	0x20C	PIO Interrrupt Configure Register 3
PIO_INT_CTL	0x210	PIO Interrupt Control Register
PIO_INT_STA	0x214	PIO Interrupt Status Register
PIO_INT_DEB	0x218	PIO Interrupt Debounce Register

1.19.4. Port Register Description

1.19.4.1. PA CONFIGURE REGISTER 0

Offset: 0x00			**Register Name: PA_CFG0** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PA7_SELECT 000: Input 001: Output 010: ETXD0 011: SPI3_MOSI 100: Reserved 101: GTXD0 110: Reserved 111: Reserved
27	/	/	Reserved
26:24	R/W	0	PA6_SELECT 000: Input 001: Output 010: ETXD1 011: SPI3_CLK

Offset: 0x00			Register Name: PA_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			100: Reserved 101: GTXD1 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PA5_SELECT 000: Input 001: Output 010: ETXD2 011: SPI3_CS0 100: Reserved 101: GTXD2 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PA4_SELECT 000: Input 001: Output 010: ETXD3 011: SPI1_CS1 100: Reserved 101: GTXD3 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PA3_SELECT 000: Input 001: Output 010: ERXD0 011: SPI1_MISO 100: UART2_RX 101: GRXD0 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PA2_SELECT 000: Input 001: Output 010:ERXD1 011: SPI1_MOSI 100: UART2_TX 101: GRXD1 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PA1_SELECT 000: Input 001: Output 010: ERXD2 011: SPI1_CLK 100: UART2_CTS 101: GRXD2 110: Reserved 111: Reserved
3	/	/	Reserved

Offset: 0x00			Register Name: PA_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
2:0	R/W	0	PA0_SELECT 000: Input 001: Output 010: ERXD3 011: SPI1_CS0 100: UART2_RTS 101: GRXD3 110: Reserved 111: Reserved

1.19.4.2. PA CONFIGURE REGISTER 1

Offset: 0x04			Register Name: PA_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PA15_SELECT 000: Input 001: Output 010: ECRS 011: UART7_RX 100: UART1_DSR 101: GTXCK/ECRS 110: I2S1_LRCK 111: Reserved
27	/	/	/
26:24	R/W	0	PA14_SELECT 000: Input 001: Output 010:ETXCK 011: UART7_TX 100: UART1_DTR 101: GNULL/ETXCK 110: I2S1_BCLK 111: Reserved
23	/	/	/
22:20	R/W	0	PA13_SELECT 000: Input 001: Output 010:ETXEN 011: UART6_RX 100: UART1_CTS 101: GTXCTL/ETXEN 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PA12_SELECT 000: Input 001: Output

Offset: 0x04			Register Name: PA_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			010:EMDIO 011: UART6_TX 100: UART1_RTS 101: GMDIO 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PA11_SELECT 000: Input 001: Output 010: EMDC 011: Reserved 100: UART1_RX 101: GMDC 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PA10_SELECT 000: Input 001: Output 010:ERXDV 011: Reserved 100: UART1_TX 101: GRXCTL/ERXDV 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PA9_SELECT 000: Input 001: Output 010: ERXERR 011: SPI3_CS1 100: Reserved 101: GNULL/ERXERR 110: I2S1_MCLK 111: Reserved
3	/	/	/
2:0	R/W	0	PA8_SELECT 000: Input 001: Output 010:ERXCK 011: SPI3_MISO 100: Reserved 101: GRXCK 110: Reserved 111: Reserved

1.19.4.3. PA CONFIGURE REGISTER 2

Offset: 0x08	Register Name: PA_CFG2 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:7	/	/	/
6:4	R/W	0	PA17_SELECT 000: Input 001: Output 010: ETXERR 011: CAN_RX 100: UART1_RING 101: GNULL/ETXERR 110: I2S1_DI 111: Reserved
3	/	/	/
2:0	R/W	0	PA16_SELECT 000: Input 001: Output 010: ECOL 011: CAN_TX 100: UART1_DCD 101: GCLKIN/ECOL 110: I2S1_DO 111: Reserved

1.19.4.4. PA CONFIGURE REGISTER 3

Offset: 0x0C			Register Name: PA_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.5. PA DATA REGISTER

Offset: 0x10			Register Name: PA_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
17:0	R/W	0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.6. PA MULTI-DRIVING REGISTER 0

Offset: 0x14			Register Name: PA_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.7. PA MULTI-DRIVING REGISTER 1

Offset: 0x18			Register Name: PA_DRV1 Default Value: 0x0000_0005
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.8. PA PULL REGISTER 0

Offset: 0x1C			Register Name: PA_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.9. PA PULL REGISTER 1

Offset: 0x20			Register Name: PA_PULL1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

1.19.4.10. PB CONFIGURE REGISTER 0

Offset: 0x24			Register Name: PB_CFG0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0	PB7_SELECT 000: Input 001: Output 010: I2S_LRCK 011: AC97_SYNC 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PB6_SELECT 000: Input 001: Output 010: I2S_BCLK 011: AC97_BCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PB5_SELECT 000: Input 001: Output 010: I2S_MCLK 011: AC97_MCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/

Offset: 0x24			Register Name: PB_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
18:16	R/W	0	PB4_SELECT 000: Input 001: Output 010: IR0_RX 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PB3_SELECT 000: Input 001: Output 010: IR0_TX 011: Reserved 100: SPDIF_MCLK 101: Reserved 110: STANBYWFI 111: Reserved
11	/	/	/
10:8	R/W	0	PB2_SELECT 000: Input 001: Output 010: PWM0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PB1_SELECT 000: Input 001: Output 010: TWI0_SDA 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PB0_SELECT 000: Input 001: Output 010: TWI0_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.11. PB CONFIGURE REGISTER 1

Offset: 0x28			Register Name: PB_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PB15_SELECT 000: Input 001: Output 010: SPI2_CLK 011: JTAG_CK0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PB14_SELECT 000: Input 001: Output 010: SPI2_CS0 011: JTAG_MS0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PB13_SELECT 000: Input 001: Output 010: SPI2_CS1 011: Reserved 100: SPDIF_DO 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PB12_SELECT 000: Input 001: Output 010: I2S_DI 011: AC97_DI 100: SPDIF_DI 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PB11_SELECT 000: Input 001: Output 010: I2S_DO3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PB10_SELECT

Offset: 0x28			Register Name: PB_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			000: Input 001: Output 010: I2S_DO2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PB9_SELECT 000: Input 001: Output 010: I2S_DO1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PB8_SELECT 000: Input 001: Output 010: I2S_DO0 011: AC97_DO 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.12. PB CONFIGURE REGISTER 2

Offset: 0x2C			Register Name: PB_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PB23_SELECT 000: Input 001: Output 010: UART0_RX 011: IR1_RX 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PB22_SELECT 000: Input 001: Output 010: UART0_TX 011: IR1_TX

Offset: 0x2C			Register Name: PB_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	Reserved
22:20	R/W	0	PB21_SELECT 000: Input 001: Output 010: TWI2_SDA 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PB20_SELECT 000: Input 001: Output 010: TWI2_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PB19_SELECT 000: Input 001: Output 010: TWI1_SDA 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PB18_SELECT 000: Input 001: Output 010: TWI1_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PB17_SELECT 000: Input 001: Output 010: SPI2_MISO 011: JTAG_DI0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/

Offset: 0x2C			Register Name: PB_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
2:0	R/W	0	PB16_SELECT 000: Input 001: Output 010: SPI2_MOSI 011: JTAG_DO0 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.13. PB CONFIGURE REGISTER 3

Offset: 0x30			Register Name: PB_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.14. PB DATA REGISTER

Offset: 0x34			Register Name: PB_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.15. PB MULTI-DRIVING REGISTER 0

Offset: 0x38	Register Name: PB_DRV0 Default Value: 0x5555_5555

Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.16. PB MULTI-DRIVING REGISTER 1

Offset: 0x3C			Register Name: PB_DRV1 Default Value: 0x0000_5555
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 16~23) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.17. PB PULL REGISTER 0

Offset: 0x40			Register Name: PB_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.18. PB PULL REGISTER 1

Offset: 0x44			Register Name: PB_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

Offset: 0x44			Register Name: PB_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 16~23) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

1.19.4.19. PC CONFIGURE REGISTER 0

Offset: 0x48			Register Name: PC_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PC7_SELECT 000: Input 001: Output 010: NRB1 011: SDC2_CLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PC6_SELECT 000: Input 001: Output 010: NRB0 011: SDC2_CMD 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PC5_SELECT 000: Input 001: Output 010: NRE# 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PC4_SELECT 000: Input 001: Output

Offset: 0x48			Register Name: PC_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			010: NCE0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PC3_SELECT 000: Input 001: Output 010: NCE1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PC2_SELECT 000: Input 001: Output 010: NCLE 011: SPI0_CLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PC1_SELECT 000: Input 001: Output 010: NALE 011: SPI0_MISO 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PC0_SELECT 000: Input 001: Output 010: NWE 011: SPI0_MOSI 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.20. PC CONFIGURE REGISTER 1

Offset: 0x4C	Register Name: PC_CFG1 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0	PC15_SELECT 000: Input 001: Output 010: NDQ7 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PC14_SELECT 000: Input 001: Output 010: NDQ6 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PC13_SELECT 000: Input 001: Output 010: NDQ5 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PC12_SELECT 000: Input 001: Output 010: NDQ4 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PC11_SELECT 000: Input 001: Output 010: NDQ3 011: SDC2_D3 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PC10_SELECT 000: Input 001: Output 010: NDQ2 011: SDC2_D2 100: Reserved 101: Reserved

Offset: 0x4C			Register Name: PC_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PC9_SELECT 000: Input 001: Output 010: NDQ1 011: SDC2_D1 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PC8_SELECT 000: Input 001: Output 010: NDQ0 011: SDC2_D0 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.21. PC CONFIGURE REGISTER 2

Offset: 0x50			Register Name: PC_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PC23_SELECT 000: Input 001: Output 010: Reserved 011: SPI0_CS0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
17	/	/	/
26:24	R/W	0	PC22_SELECT 000: Input 001: Output 010: NCE7 011: SPI2_MISO 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/

Offset: 0x50			Register Name: PC_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
22:20	R/W	0	PC21_SELECT 000: Input 001: Output 010: NCE6 011: SPI2_MOSI 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PC20_SELECT 000: Input 001: Output 010: NCE5 011: SPI2_CLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PC19_SELECT 000: Input 001: Output 010: NCE4 011: SPI2_CS0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PC18_SELECT 000: Input 001: Output 010: NCE3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PC17_SELECT 000: Input 001: Output 010: NCE2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PC16_SELECT 000: Input 001: Output 010: NWP 011: Reserved

Offset: 0x50			Register Name: PC_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
			100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.22. PC CONFIGURE REGISTER 3

Offset: 0x54			Register Name: PC_CFG3 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:3	/	/	/
2:0	R/W	0	PC24_SELECT 000: Input 001: Output 010: NDQS 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.23. PC DATA REGISTER

Offset: 0x58			Register Name: PC_DAT Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:24	/	/	/
23:0	R/W	0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.24. PC MULTI-DRIVING REGISTER 0

Offset: 0x5C			Register Name: PC_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving_SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.25. PC MULTI-DRIVING REGISTER 1

Offset: 0x60			Register Name: PC_DRV1 Default Value: 0x0001_5555
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~24) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.26. PC PULL REGISTER 0

Offset: 0x64			Register Name: PC_PULL0 Default Value: 0x0000_5140
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0000_5140	PC_PULL PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.27. PC PULL REGISTER 1

Offset: 0x68			Register Name: PC_PULL1 Default Value: 0x0000_4016
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x0000_4016	PC_PULL PC[n] Pull-up/down Select (n = 16~24) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.28. PD CONFIGURE REGISTER 0

Offset: 0x6C			Register Name: PD_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PD7_SELECT 000: Input 001: Output 010: LCD0_D7 011: LVDS0_VNC 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	Reserved
26:24	R/W	0	PD6_SELECT 000: Input 001: Output 010: LCD0_D6 011: LVDS0_VPC 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PD5_SELECT 000: Input 001: Output 010: LCD0_D5 011: LVDS0_VN2 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/

Offset: 0x6C			Register Name: PD_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
18:16	R/W	0	PD4_SELECT 000: Input 001: Output 010: LCD0_D4 011: LVDS0_VP2 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PD3_SELECT 000: Input 001: Output 010: LCD0_D3 011: LVDS0_VN1 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PD2_SELECT 000: Input 001: Output 010: LCD0_D2 011: LVDS0_VP1 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PD1_SELECT 000: Input 001: Output 010: LCD0_D1 011: LVDS0_VN0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PD0_SELECT 000: Input 001: Output 010: LCD0_D0 011: LVDS0_VP0 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.29. PD CONFIGURE REGISTER 1

Offset: 0x70			Register Name: PD_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PD15_SELECT 000: Input 001: Output 010: LCD0_D15 011: LVDS1_VN2 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PD14_SELECT 000: Input 001: Output 010: LCD0_D14 011: LVDS1_VP2 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PD13_SELECT 000: Input 001: Output 010: LCD0_D13 011: LVDS1_VN1 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PD12_SELECT 000: Input 001: Output 010: LCD0_D12 011: LVDS1_VP1 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PD11_SELECT 000: Input 001: Output 010: LCD0_D11 011: LVDS1_VN0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PD10_SELECT

Offset: 0x70			Register Name: PD_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			000: Input 001: Output 010: LCD0_D10 011: LVDS1_VP0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PD9_SELECT 000: Input 001: Output 010: LCD0_D9 011: LVDS0_VN3 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PD8_SELECT 000: Input 001: Output 010: LCD0_D8 011: LVDS0_VP3 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.30. PD CONFIGURE REGISTER 2

Offset: 0x74			Register Name: PD_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PD23_SELECT 000: Input 001: Output 010: LCD0_D23 011: SMC_DET 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PD22_SELECT 000: Input 001: Output 010: LCD0_D22 011: SMC_VPPPP

Offset: 0x74			Register Name: PD_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PD21_SELECT 000: Input 001: Output 010: LCD0_D21 011: SMC_VPPEN 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PD20_SELECT 000: Input 001: Output 010: LCD0_D20 011: CSI1_MCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PD19_SELECT 000: Input 001: Output 010: LCD0_D19 011: LVDS1_VN3 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PD18_SELECT 000: Input 001: Output 010: LCD0_D18 011: LVDS1_VP3 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PD17_SELECT 000: Input 001: Output 010: LCD0_D17 011: LVDS1_VNC 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/

Offset: 0x74			Register Name: PD_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
2:0	R/W	0	PD16_SELECT 000: Input 001: Output 010: LCD0_D16 011: LVDS1_VPC 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.31. PD CONFIGURE REGISTER 3

Offset: 0x78			Register Name: PD_CFG3 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:15	/	/	/
14:12	R/W	0	PD27_SELECT 000: Input 001: Output 010: LCD0_ VSYNC 011: SMC_SDA 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	Reserved
10:8	R/W	0	PD26_SELECT 000: Input 001: Output 010: LCD0_ HSYNC 011: SMC_SLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PD25_SELECT 000: Input 001: Output 010: LCD0_ DE 011: SMC_RST 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PD24_SELECT 000: Input 001: Output

Offset: 0x78			Register Name: PD_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			010: LCD0_CLK 011: SMC_VCCEN 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.32. PD DATA REGISTER

Offset: 0x7C			Register Name: PD_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.33. PD MULTI-DRIVING REGISTER 0

Offset: 0x80			Register Name: PD_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.34. PD MULTI-DRIVING REGISTER 1

Offset: 0x84	Register Name: PD_DRV1 Default Value: 0x0055_5555

Bit	Read/Write	Default	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.35. PD PULL REGISTER 0

Offset: 0x88			Register Name: PD_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.36. PD PULL REGISTER 1

Offset: 0x8C			Register Name: PD_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

1.19.4.37. PE CONFIGURE REGISTER 0

Offset: 0x90	Register Name: PE_CFG0 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0	PE7_SELECT 000: Input 001: Output 010: TS0_D3 011: CSI0_D3 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PE6_SELECT 000: Input 001: Output 010: TS0_D2 011: CSI0_D2 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PE5_SELECT 000: Input 001: Output 010: TS0_D1 011: CSI0_D1 100: SMC_VPPEN 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PE4_SELECT 000: Input 001: Output 010: TS0_D0 011: CSI0_D0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PE3_SELECT 000: Input 001: Output 010: TS0_DVLD 011: CSI0_VSYNC 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PE2_SELECT 000: Input 001: Output 010: TS0_SYNC 011: CSI0_HSYNC 100: Reserved 101: Reserved

Offset: 0x90			Register Name: PE_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PE1_SELECT 000: Input 001: Output 010: TS0_ERR 011: CSI0_CK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PE0_SELECT 000: Input 001: Output 010: TS0_CLK 011: CSI0_PCK 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.38. PE CONFIGURE REGISTER 1

Offset: 0x94			Register Name: PE_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	0	PE11_SELECT 000: Input 001: Output 010: TS0_D7 011: CSI0_D7 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PE10_SELECT 000: Input 001: Output 010: TS0_D6 011: CSI0_D6 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/

Offset: 0x94			Register Name: PE_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
6:4	R/W	0	PE9_SELECT 000: Input 001: Output 010: TS0_D5 011: CSI0_D5 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PE8_SELECT 000: Input 001: Output 010: TS0_D4 011: CSI0_D4 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.39. PE CONFIGURE REGISTER 2

Offset: 0x98			Register Name: PE_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.40. PE CONFIGURE REGISTER 3

Offset: 0x98			Register Name: PE_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.41. PE DATA REGISTER

Offset: 0xA0	Register Name: PE_DAT Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:12	/	/	/
11:0	R/W	0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.42. PE MULTI-DRIVING REGISTER 0

Offset: 0xA4			Register Name: PE_DRV0 Default Value: 0x0055_5555
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.43. PE MULTI-DRIVING REGISTER 1

Offset: 0xA8			Register Name: PE_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.44. PE PULL REGISTER 0

Offset: 0xAC			Register Name: PE_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/

Offset: 0xAC			Register Name: PE_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~11)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.45. PE PULL REGISTER 1

Offset: 0xB0			Register Name: PE_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.46. PF CONFIGURE REGISTER 0

Offset: 0xB4			Register Name: PF_CFG0 Default Value: 0x0040_4044
Bit	**Read/Write**	**Default**	**Description**
31:23	/	/	/
22:20	R/W	0x4	PF5_SELECT 000: Input 001: Output 010: SDC0_D2 011: Reserved 100: JTAG_CK1 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PF4_SELECT 000: Input 001: Output 010: SDC0_D3 011: Reserved 100: UART0_RX 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0x4	PF3_SELECT

Offset: 0xB4			Register Name: PF_CFG0 Default Value: 0x0040_4044
Bit	**Read/Write**	**Default**	**Description**
			000: Input 001: Output 010: SDC0_CMD 011: Reserved 100: JTAG_DO1 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PF2_SELECT 000: Input 001: Output 010: SDC0_CLK 011: Reserved 100: UART0_TX 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0x4	PF1_SELECT 000: Input 001: Output 010: SDC0_D0 011: Reserved 100: JTAG_DI1 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0x4	PF0_SELECT 000: Input 001: Output 010: SDC0_D1 011: Reserved 100: JTAG_MS1 101: Reserved 110: Reserved 111: Reserved

1.19.4.47. PF CONFIGURE REGISTER 1

Offset: 0xB8			Register Name: PF_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.48. PF CONFIGURE REGISTER 2

Offset: 0xBC			Register Name: PF_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.49. PF CONFIGURE REGISTER 3

Offset: 0xC0			Register Name: PF_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.50. PF DATA REGISTER

Offset: 0xC4			Register Name: PF_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5:0	R/W	0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.51. PF MULTI-DRIVING REGISTER 0

Offset: 0xC8			Register Name: PF_DRV0 Default Value: 0x0000_0555
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/

Offset: 0xC8			Register Name: PF_DRV0 Default Value: 0x0000_0555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~5)	R/W	0x1	PF_DRV PF[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.52. PF MULTI-DRIVING REGISTER 1

Offset: 0xCC			Register Name: PF_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/

1.19.4.53. PF PULL REGISTER 0

Offset: 0xD0			Register Name: PF_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~5) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.54. PF PULL REGISTER 1

Offset: 0xD4			Register Name: PF_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

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1.19.4.55. PG CONFIGURE REGISTER 0

Offset: 0xD8			Register Name: PG_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PG7_SELECT 000: Input 001: Output 010: TS1_D3 011: CSI1_D3 100: UART3_RX 101: CSI0_D11 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PG6_SELECT 000: Input 001: Output 010: TS1_D2 011: CSI1_D2 100: UART3_TX 101: CSI0_D10 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PG5_SELECT 000: Input 001: Output 010: TS1_D1 011: CSI1_D1 100: SDC1_D3 101: CSI0_D9 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PG4_SELECT 000: Input 001: Output 010:TS1_D0 011: CSI1_D0 100: SDC1_D2 101: CSI0_D8 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PG3_SELECT 000: Input 001: Output 010: TS1_DVLD 011: CSI1_VSYNC 100: SDC1_D1 101: Reserved

Offset: 0xD8			Register Name: PG_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PG2_SELECT 000: Input 001: Output 010: TS1_SYNC 011: CSI1_HSYNC 100: SDC1_D0 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PG1_SELECT 000: Input 001: Output 010: TS1_ERR 011: CSI1_CK 100: SDC1_CLK 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PG0_SELECT 000: Input 001: Output 010: TS1_CLK 011: CSI1_PCK 100: SDC1_CMD 101: Reserved 110: Reserved 111: Reserved

1.19.4.56. PG CONFIGURE REGISTER 1

Offset: 0xDC			Register Name: PG_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	0	PG11_SELECT 000: Input 001: Output 010: TS1_D7 011: CSI1_D7 100: UART4_RX 101: CSI0_D15 110: Reserved 111: Reserved
11	/	/	/

Offset: 0xDC			Register Name: PG_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
10:8	R/W	0	PG10_SELECT 000: Input 001: Output 010: TS1_D6 011: CSI1_D6 100: UART4_TX 101: CSI0_D14 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PG9_SELECT 000: Input 001: Output 010:TS1_D5 011: CSI1_D5 100: UART3_CTS 101: CSI0_D13 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PG8_SELECT 000: Input 001: Output 010: TS1_D4 011: CSI1_D4 100: UART3_RTS 101: CSI0_D12 110: Reserved 111: Reserved

1.19.4.57. PG CONFIGURE REGISTER 2

Offset: 0xE0			Register Name: PG_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.58. PG CONFIGURE REGISTER 3

Offset: 0xE4			Register Name: PG_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

Offset: 0xE4			Register Name: PG_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.59. PG DATA REGISTER

Offset: 0xE8			Register Name: PG_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:0	R/W	0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.60. PG MULTI-DRIVING REGISTER 0

Offset: 0xEC			Register Name: PG_DRV0 Default Value: 0x0555_5555
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PG_DRV PG[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.61. PG MULTI-DRIVING REGISTER 1

Offset: 0xF0	Register Name: PG_DRV1 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:24	/	/	/

1.19.4.62. PG PULL REGISTER 0

Offset: 0xF4			Register Name: PG_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.63. PG PULL REGISTER 1

Offset: 0xF8			Register Name: PG_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.64. PH CONFIGURE REGISTER 0

Offset: 0xFC			Register Name: PH_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PH7_SELECT 000: Input 001: Output 010: LCD1_D7 011: Reserved 100: UART5_RX 101: MS_CLK

Offset: 0xFC			Register Name: PH_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			110: EINT7 111: CSI1_D7
27	/	/	/
26:24	R/W	0	PH6_SELECT 000: Input 001: Output 010: LCD1_D6 011: Reserved 100: UART5_TX 101: MS_BS 110: EINT6 111: CSI1_D6
23	/	/	/
22:20	R/W	0	PH5_SELECT 000: Input 001: Output 010: LCD1_D5 011: Reserved 100: UART4_RX 101: Reserved 110: EINT5 111: CSI1_D5
19	/	/	/
18:16	R/W	0	PH4_SELECT 000: Input 001: Output 010: LCD1_D4 011: Reserved 100: UART4_TX 101: Reserved 110: EINT4 111: CSI1_D4
15	/	/	/
14:12	R/W	0	PH3_SELECT 000: Input 001: Output 010: LCD1_D3 011: Reserved 100: UART3_CTS 101: Reserved 110: EINT3 111: CSI1_D3
11	/	/	/
10:8	R/W	0	PH2_SELECT 000: Input 001: Output 010: LCD1_D2 011: Reserved 100: UART3_RTS 101: Reserved 110: EINT2 111: CSI1_D2
7	/	/	/
6:4	R/W	0	PH1_SELECT

Offset: 0xFC			Register Name: PH_CFG0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
			000: Input 001: Output 010: LCD1_D1 011: Reserved 100: UART3_RX 101: Reserved 110: EINT1 111: CSI1_D1
3	/	/	/
2:0	R/W	0	PH0_SELECT 000: Input 001: Output 010: LCD1_D0 011: Reserved 100: UART3_TX 101: Reserved 110: EINT0 111: CSI1_D0

1.19.4.65. PH CONFIGURE REGISTER 1

Offset: 0x100			Register Name: PH_CFG1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0	PH15_SELECT 000: Input 001: Output 010: LCD1_D15 011: ETXD2 100: KP_IN5 101: SMC_VPPPP 110: EINT15 111: CSI1_D15
27	/	/	/
26:24	R/W	0	PH14_SELECT 000: Input 001: Output 010: LCD1_D14 011: ETXD3 100: KP_IN4 101: SMC_VPPEN 110: EINT14 111: CSI1_D14
23	/	/	/
22:20	R/W	0	PH13_SELECT 000: Input 001: Output 010: LCD1_D13 011: Reserved

Offset: 0x100			Register Name: PH_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			100: PS2_SDA1 101: SMC_RST 110: EINT13 111: CSI1_D13
19	/	/	/
18:16	R/W	0	PH12_SELECT 000: Input 001: Output 010: LCD1_D12 011: Reserved 100: PS2_SCK1 101: Reserved 110: EINT12 111: CSI1_D12
15	/	/	/
14:12	R/W	0	PH11_SELECT 000: Input 001: Output 010: LCD1_D11 011: ERXD0 100: KP_IN3 101: MS_D3 110: EINT11 111: CSI1_D11
11	/	/	/
10:8	R/W	0	PH10_SELECT 000: Input 001: Output 010: LCD1_D10 011: ERXD1 100: KP_IN2 101: MS_D2 110: EINT10 111: CSI1_D10
7	/	/	/
6:4	R/W	0	PH9_SELECT 000: Input 001: Output 010: LCD1_D9 011: ERXD2 100: KP_IN1 101: MS_D1 110: EINT9 111: CSI1_D9
3	/	/	/
2:0	R/W	0	PH8_SELECT 000: Input 001: Output 010: LCD1_D8 011: ERXD3 100: KP_IN0 101: MS_D0 110: EINT8 111: CSI1_D8

1.19.4.66. PH CONFIGURE REGISTER 2

Offset: 0x104			Register Name: PH_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PH23_SELECT 000: Input 001: Output 010: LCD1_D23 011: ETXEN 100: KP_OUT3 101: SDC1_CLK 110: Reserved 111: CSI1_D23
27	/	/	/
26:24	R/W	0	PH22_SELECT 000: Input 001: Output 010: LCD1_D22 011: EMDIO 100: KP_OUT2 101: SDC1_CMD 110: Reserved 111: CSI1_D22
23	/	/	/
22:20	R/W	0	PH21_SELECT 000: Input 001: Output 010: LCD1_D21 011: EMDC 100: CAN_RX 101: Reserved 110: EINT21 111: CSI1_D21
19	/	/	/
18:16	R/W	0	PH20_SELECT 000: Input 001: Output 010: LCD1_D20 011: ERXDV 100: CAN_TX 101: Reserved 110: EINT20 111: CSI1_D20
15	/	/	/
14:12	R/W	0	PH19_SELECT 000: Input 001: Output 010: LCD1_D19 011: ERXERR 100: KP_OUT1 101: SMC_SDA 110: EINT19 111: CSI1_D19
11	/	/	/
10:8	R/W	0	PH18_SELECT

Offset: 0x104			Register Name: PH_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			000: Input 001: Output 010: LCD1_D18 011: ERXCK 100: KP_OUT0 101: SMC_SCK 110: EINT18 111: CSI1_D18
7	/	/	/
6:4	R/W	0	PH17_SELECT 000: Input 001: Output 010: LCD1_D17 011: ETXD0 100: KP_IN7 101: SMC_VCCEN 110: EINT17 111: CSI1_D17
3	/	/	/
2:0	R/W	0	PH16_SELECT 000: Input 001: Output 010: LCD1_D16 011: ETXD1 100: KP_IN6 101: Reserved 110: EINT16 111: CSI1_D16

1.19.4.67. PH CONFIGURE REGISTER 3

Offset: 0x108			Register Name: PH_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	0	PH27_SELECT 000: Input 001: Output 010: LCD1_ VSYNC 011: ETXERR 100: KP_OUT7 101: SDC1_D3 110: Reserved 111: CSI1_VSYNC
11	/	/	Reserved
10:8	R/W	0	PH26Select 000: Input 001: Output 010: LCD1_HSYNC 011: ECOL

Offset: 0x108			Register Name: PH_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			100: KP_OUT6 101: SDC1_D2 110: Reserved 111: CSI1_HSYNC
7	/	/	/
6:4	R/W	0	PH25_SELECT 000: Input 001: Output 010: LCD1_DE 011: ECRS 100: KP_OUT5 101: SDC1_D1 110: Reserved 111: CSI1_FIELD
3	/	/	/
2:0	R/W	0	PH24_SELECT 000: Input 001: Output 010: LCD1_CLK 011: ETXCK 100: KP_OUT4 101: SDC1_D0 110: Reserved 111: CSI1_PCLK

1.19.4.68. PH DATA REGISTER

Offset: 0x10C			Register Name: PH_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.69. PH MULTI-DRIVING REGISTER 0

Offset: 0x110	Register Name: PH_DRV0 Default Value: 0x5555_5555

Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PH MULTI-DRIVING REGISTER 1

Offset: 0x114			Register Name: PH_DRV1 Default Value: 0x0055_5555
Bit	Read/Write	Default	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.70. PH PULL REGISTER 0

Offset: 0x118			Register Name: PH_PULL0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PH_PULL PH[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.71. PH PULL REGISTER 1

Offset: 0x11C			Register Name: PH_PULL1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:24	/	/	/

Offset: 0x11C			Register Name: PH_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~11)	R/W	0x0	PH_PULL PH[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

1.19.4.72. PI CONFIGURE REGISTER 0

Offset: 0x120			Register Name: PI_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PI7_SELECT 000: Input 001: Output 010: SDC3_D1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PI6_SELECT 000: Input 001: Output 010: SDC3_D0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PI5_SELECT 000: Input 001: Output 010: SDC3_CLK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PI4_SELECT 000: Input 001: Output 010: SDC3_CMD 011: Reserved

Offset: 0x120			Register Name: PI_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PI3_SELECT 000: Input 001: Output 010: PWM1 011: TWI4_SDA 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PI2_SELECT 000: Input 001: Output 010: Reserved 011: TWI4_SCK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PI1_SELECT 000: Input 001: Output 010: Reserved 011: TWI3_SDA 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PI0_SELECT 000: Input 001: Output 010: Reserved 011: TWI3_SCK 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.73. PI CONFIGURE REGISTER 1

Offset: 0x124			Register Name: PI_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

Offset: 0x124			Register Name: PI_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PI15_SELECT 000: Input 001: Output 010: SPI1_CS1 011: PS2_SDA1 100: TCLKIN1 101: Reserved 110: EINT27 111: Reserved
27	/	/	/
26:24	R/W	0	PI14_SELECT 000: Input 001: Output 010: SPI0_CS1 011: PS2_SCK1 100: TCLKIN0 101: Reserved 110: EINT26 111: Reserved
23	/	/	/
22:20	R/W	0	PI13_SELECT 000: Input 001: Output 010: SPI0_MISO 011: UART6_RX 100: CLK_OUT_B 101: Reserved 110: EINT25 111: Reserved
19	/	/	/
18:16	R/W	0	PI12_SELECT 000: Input 001: Output 010: SPI0_MOSI 011: UART6_TX 100: CLK_OUT_A 101: Reserved 110: EINT24 111: Reserved
15	/	/	/
14:12	R/W	0	PI11_SELECT 000: Input 001: Output 010: SPI0_CLK 011: UART5_RX 100: Reserved 101: Reserved 110: EINT23 111: Reserved
11	/	/	/
10:8	R/W	0	PI10_SELECT 000: Input 001: Output

Offset: 0x124			Register Name: PI_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			010: SPI0_CS0 011: UART5_TX 100: Reserved 101: Reserved 110: EINT22 111: Reserved
7	/	/	/
6:4	R/W	0	PI9_SELECT 000: Input 001: Output 010: SDC3_D3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PI8_SELECT 000: Input 001: Output 010: SDC3_D2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

1.19.4.74. PI CONFIGURE REGISTER 2

Offset: 0x128			Register Name: PI_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:23	/	/	/
22:20	R/W	0	PI21_SELECT 000: Input 001: Output 010: PS2_SDA0 011: UART7_RX 100: HSDA 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PI20_SELECT 000: Input 001: Output 010: PS2_SCK0 011: UART7_TX 100: HSCL 101: Reserved

Offset: 0x128			Register Name: PI_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PI19_SELECT 000: Input 001: Output 010: SPI1_MISO 011: UART2_RX 100: Reserved 101: Reserved 110: EINT31 111: Reserved
11	/	/	/
10:8	R/W	0	PI18_SELECT 000: Input 001: Output 010: SPI1_MOSI 011: UART2_TX 100: Reserved 101: Reserved 110: EINT30 111: Reserved
7	/	/	/
6:4	R/W	0	PI17_SELECT 000: Input 001: Output 010: SPI1_CLK 011: UART2_CTS 100: Reserved 101: Reserved 110: EINT29 111: Reserved
3	/	/	/
2:0	R/W	0	PI16_SELECT 000: Input 001: Output 010: SPI1_CS0 011: UART2_RTS 100: Reserved 101: Reserved 110: EINT28 111: Reserved

1.19.4.75. PI CONFIGURE REGISTER 3

Offset: 0x12C			Register Name: PI_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.76. PI DATA REGISTER

Offset: 0x130			Register Name: PI_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:22	/	/	/
21:0	R/W	0	PI_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

1.19.4.77. PI MULTI-DRIVING REGISTER 0

Offset: 0x134			Register Name: PI_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PI_DRV PI[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

1.19.4.78. PI MULTI-DRIVING REGISTER 1

Offset: 0x138			Register Name: PI_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	Reserved
[2i+1:2i] (i=0~5)	R/W	0x1	PI_DRV PI[n] Multi-Driving Select (n = 16~21) 00: Level 0 01: Level 1

Offset: 0x138			Register Name: PI_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			10: Level 2 11: Level 3

1.19.4.79. PI PULL REGISTER 0

Offset: 0x13C			Register Name: PI_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
[2i+1:2i] (i=0~12)	R/W	0x0	PI_PULL PI[n] Pull-up/down Select (n = 0~12) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1.19.4.80. PI PULL REGISTER 1

Offset: 0x140			Register Name: PI_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

1.19.4.81. PIO INTERRUPT CONFIGURE REGISTER 0

Offset: 0x200			Register Name: PIO_INT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge

Offset: 0x200			Register Name: PIO_INT_CFG0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
			0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

1.19.4.82. PIO INTERRUPT CONFIGURE REGISTER 1

Offset: 0x204			Register Name: PIO_INT_CFG1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

1.19.4.83. PIO INTERRUPT CONFIGURE REGISTER 2

Offset: 0x208			Register Name: PIO_INT_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 16~23) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative)

Offset: 0x208			Register Name: PIO_INT_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
			Others: Reserved

1.19.4.84. PIO INTERRUPT CONFIGURE REGISTER 3

Offset: 0x20C			Register Name: PIO_INT_CFG3 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 24~31) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

1.19.4.85. PIO INTERRUPT CONTROL REGISTER

Offset: 0x210			Register Name: PIO_INT_CTL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[n] (n=0~31)	R/W	0	PIO_INT_CTL External INTn Enable (n = 0~31) 0: Disable 1: Enable

1.19.4.86. PIO INTERRUPT STATUS REGISTER

Offset: 0x214			Register Name: PIO_INT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[n] (n=0~31)	R/W	0	PIO_INT_STATUS External INTn Pending Bit (n = 0~31) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

1.19.4.87. PIO INTERRUPT DEBOUNCE REGISTER

Offset: 0x218			Register Name: PIO_INT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

Chapter 2 Memory

This chapter details the A20 memory subsystem:

- DRAM
- NAND FLASH

2.1. DRAM

1.19.5. Overview

The DRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all in-dusty-standard double data rate II (DDR2) ordinary SDRAM andouble data rate III (DDR3) ordinary SDRAM. It supports up to a 16G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

It features:

- Support DDR3L/DDR3/DDR2 SDRAM
- Support different memory device's power of 1.35V,1.5V and 1.8V
- Support memory capacity up to 16G bits (2GB)
- 16 address lines and 3 bank address lines
- Data IO size can up to 32-bit for DDR2 and DDR3 (x8, x16)
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different applications
- Priority of transferring through multiple ports is programmable
- Random read or write operations

2.2. NAND Flash

1.19.6. Overview

The NFC is the NAND Flash Controller which supports all NAND/MLC flash memory available in the market. New type flash can be supported by software reconfiguration. The NFC can support 8 NAND flash with 1.8/3.3 V voltage supply. There are 8 separate chip select lines (CE#) for connecting up to 8 flash chips with2 R/B signals.

The On-the-fly error correction code (ECC) is built-in NFC for enhancing reliability. BCH is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

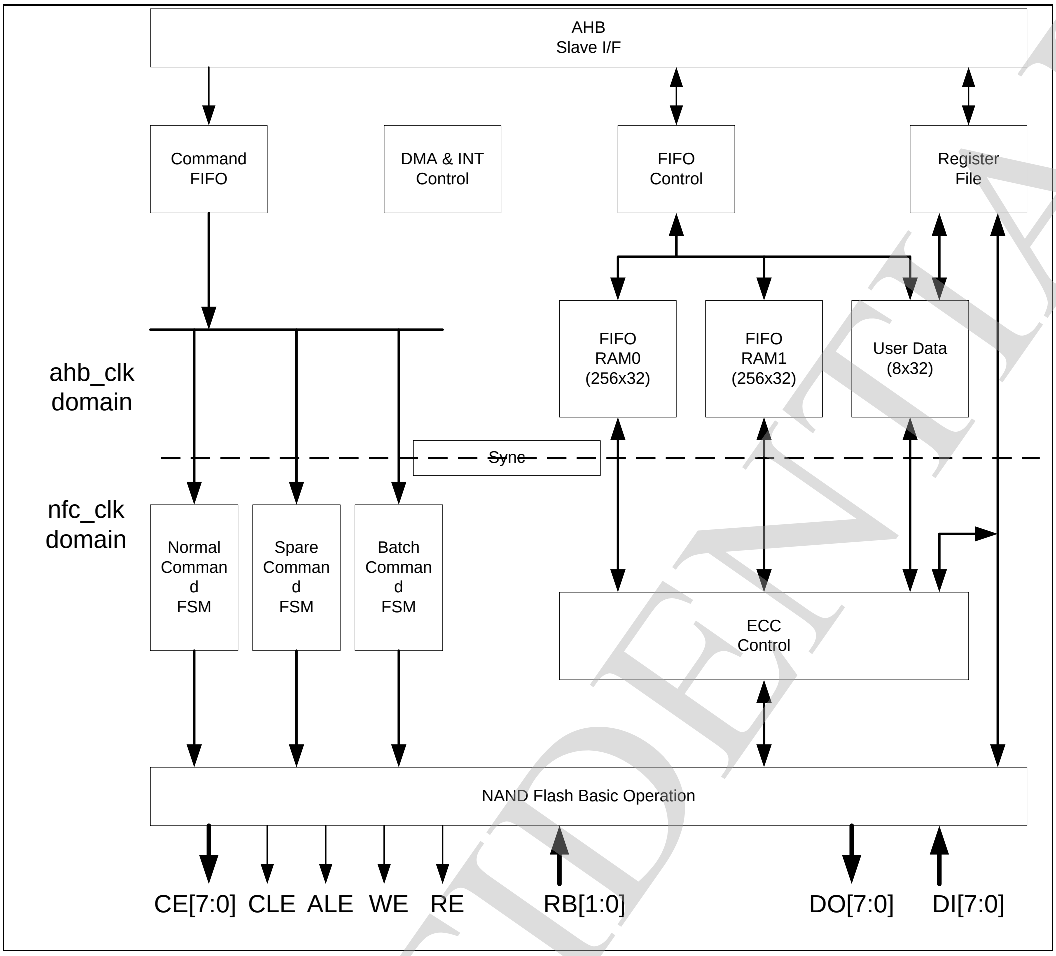
The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control for reading or writing external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kind of modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

It features:

- Comply to ONFI 2.3 and Toggle 1.0
- Support 64-bit ECC per 512 bytes or 1024 bytes
- Support 8bits data bus width
- Support 1.8V/3.3V signal voltage
- Support 1K/2K/4K/8K/16K page size
- Support up to 8 CE and 2 RB
- Support system boot from NAND flash
- Support SLC/MLC NAND and EF-NAND
- Support SDR/DDR NAND interface

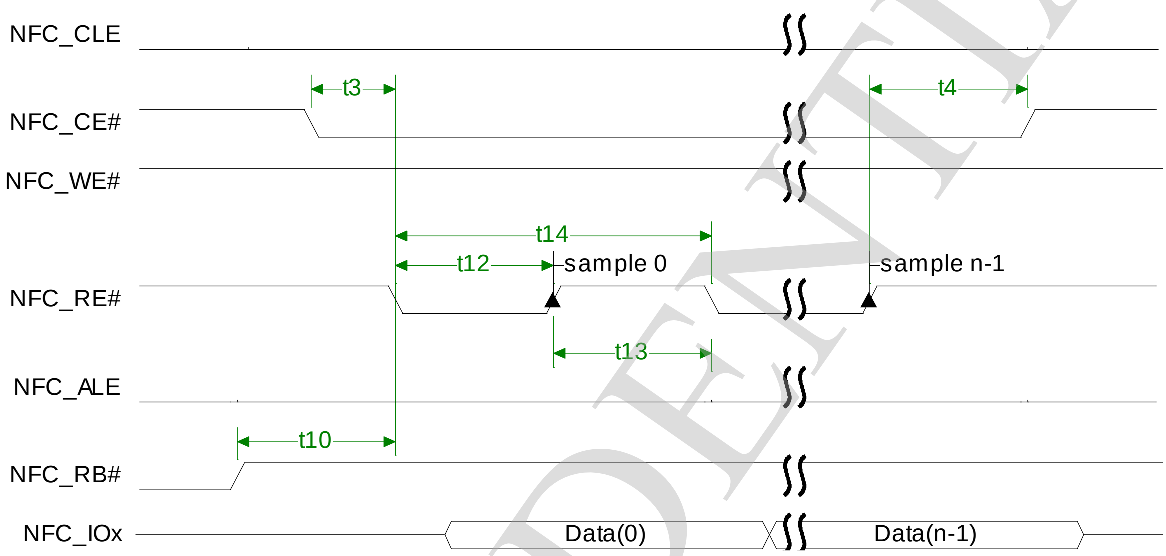
1.19.7. Nand Flash Block Diagram



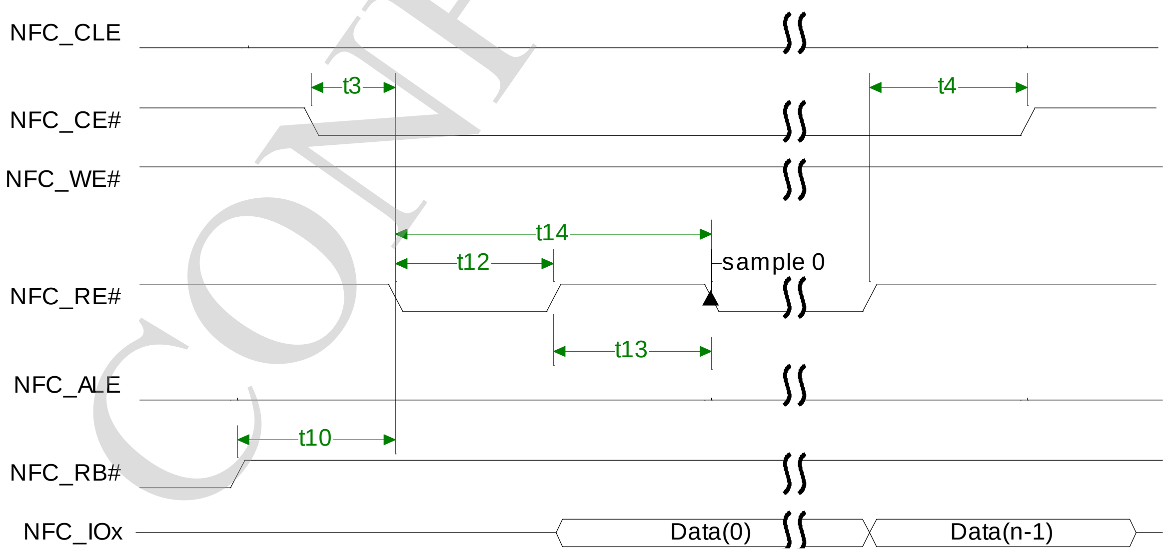
1.19.8. NFC Timing Diagram

Typically, there are two kinds of serial access method. One method is conventional method which fetching data at the rise edge of NFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NFC_RE# signal line.

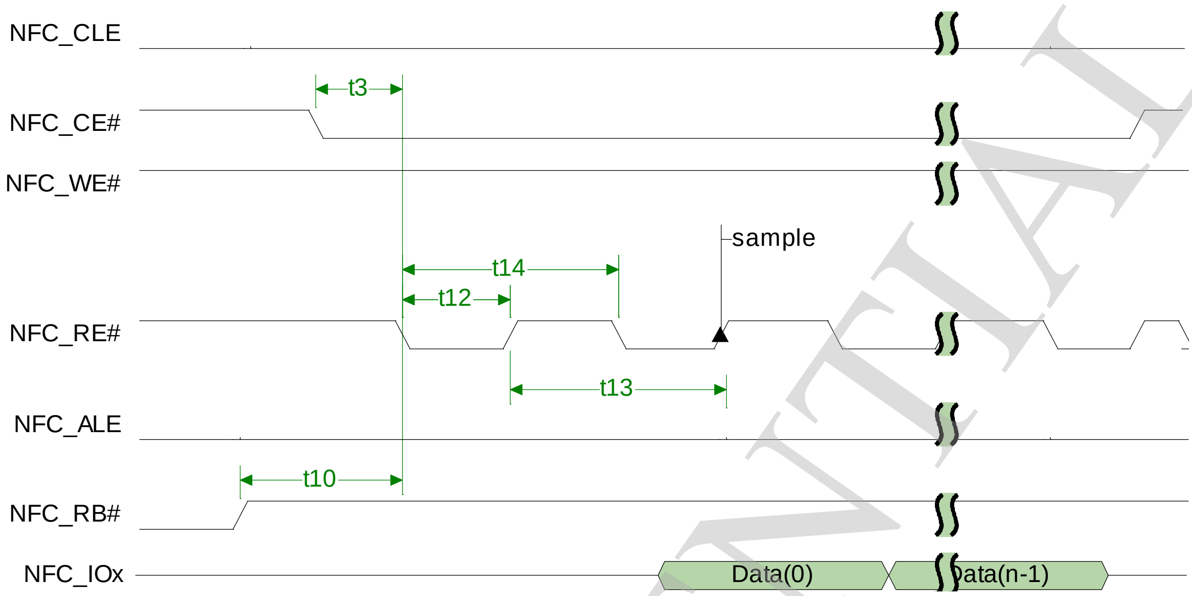
Conventional Serial Access after Read Cycle (SAM0)



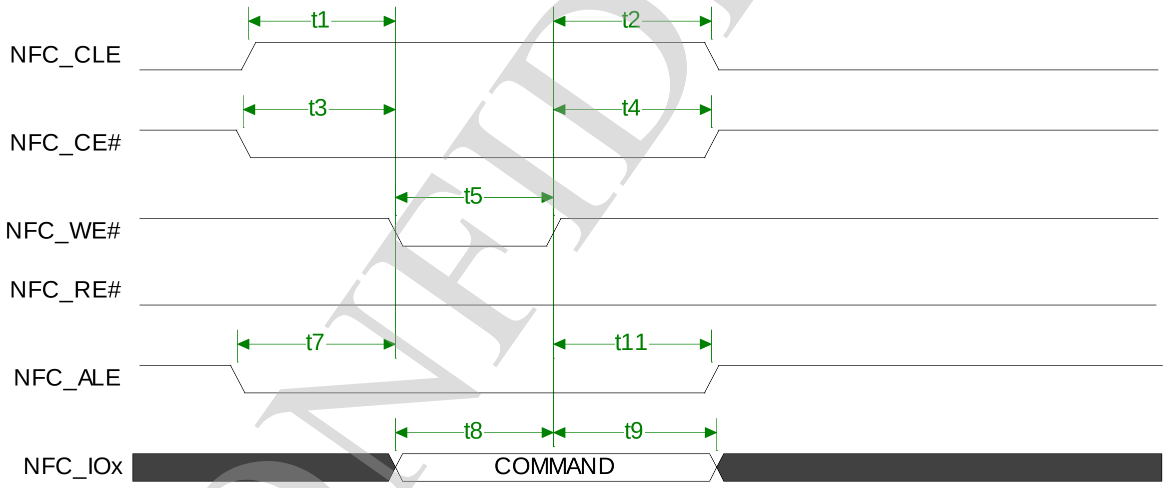
EDO type Serial Access after Read Cycle (SAM1)



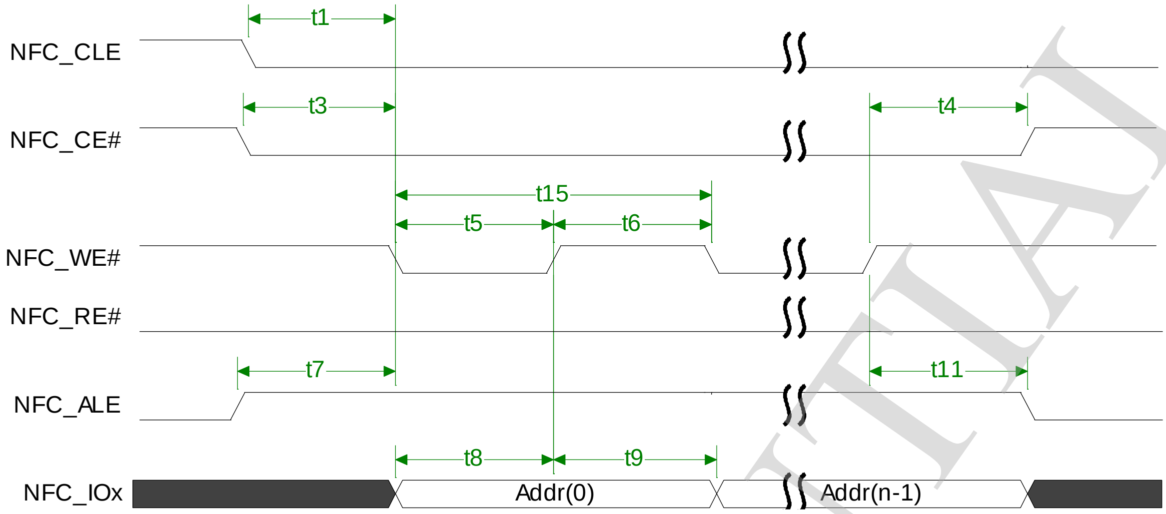
Extending EDO type Serial Access Mode (SAM2)



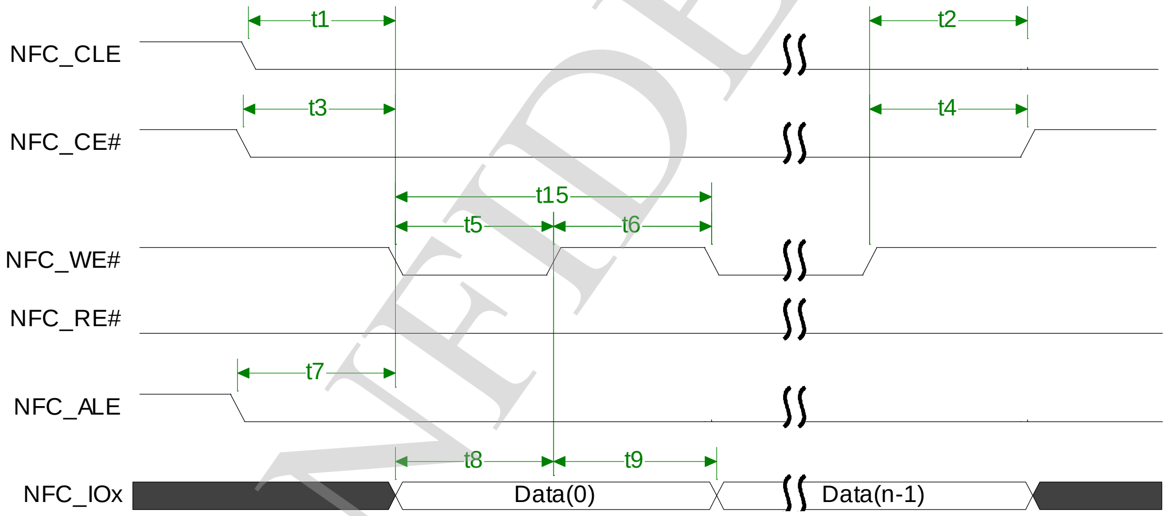
Command Latch Cycle



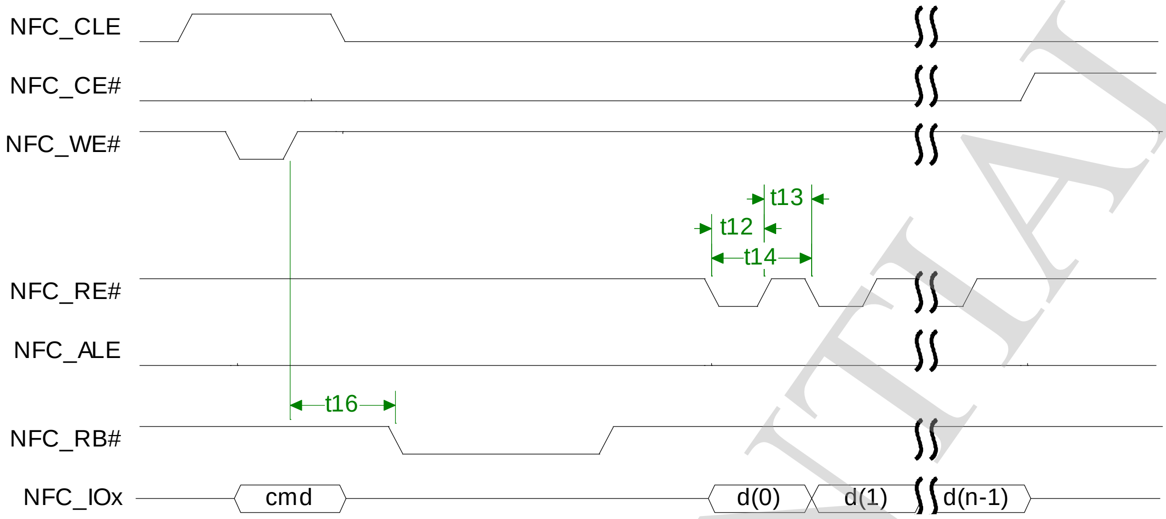
Address Latch Cycle



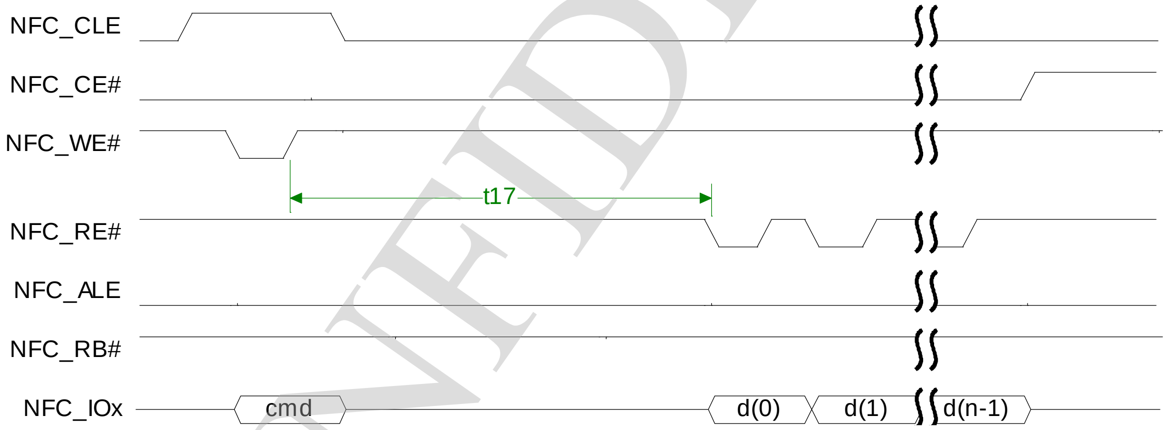
Write Data to Flash Cycle



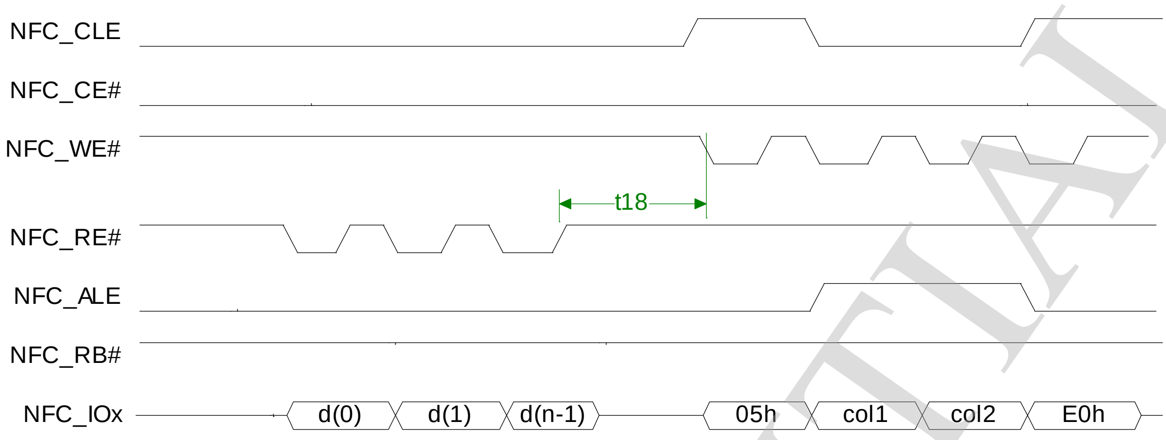
Waiting R/B# ready Diagram



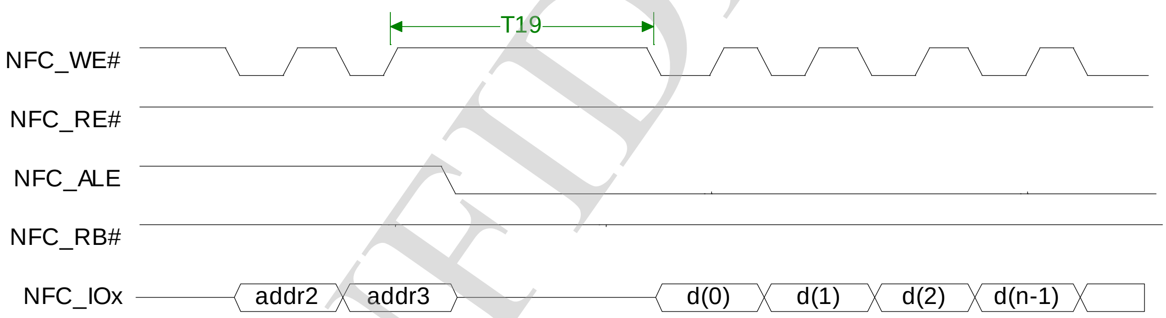
WE# high to RE# low Timing Diagram



RE# high to WE# low Timing Diagram



Address to Data Loading Timing Diagram



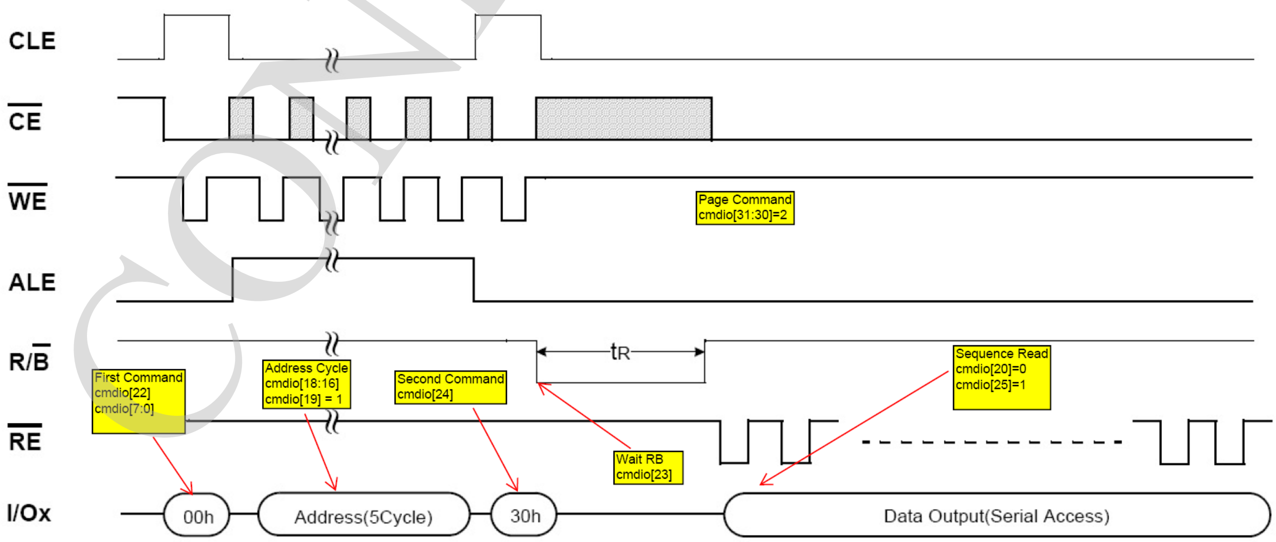
Timing Cycle List:

ID	Parameter	Timing	Notes
T1	NFC_CLE setup time	T	
T2	NFC_CLE hold time	T	
T3	NFC_CE setup time	T	
T4	NFC_CE hold time	T	
T5	NFC_WE# pulse width	T	
T6	NFC_WE# hold time	T	
T7	NFC_ALE setup time	T	

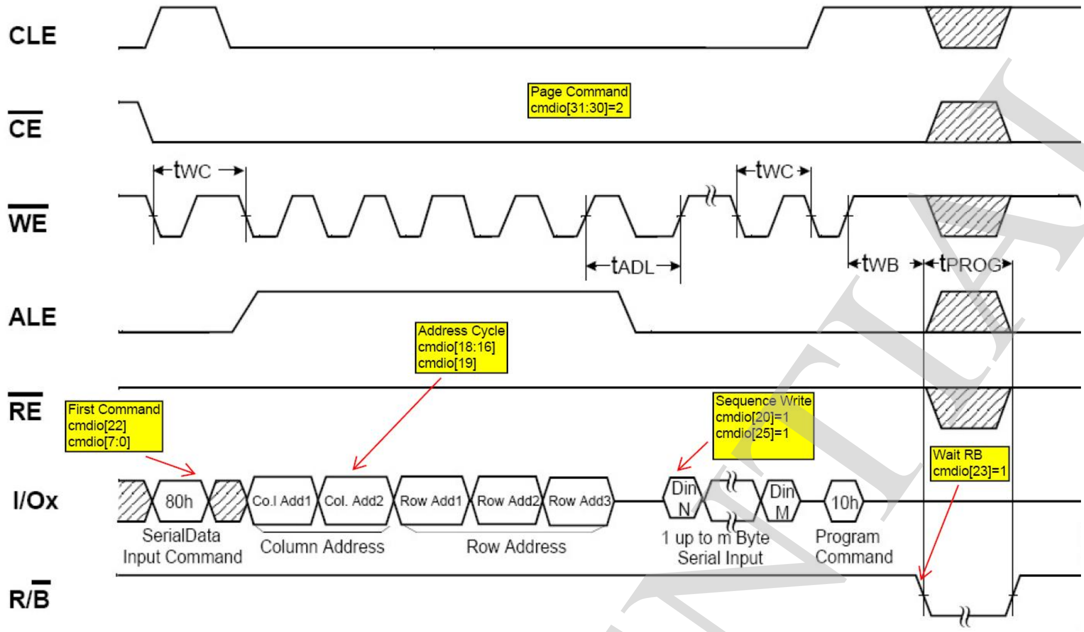
ID	Parameter	Timing	Notes
T8	Data setup time	T	
T9	Data hold time	T	
T10	Ready to NFC_RE# low	3T	
T11	NFC_ALE hold time	T	
T12	NFC_RE# pulse width	T	
T13	NFC_RE# hold time	T	
T14	Read cycle time	2T	
T15	Write cycle time	2T	
T16	NFC_WE# high to R/B# busy	tWB	Specified by timing configure register(NFC_TIMING_CFG)
T17	NFC_WE# high to NFC_RE# low	tWHR	Specified by timing configure register(NFC_TIMING_CFG)
T18	NFC_RE# high to NFC_WE# low	tRHW	Specified by timing configure register(NFC_TIMING_CFG)
T19	Address to Data Loading time	tADL	Specified by timing configure register(NFC_TIMING_CFG)

Note: T is the clock period duration of NFC_CLK (x2).

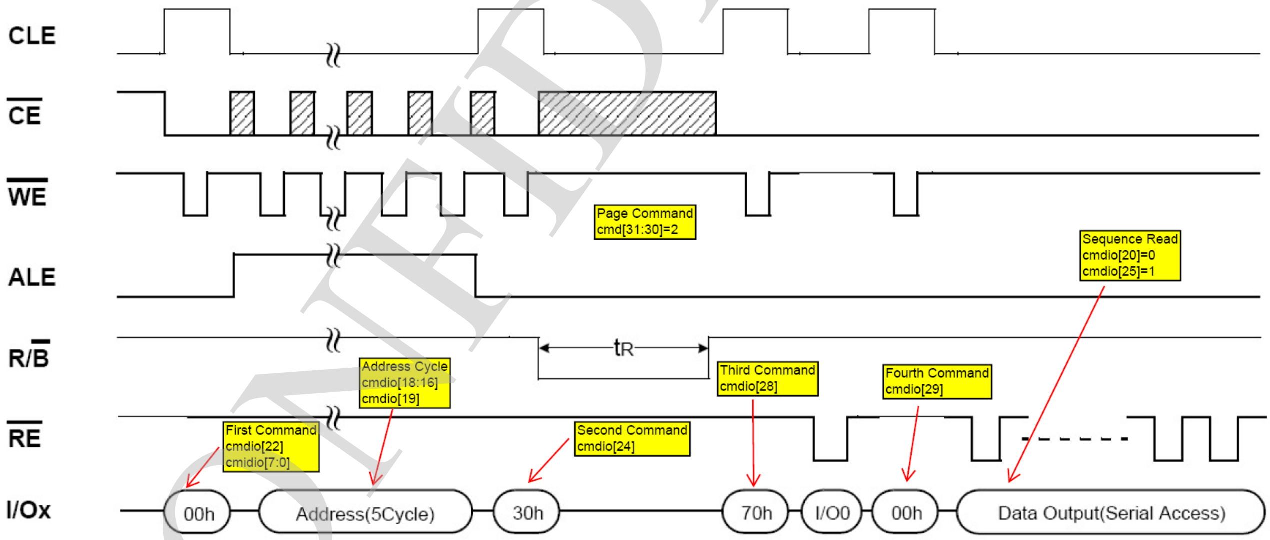
1.19.9. NFC Operation Guide



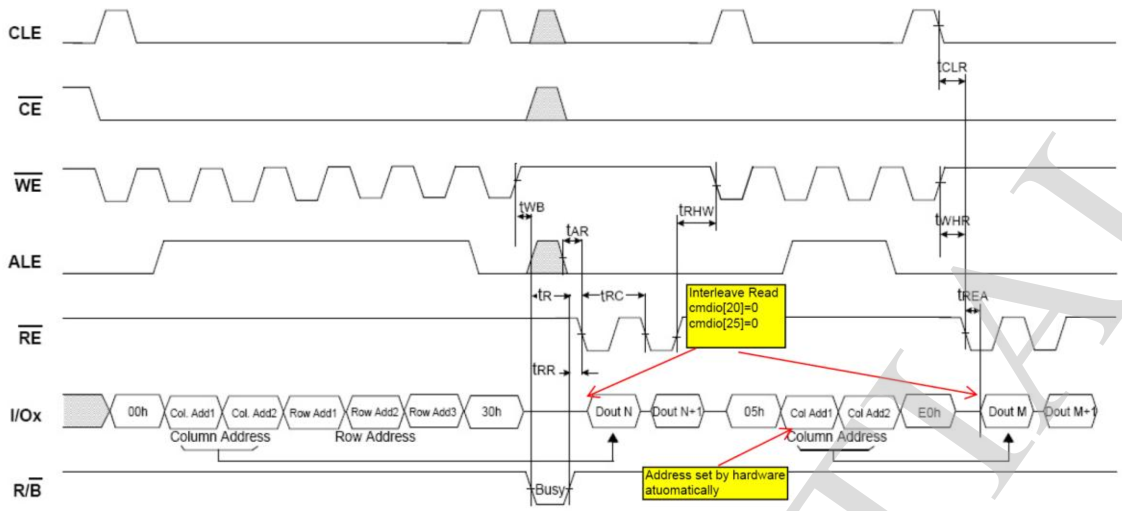
Page Read Command Diagram



Page Program Diagram



EF-NAND Page Read Diagram



Interleave Page Read Diagram

Chapter 3 Graphic

This chapter mainly details the mixer processor in A20.

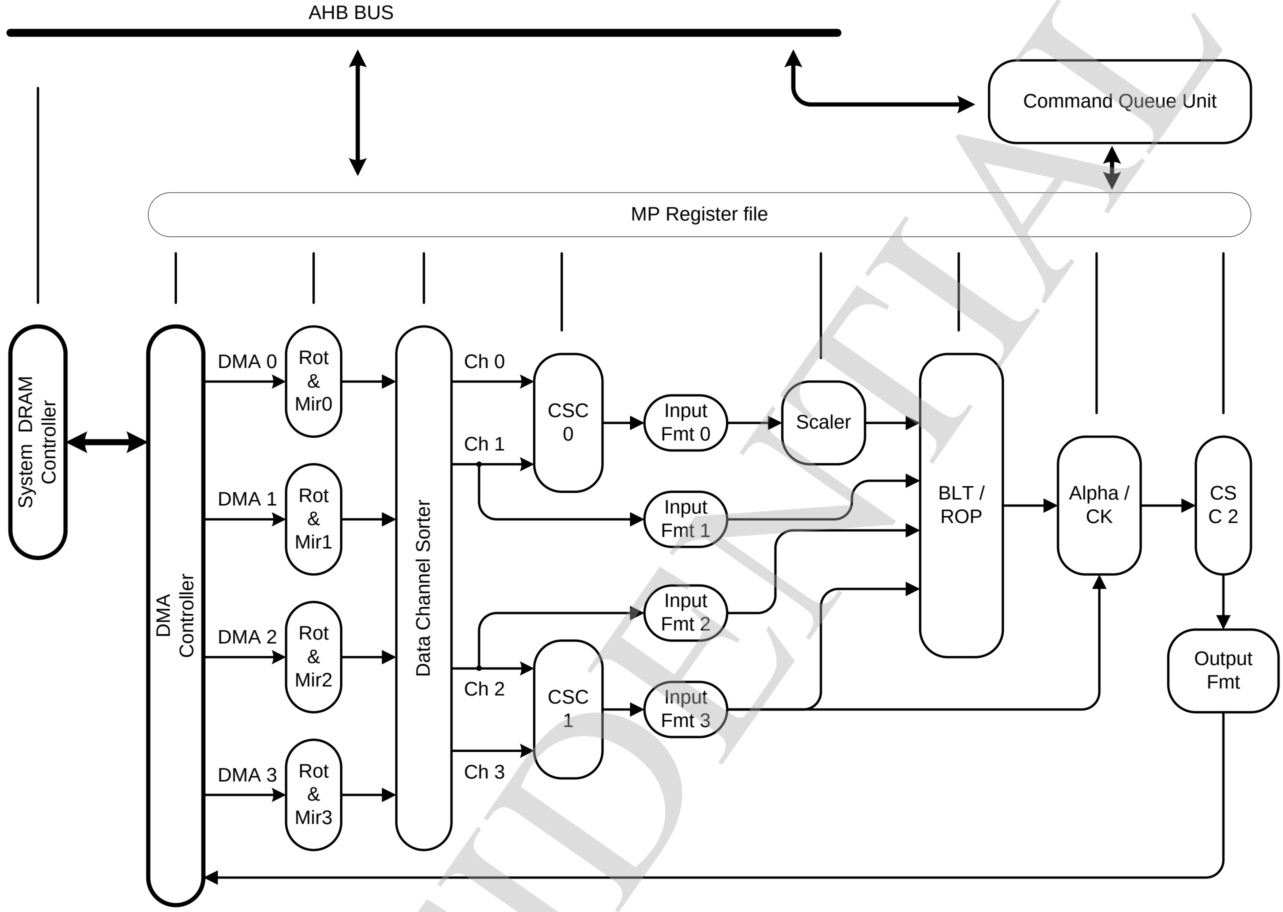
3.1. Mixer Processor

3.1.1. Overview

The mixer processor features:

- support multiple color formats
  - ARGB 8888/4444/1555
  - RGB565
  - MONO 1/2/4/8 bpp
  - Palette 1/2/4/8 bpp (input only)
  - YUV 444/422/420
- Buffer block size up to 8192x8192 pixels
- Memory scan order option support
- Clipping support
- ROP2
  - Line / Rectangle / Point
  - Block fill
- ROP3
  - BitBLT
  - PatBLT
  - StretchBLT
- ROP4
  - MaskBLT
- Support 90/180/270 degree rotation
- Mirror support
- Alpha blending
  - Plane & Pixel alpha support
  - Output alpha configurable support
- Color key support
- Scaling
  - 4x4 taps
  - 32 phase
- Color space convert support

3.1.2. Mixer Processor Block Diagram



3.1.3. MP Register List

Module name	Base address
MP	0x01e80000

Register name	Offset	Description
MP_CTL_REG	0x0	Mixer control register
MP_STS_REG	0x4	Mixer Status register
MP_IDMAGLBCTL_REG	0x8	Input DMA globe control register

Register name	Offset	Description
MP_IDMA_H4ADD_REG	0xC	Input DMA start address high 4bits register
MP_IDMA_L32ADD_REG	0x10 – 0x1C	Input DMA start address low 32bits register
MP_IDMALINEWIDTH_REG	0x20 – 0x2C	Input DMA line width register
MP_IDMASIZE_REG	0x30 – 0x3C	Input DMA memory block size register
MP_IDMACOOR_REG	0x40 – 0x4C	Input DMA memory block coordinate control register
MP_IDMASET_REG	0x50 – 0x5C	Input DMA setting register
MP_IDMAFILLCOLOR_REG	0x60 – 0x6C	Input DMA fill-color register
MP_IDMASORT_REG	0x70	Input DMA channel sorter register
MP_CSC0CTL_REG	0x74	Color space converter 0 control register
MP_CSC1CTL_REG	0x78	Color space converter 1 control register
MP_SCACTL_REG	0x80	Scaler control register
MP_SCAOUTSIZE_REG	0x84	Scaling output size register
MP_SCAHORFCT_REG	0x88	Scaler horizontal scaling factor register
MP_SCAVERFCT_REG	0x8C	Scaler vertical scaling factor register
MP_SCAHORPHASE_REG	0x90	Scaler horizontal start phase setting register
MP_SCAVERPHASE_REG	0x94	Scaler vertical start phase setting register
MP_ROPCTL_REG	0xB0	ROP control register
MP_ROPIDX0CTL_REG	0xB8	ROP channel 3 index 0 control table setting register
MP_ROPIDX1CTL_REG	0xBC	ROP channel 3 index 1 control table setting register
MP_ALPHACKCTL_REG	0xC0	Alpha / Color key control register
MP_CKMIN_REG	0xC4	Color key min color register
MP_CKMAX_REG	0xC8	Color key max color register
MP_ROPOUTFILLCOLOR_REG	0xCC	Fill color of ROP output setting register
MP_CSC2CTL_REG	0xD0	Color space converter 2 control register
MP_OUTCTL_REG	0xE0	Output control register
MP_OUTSIZE_REG	0xE8	Output size register
MP_OUTH4ADD_REG	0xEC	Output address high 4bits register
MP_OUTL32ADD_REG	0xF0 – 0xF8	Output address low 32bits register
MP_OUTLINEWIDTH_REG	0x100 – 0x108	Output line width register

Register name	Offset	Description
MP_OUTALPHACTL_REG	0x120	Output alpha control register
MP_ICSCYGCOEF_REG	0x180 – 0x188	CSC0/1 Y/G coefficient register
MP_ICSCYGCONS_REG	0x18C	CSC0/1 Y/G constant register
MP_ICSCURCOEF_REG	0x190 – 0x198	CSC0/1 U/R coefficient register
MP_ICSCURCONS_REG	0x19C	CSC0/1 U/R constant register
MP_ICSCVBCOEF_REG	0x1A0 – 0x1A8	CSC0/1 V/B coefficient register
MP_ICSCVBCONS_REG	0x1AC	CSC0/1 V/B constant register
MP_OCSCYGCOEF_REG	0x1C0 – 0x1C8	CSC2 Y/G coefficient register
MP_OCSCYGCONS_REG	0x1CC	CSC2 Y/G constant register
MP_OCSCURCOEF_REG	0x1D0 – 0x1D8	CSC2 U/R coefficient register
MP_OCSCURCONS_REG	0x1DC	CSC2 U/R constant register
MP_OCSCVBCOEF_REG	0x1E0 – 0x1E8	CSC2 V/B coefficient register
MP_OCSCVBCONS_REG	0x1EC	CSC2 V/B constant register
Memory		
	0x200 – 0x27C	Scaling horizontal filtering coefficient RAM block
	0x280 – 0x2FC	Scaling vertical filtering coefficient RAM block
	0x400 – 0x7FF	Palette table

3.1.4. MP Register Description

3.1.4.1. MIXER CONTROL REGISTER

Offset: 0x0			Register Name: MP_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0	**HWERRIRQ_EN** Hardware error IRQ enable control 0:disable

Offset: 0x0			Register Name: MP_CTL_REG
Bit	Read/Write	Default/Hex	Description
			1:enable
8	R/W	0	**FINISHIRQ_EN** Mission finish IRQ enable control 0:disable 1:enable
7:2	/	/	/
1	R/W	0	**START_CTL** Start control If the bit is set, the module will start 1 frame operation and stop auto.
0	R/W	0	**MP_EN** Enable control 0:disable 1:enable

3.1.4.2. MIXER STATUS REGISTER

Offset: 0x4			Register Name: MP_STS_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R	0	**HWERR_FLAG** Hardware error status
12	R	0	**BUSY_FLAG** Module working status 0:idle 1:running
11:10	/	/	/
9	R/W	0	**HWERRIRQ_FLAG** Hardware error IRQ It will be set when hardware error occur, and cleared by writing 1.
8	R/W	0	**FINISHIRQ_FLAG**

Offset: 0x4			Register Name: MP_STS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Mission finish IRQ It will be set when 1 frame operation accomplished, and cleared by writing 1.
7:0	/	/	/

3.1.4.3. INPUT DMA GLOBE CONTROL REGISTER

Offset: 0x8			Register Name: MP_IDMAGLBCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0	**MEMSCANORDER** Memory scan order selection 0: Top to down Left to right 1: Top to down Right to left 2: Down to top Left to right 3: Down to top Right to left Note: ----Four input DMA channel use the same scan rule. ----The each output DMA channel should match the same memory scan order rule with the input DMA channel.
7:0	/	/	/

3.1.4.4. INPUT DMA START ADDRESS HIGH 4BITS REGISTER

Offset: 0xC			**Register Name: MP_IDMA_H4ADD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0	**IDMA3_H4ADD** iDMA3 High 4bits address in bits
23:20	/	/	/
19:16	R/W	0	**IDMA2_H4ADD** iDMA2 High 4bits address in bits
15:12	/	/	/
11:8	R/W	0	**IDMA1_H4ADD** iDMA1 High 4bits address in bits
7:4	/	/	/
3:0	R/W	0	**IDMA0_H4ADD** iDMA0 High 4bits address in bits

3.1.4.5. INPUT DMA START ADDRESS LOW 32BITS REGISTER

Offset: **iDMA0:0x10** **iDMA1:0x14** **iDMA2:0x18** **iDMA3:0x1C**			**Register Name: MP_IDMA_L32ADD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**IDMA_L32ADD** iDMA Low 32bits address in bits

3.1.4.6. INPUT DMA LINE WIDTH REGISTER

Offset: iDMA0:0x20 iDMA1:0x24 iDMA2:0x28 iDMA3:0x2C			Register Name: MP_IDMALINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**IDMA_LINEWIDTH** iDMA Line width in bits

3.1.4.7. INPUT DMA MEMORY BLOCK SIZE REGISTER

Offset: iDMA0:0x30 iDMA1:0x34 iDMA2:0x38 iDMA3:0x3C			Register Name: MP_IDMASIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**IDMA_HEIGHT** Memory block height in pixels The height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0	**IDMA_WIDTH** Memory block width in pixels The width = The value of these bits add 1

3.1.4.8. INPUT DMA MEMORY BLOCK COORDINATE CONTROL REGISTER

Offset: iDMA0:0x40 iDMA1:0x44 iDMA2:0x48 iDMA3:0x4C			Register Name: MP_IDMACOOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**IDMA_YCOOR** Y coordinate Y is the left-top y coordinate of layer on output window in pixels The Y represent the two's complement
15:0	R/W	0	**IDMA_XCOOR** X coordinate X is left-top x coordinate of the layer on output window in pixels The X represent the two's complement

3.1.4.9. INPUT DMA SETTING REGISTER

Offset: iDMA0:0x50 iDMA1:0x54 iDMA2:0x58 iDMA3:0x5C			Register Name: MP_IDMASET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**IDMA_GLBALPHA** Globe alpha value
23:17	/	/	/
16	R/W	0	**IDMA_FCMODEN** Fill color mode enable control 0: disable 1: enable
15:12	R/W	0	**IDMA_PS** Input data pixel sequence

Offset: iDMA0:0x50 iDMA1:0x54 iDMA2:0x58 iDMA3:0x5C			Register Name: MP_IDMASET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Reference input pixel sequence table
11:8	R/W	0	**IDMA_FMT** Input data format 0x0:32bpp – A8R8G8B8 or interleaved AYUV8888 0x1:16bpp – A4R4G4B4 0x2:16bpp – A1R5G5B5 0x3:16bpp – R5G6B5 0x4:16bpp – interleaved YUV422 0x5:16bpp – U8V8 0x6:8bpp – Y8 0x7:8bpp – MONO or palette 0x8:4bpp – MONO or palette 0x9:2bpp – MONO or palette 0xa:1bpp – MONO or palette Other: reserved Note: if the input data format is 16 or 32bpp, and the work mode is palette mode, only the low 8 bits input data is valid.
7:4	R/W	0	**IDMA_ROTMIRCTL** Rotation and mirroring control 0:normal 1:X 2:Y 3:XY 4:A 5:AX 6:AY 7:AXY Other: reserved
3:2	R/W	0	**IDMA_ALPHACTL** Alpha control

Offset: iDMA0:0x50 iDMA1:0x54 iDMA2:0x58 iDMA3:0x5C			**Register Name: MP_IDMASET_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
			0:Ignore Output alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 1:Globe alpha enable Ignore pixel alpha value Output alpha value = globe alpha value 2: Globe alpha mix pixel alpha Output alpha value = globe alpha value * pixels alpha value 3:Reserved Note: the output alpha value here means the input alpha value of the ALU following the DMA controller.
1	R/W	0	**IDMA_WORKMOD** Work mode selection 0: normal mode (non-palette mode) 1: palette mode
0	R/W	0	**IDMA_EN** Input DMA enable control 0:disable input DMA channel, the respective fill-color value will stead of the input data. 1:enable

3.1.4.10. INPUT DMA FILL-COLOR REGISTER

Offset: iDMA0:0x60 iDMA1:0x64 iDMA2:0x68 iDMA3:0x6C	**Register Name: MP_IDMAFILLCOLOR_REG**

Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	**IDMA_FCALPHA** Alpha
23:16	R/W	0	**IDMA_FCRED** Red
15:8	R/W	0	**IDMA_FCGREEN** Green
7:0	R/W	0	**IDMA_FCBLUE** Blue

3.1.4.11. COLOR SPACE CONVERTER 0 CONTROL REGISTER

Offset: 0x74			Register Name: MP_CSC0CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0	**CSC0_DATAMOD** Data mode control 0: Interleaved AYUV8888 mode 1: Interleaved YUV422 mode In mode 0 and mode 1, only the channel 0 data path is valid for this module, the channel 1 data flow will by-pass the csc0 module, and direct to input formatter 1. 2: Planar YUV422 mode (UV combined only) 3: Planar YUV420 mode (UV combined only) 4: Planar YUV411 mode (UV combined only) In mode 2/3/4, following rule: ----Y component data transfer through channel 0, and UV component data transfer through channel 1.

Offset: 0x74			Register Name: MP_CSC0CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			----In this mode, the output data of the input formatter 1 will be stead of the respective fill-color value.
3:1	/	/	/
0	R/W	0	**CSC0_EN** Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

3.1.4.12. COLOR SPACE CONVERTER 1 CONTROL REGISTER

Offset: 0x78			Register Name: MP_CSC1CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0	**CSC1_DATAMOD** Data mode control 0: Interleaved AYUV8888 mode 1: Interleaved YUV422 mode In mode 0 and mode 1, only the channel 3 data path is valid for this module, the channel 2 data flow will by-pass the csc1 module, and direct to input formatter 2. 2: Planar YUV422 mode (UV combined only) 3: Planar YUV420 mode (UV combined only) 4: Planar YUV411 mode (UV combined only)

Offset: 0x78			Register Name: MP_CSC1CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			In mode 2/3/4, following rule: ----Y component data transfer through channel 3, and UV component data transfer through channel 2. ----In this mode, the output data of the input formatter 2 will be stead of the respective fill-color value.
3:1	/	/	/
0	R/W	0	**CSC1_EN** Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

3.1.4.13. SCALER CONTROL REGISTER

Offset: 0x80			Register Name: MP_SCACTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0	**SCA_ALGSEL** Scaling algorithm selection 0: bi-cubic(4 taps in vertical and horizontal) 1: linear in vertical and bi-linear in horizontal(2 taps in vertical and 4 taps in horizontal) 2: extractive in vertical and bi-linear in horizontal(1 tap in vertical and 4 taps in horizontal) 3: reserved
3:1	/	/	/
0	R/W	0	**SCA_EN** Enable control 0: Disable scaler, ignore the whole scaling setting, and the data flow will by-pass the module. 1:

Offset: 0x80			Register Name: MP_SCACTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Enable scaling function.

3.1.4.14. SCALING OUTPUT SIZE REGISTER

Offset: 0x84			Register Name: MP_SCAOUTSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**SCA_OUTHEIGHT** Output height The output height = The value of these bits add 1 The minimum output height is 8 pixels.
15:13	/	/	/
12:0	R/W	0	**SCA_OUTWIDTH** Output width The output width = The value of these bits add 1 The minimum output width is 16 pixels.

3.1.4.15. SCALER HORIZONTAL SCALING FACTOR REGISTER

Offset: 0x88			Register Name: MP_SCAHORFCT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	**/**	**/**	**/**
23:16	**R/W**	**0**	**SCA_HORINTFCT** The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:00	**R/W**	**0**	**SCA_HORFRAFCT** The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

Offset: 0x88			Register Name: MP_SCAHORFCT_REG
Bit	Read/Write	Default/Hex	Description
			The input width is the memory block width of respective iDMA channel.

3.1.4.16. SCALER VERTICAL SCALING FACTOR REGISTER

Offset: 0x8C			Register Name: MP_SCAVERFCT_REG
Bit	Read/ Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	**SCA_VERINTFCT** The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:00	R/W	0	**SCA_VERFRAFCT** The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height The input height is the memory block height of respective iDMA channel.

3.1.4.17. SCALER HORIZONTAL START PHASE SETTING REGISTER

Offset: 0x90			Register Name: MP_SCAHORPHASE_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:00	R/W	0	**SCA_HORPHASE** Start phase in horizontal (complement) This value equals to start phase * 2^{16}

3.1.4.18. SCALER VERTICAL START PHASE SETTING REGISTER

Offset: 0x94			Register Name: MP_SCAVERPHASE_REG
Bit	**Read/W rite**	**Default/He x**	**Description**
31:20	/	/	/
19:00	R/W	0	SCA_VERPHASE Start phase in vertical (complement) This value equals to start phase * 2^{16}

3.1.4.19. ROP CONTROL REGISTER

Offset: 0xB0			Register Name: MP_ROPCTL_REG
Bit	**Read/W rite**	**Default/H ex**	**Description**
31:16	/	/	/
15:14	R/W	0	**ROP_ALPHABYPASSSEL** ROP output Alpha channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved Note: the bit is only valid in by-pass mode of Alpha channel
13:12	R/W	0	**ROP_REDBYPASSSEL** ROP output Red channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved Note: the bit is only valid in by-pass mode of Red channel
11:10	R/W	0	**ROP_GREENBYPASSSEL** ROP output Green channel selection 0: channel 0 1: channel 1

Offset: 0xB0			Register Name: MP_ROPCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			2: channel 2 3:reserved Note: the bit is only valid in by-pass mode of Green channel
9:8	R/W	0	**ROP_BLUEBYPASSSEL** ROP output Blue channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved Note: the bit is only valid in by-pass mode of Blue channel
7	R/W	0	**ROP_ALPHABYPASSEN** ROP Alpha channel by-pass enable control 0:pass through 1:by-pass
6	R/W	0	**ROP_REDBYPASSEN** ROP Red channel by-pass enable control 0:pass through 1:by-pass
5	R/W	0	**ROP_GREENBYPASSEN** ROP Green channel by-pass enable control 0:pass through 1:by-pass
4	R/W	0	**ROP_BLUEBYPASSEN** ROP Blue channel by-pass enable control 0:pass through 1:by-pass
3:1	/	/	/
0	R/W	0	**ROP_MOD** ROP type selection 0:ROP3 1:ROP4 ----In ROP3 mode, only the value of 'channel 3 index 0 control

Offset: 0xB0			Register Name: MP_ROPCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			table setting register' will be selected. ----In ROP3 mode, the channel 3 data will by-pass the ROP module. ----In ROP3 mode, the channel 3 data will direct to Alpha/CK module. ----In ROP4 mode, the respective input DMA channel fill color of channel 3 will transfer to Alpha/CK module.

3.1.4.20. ROP CHANNEL 3 INDEX 0 CONTROL TABLE SETTING REGISTER

Offset: 0xB8			Register Name: MP_ROPIDX0CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0	**NOD7_CTL** Index 0 node7 setting (channel 0' and channel 1' and channel 2' mix not logic) 0:by-pass 1:not
14:11	R/W	0	**NOD6_CTL** Index 0 node6 setting (channel 0' and channel 1' and channel 2' mix logic) 0:and 1:or 2:xor 3:add in byte 4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0' mix channel 1' then sub channel 2' in byte 8:channel 0' mix channel 1' then sub channel 2' in word (32bit) Other: Reserved
10	R/W	0	**NOD5_CTL** Index 0 node5 setting (channel 0' and channel 1' mix not logic) 0:by-pass 1:not

Offset: 0xB8			Register Name: MP_ROPIDX0CTL_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0	**NOD4_CTL** Index 0 node4 setting (channel 0' and channel 1' mix logic) 0:and 1:or 2:xor 3:add in byte 4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0' sub channel 1' in byte 8:channel 0' sub channel 1' in word (32bit) Other: Reserved
5	R/W	0	**NOD3_CTL** Index 0 node3 setting (channel 2' not logic) 0:by-pass 1:not
4	R/W	0	**NOD2_CTL** Index 0 node2 setting (channel 1' not logic) 0:by-pass 1:not
3	R/W	0	**NOD1_CTL** Index 0 node1 setting (channel 0' not logic) 0:by-pass 1:not
2:0	R/W	0	**NOD0_CTL** Index 0 node0 setting (sorting control) 0:012 1:021 2:102 3:120 4:201 5:210 Other: Reserved

Note: the result of the add or multiply operation will select the high 8 (byte operation) or 32bits (word operation).

3.1.4.21. ROP CHANNEL 3 INDEX 1 CONTROL TABLE SETTING REGISTER

Offset: 0xBC			Register Name: MP_ROPIDX1CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0	**NOD7_CTL** Index 1 node7 setting (channel 0’ and channel 1’ and channel 2’ mix not logic) 0:by-pass 1:not
14:11	R/W	0	**NOD6_CTL** Index 1 node6 setting (channel 0’ and channel 1’ and channel 2’ mix logic) 0:and 1:or 2:xor 3:add in byte 4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0’ mix channel 1’ then sub channel 2’ in byte 8:channel 0’ mix channel 1’ then sub channel 2’ in word (32bit) Other: Reserved
10	R/W	0	**NOD5_CTL** Index 1 node5 setting (channel 0’ and channel 1’ mix not logic) 0:by-pass 1:not
9:6	R/W	0	**NOD4_CTL** Index 1 node4 setting (channel 0’ and channel 1’ mix logic) 0:and 1:or 2:xor 3:add in byte 4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit)

Offset: 0xBC			Register Name: MP_ROPIDX1CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			7:channel 0' sub channel 1' in byte 8:channel 0' sub channel 1' in word (32bit) Other: Reserved
5	R/W	0	**NOD3_CTL** Index 1 node3 setting (channel 2' not logic) 0:by-pass 1:not
4	R/W	0	**NOD2_CTL** Index 1 node2 setting (channel 1' not logic) 0:by-pass 1:not
3	R/W	0	**NOD1_CTL** Index 1 node1 setting (channel 0' not logic) 0:by-pass 1:not
2:0	R/W	0	**NOD0_CTL** Index 1 node0 setting (sorting control) 0:012 1:021 2:102 3:120 4:201 5:210 Other: Reserved

Note: the result of the add or multiply operation will select the high 8 (byte operation) or 32bits (word operation).

3.1.4.22. ALPHA / COLOR KEY CONTROL REGISTER

Offset: 0xC0			Register Name: MP_ALPHACKCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0	**CK_REDCON**

Offset: 0xC0			Register Name: MP_ALPHACKCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Red control condition 0: if (R value of ck min color) <= (R value of layer0) <= (R value of ck max color), The red control condition is true, else the condition is false. 1: if (R value of ck min color) > (R value of layer0) or (R value of layer0) > (R value of ck max color), The red control condition is true, else the condition is false.
9	R/W	0	**CK_GREENCON** Green control condition 0: if (G value of ck min color) <= (G value of layer0) <= (G value of ck max color), The green control condition is true, else the condition is false. 1: if (G value of ck min color) > (G value of layer0) or (G value of layer0) > (G value of ck max color), The green control condition is true, else the condition is false.
8	R/W	0	**CK_BLUECON** Blue control condition 0: if (B value of ck min color) <= (B value of layer0) <= (B value of ck max color), The blue control condition is true, else the condition is false. 1: if (B value of ck min color) > (B value of layer0) or (B value of layer0) > (B value of ck max color), The blue control condition is true, else the condition is false.
7:5	/	/	/
4	R/W	0	**PRI** Priority selection 0: ROP output channel is higher than channel 3 1: Channel 3 is higher than ROP output channel
3	/	/	/
2:1	R/W	0	**ALPHACK_MOD** Alpha / Color key mode selection 0: alpha mode 1: color key mode, using the high priority layer as matching

Offset: 0xC0			Register Name: MP_ALPHACKCTL_REG
Bit	Read/Write	Default/Hex	Description
			condition, if it is true, the low priority layer pass. 2: color key mode, using the low priority layer as matching condition, if it is true, the high priority layer pass. 3: Reserved
0	R/W	0	**ALPHACK_EN** Enable control 0: the ROP data will by-pass the alpha/ck module 1: enable Note: if the module is disabled, the data of channel 3 will be ignored, and only the ROP data will pass through to CSC2 module.

3.1.4.23. COLOR KEY MIN COLOR REGISTER

Offset: 0xC4			Register Name: MP_CKMIN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	**CKMIN_R** Red
15:8	R/W	0	**CKMIN_G** Green
7:0	R/W	0	**CKMIN_B** Blue

3.1.4.24. COLOR KEY MAX COLOR REGISTER

Offset: 0xC8			Register Name: MP_CKMAX_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	**CKMAX_R**

Offset: 0xC8			Register Name: MP_CKMAX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Red
15:8	R/W	0	**CKMAX_G** Green
7:0	R/W	0	**CKMAX_B** Blue

3.1.4.25. FILL COLOR OF ROP OUTPUT SETTING REGISTER

Offset: 0xCC			Register Name: MP_ROPOUTFILLCOLOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	Alpha
23:16	R/W	0	Red
15:8	R/W	0	Green
7:0	R/W	0	Blue

3.1.4.26. COLOR SPACE CONVERTER 2 CONTROL REGISTER

Offset: 0xD0			Register Name: MP_CSC2CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0	**CSC2_EN** Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

3.1.4.27. OUTPUT CONTROL REGISTER

Offset: 0xE0			Register Name: MP_OUTCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0	**OUT_PS** Output data pixel sequence Reference output pixel sequence table
7	R/W	0	**RND_EN** Round enable 0:disabled 1:enabled
6:4	/	/	/
3:0	R/W	0	**OUT_FMT** Output data format 0x0: 32bpp – A8R8G8B8 or interleaved AYUV8888 0x1: 16bpp – A4R4G4B4 0x2: 16bpp – A1R5G5B5 0x3: 16bpp – R5G6B5 0x4: 16bpp – interleaved YUV422 0x5: planar YUV422 (UV combined) 0x6: planar YUV422 0x7: 8bpp – MONO 0x8: 4bpp – MONO 0x9: 2bpp – MONO 0xa: 1bpp – MONO 0xb: planar YUV420 (UV combined) 0xc: planar YUV420 0xd: planar YUV411 (UV combined) 0xe: planar YUV411 Other: reserved Note: In all YUV output data format, the CSC2 must be enabled, otherwise the output data mode will be 32bpp A8R8G8B8 mode.

Output data mode and output data ports mapping:

Output data mode	Output data channel selection		
	Channel 0	Channel 1	Channel 2
A8R8G8B8 or interleaved AYUV8888	ARGB or AYUV	Ignore	Ignore
A4R4G4B4	ARGB	Ignore	Ignore
A1R5G5B5	ARGB	Ignore	Ignore
R5G6B5	RGB	Ignore	Ignore
interleaved YUV422	YUV	Ignore	Ignore
planar YUV422 (UV combined)	Y	UV	Ignore
planar YUV422	Y	U	V
8bpp – MONO	MONO	Ignore	Ignore
4bpp – MONO	MONO	Ignore	Ignore
2bpp – MONO	MONO	Ignore	Ignore
1bpp – MONO	MONO	Ignore	Ignore
planar YUV420 (UV combined)	Y	UV	Ignore
planar YUV420	Y	U	V
planar YUV411 (UV combined)	Y	UV	Ignore
planar YUV411	Y	U	V

3.1.4.28. OUTPUT SIZE REGISTER

Offset: 0xE8			**Register Name: MP_OUTSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**OUT_HEIGHT** Height The value add 1 equal the actual output image height
15:11	/	/	/
12:0	R/W	0	**OUT_WIDTH** Width The value add 1 equal the actual output image width

3.1.4.29. OUTPUT ADDRESS HIGH 4BITS REGISTER

Offset: 0xEC			**Register Name: MP_OUTH4ADD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0	**OUTCH2_H4ADD**

Offset: 0xEC			Register Name: MP_OUTH4ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Output channel 2 High 4bits address in bits
15:12	/	/	/
11:8	R/W	0	**OUTCH1_H4ADD** Output channel 1 High 4bits address in bits
7:4	/	/	/
3:0	R/W	0	**OUTCH0_H4ADD** Output channel 0 High 4bits address in bits

3.1.4.30. OUTPUT ADDRESS LOW 32BITS REGISTER

Offset: Out channel 0:0xF0 Out channel 1:0xF4 Out channel 2:0xF8			Register Name: MP_OUTL32ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**OUT_L32ADD** Output channel Low 32bits address in bits

3.1.4.31. OUTPUT LINE WIDTH REGISTER

Offset: Out channel 0:0x100 Out channel 1:0x104 Out channel 2:0x108			Register Name: MP_OUTLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**OUT_LINEWIDTH** Output channel

Offset: Out channel 0:0x100 Out channel 1:0x104 Out channel 2:0x108			Register Name: MP_OUTLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Line width in bits

3.1.4.32. OUTPUT ALPHA CONTROL REGISTER

Offset: 0x120			**Register Name: MP_OUTALPHACTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**IMG_ALPHA** Output image area alpha value, the image area include A0,A1 and overlapping area A2.
23:16	R/W	0	**NONIMG_ALPHA** Output non-image area alpha value, the non-image area means the pure fill color area.
15:8	/	/	/
7:6	R/W	0	**A2ALPHACTL** A2 area alpha value control 0: using A0 self pixel alpha (A0pA) 1: using A1 self pixel alpha (A1pA) 2: the alpha value = A0pA + A1pA * (1 - A0pA) 3: using the Output image area alpha value (bit31:24)
5:4	R/W	0	**A3ALPHACTL** A3 area alpha value control 0: 0xff 1: using the Output non-image area alpha value (bit23:16) Other: reserved
3:2	R/W	0	**A1ALPHACTL** A1 area alpha value control 0: using A1 self pixel alpha 1: using the Output image area alpha value (bit31:24) Other: reserved
1:0	R/W	0	**A0ALPHACTL**

Offset: 0x120			Register Name: MP_OUTALPHACTL_REG
Bit	Read/Write	Default/Hex	Description
			A0 area alpha value control 0: using A0 self pixel alpha 1: using the Output image area alpha value (bit31:24) Other: reserved

Description:
There is some area in output memory block:

The alpha / color key module is enabled:
Only the high priority image area is called A0
Only the low priority image area is called A1
The high priority and low priority mixed image area is called A2
The other area is called A3
And the A0,A1,A2 is called image area, the A3 is called non-image area.

The alpha / color key module is disabled:
Only the ROP output image area is called A0, A0 is called image area.
The other area is called A3, A3 is called non-image area.

Note: the register setting is only valid in ARGB or AYUV mode.

3.1.4.33. CSC0/1 Y/G COEFFICIENT REGISTER

Offset: G/Y component: 0x180 R/U component: 0x184 B/V component: 0x188			Register Name: MP_ICSCYGCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x4a7 0x1e6f 0x1cbf	**CSC1_YGCOEF** the Y/G coefficient for CSC1 the value equals to coefficient*2^{10}
15:13	/	/	/

Offset: G/Y component: 0x180 R/U component: 0x184 B/V component: 0x188			Register Name: MP_ICSCYGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12:00	R/W	0x4a7 0x1e6f 0x1cbf	**CSC0_YGCOEF** the Y/G coefficient for CSC0 the value equals to coefficient*2^{10}

3.1.4.34. CSC0/1 Y/G CONSTANT REGISTER

Offset: 0x18C			Register Name: MP_ICSCYGCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x877	**CSC1_YGCONS** the Y/G constant for CSC1 the value equals to coefficient*2^4
15:14	/	/	/
13:00	R/W	0x877	**CSC0_YGCONS** the Y/G constant for CSC0 the value equals to coefficient*2^4

3.1.4.35. CSC0/1 U/R COEFFICIENT REGISTER

Offset: G/Y component: 0x190 R/U component: 0x194 B/V component: 0x198			Register Name: MP_ICSCURCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7 0x00	**CSC1_URCOEF** the U/R coefficient for CSC1

Offset: G/Y component: 0x190 R/U component: 0x194 B/V component: 0x198			Register Name: MP_ICSCURCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
		0x662	the value equals to coefficient*2^{10}
15:13	/	/	/
12:00	R/W	0x4a7 0x00 0x662	**CSC0_URCOEF** the U/R coefficient for CSC0 the value equals to coefficient*2^{10}

3.1.4.36. CSC0/1 U/R CONSTANT REGISTER

Offset: 0x19C			Register Name: MP_ICSCURCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x3211	**CSC1_URCONS** the U/R constant for CSC1 the value equals to coefficient*2^{4}
15:14	/	/	/
13:00	R/W	0x3211	**CSC0_URCONS** the U/R constant for CSC0 the value equals to coefficient*2^{4}

3.1.4.37. CSC0/1 V/B COEFFICIENT REGISTER

Offset: G/Y component: 0x1A0 R/U component: 0x1A4 B/V component: 0x1A8			Register Name: MP_ICSCVBCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7	**CSC1_VBCOEF**

Offset: G/Y component: 0x1A0 R/U component: 0x1A4 B/V component: 0x1A8			Register Name: MP_ICSCVBCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
		0x812 0x00	the V/B coefficient for CSC1 the value equals to coefficient*2^{10}
15:13	/	/	/
12:00	R/W	0x4a7 0x812 0x00	**CSC0_VBCOEF** the V/B coefficient for CSC0 the value equals to coefficient*2^{10}

3.1.4.38. CSC0/1 V/B CONSTANT REGISTER

Offset: 0x1AC			Register Name: MP_ICSCVBCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x2eb1	**CSC1_VBCONS** the V/B constant for CSC1 the value equals to coefficient*2^4
15:14	/	/	/
13:00	R/W	0x2eb1	**CSC0_VBCONS** the V/B constant for CSC0 the value equals to coefficient*2^4

3.1.4.39. CSC2 Y/G COEFFICIENT REGISTER

Offset: G/Y component: 0x1C0 R/U component: 0x1C4 B/V component: 0x1C8			Register Name: MP_OCSCYGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/

Offset: G/Y component: 0x1C0 R/U component: 0x1C4 B/V component: 0x1C8			Register Name: MP_OCSCYGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12:00	R/W		**CSC2_YGCOEF** the Y/G coefficient the value equals to coefficient*2^{10}

3.1.4.40. CSC2 Y/G CONSTANT REGISTER

Offset: 0x1CC			Register Name: MP_OCSCYGCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W		**CSC2_YGCONS** the Y/G constant the value equals to coefficient*2^{4}

3.1.4.41. CSC2 U/R COEFFICIENT REGISTER

Offset: G/Y component: 0x1D0 R/U component: 0x1D4 B/V component: 0x1D8			Register Name: MP_OCSCURCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W		**CSC2_URCOEF** the U/R coefficient the value equals to coefficient*2^{10}

3.1.4.42. CSC2 U/R CONSTANT REGISTER

Offset: 0x1DC			Register Name: MP_OCSCURCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W		**CSC2_URCONS** the U/R constant the value equals to coefficient*2^4

3.1.4.43. CSC2 V/B COEFFICIENT REGISTER

Offset: G/Y component: 0x1E0 R/U component: 0x1E4 B/V component: 0x1E8			Register Name: MP_OCSCVBCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W		**CSC2_VBCOEF** the V/B coefficient the value equals to coefficient*2^{10}

3.1.4.44. CSC2 V/B CONSTANT REGISTER

Offset: 0x1EC			Register Name: MP_OCSCVBCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
13:00	R/W		**CSC2_VBCONS** the V/B constant the value equals to coefficient*2^4

3.1.4.45. SCALING HORIZONTAL FILTERING COEFFICIENT RAM BLOCK

Offset: 0x200 – 0x27C			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0	Horizontal tap2 coefficient The value equals to coefficient*2^6
15:08	R/W	0	Horizontal tap1 coefficient The value equals to coefficient*2^6
07:00	R/W	0	Horizontal tap0 coefficient The value equals to coefficient*2^6

3.1.4.46. SCALING VERTICAL FILTERING COEFFICIENT RAM BLOCK

Offset: 0x280 – 0x2FC			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0	Vertical tap2 coefficient The value equals to coefficient*2^6
15:08	R/W	0	Vertical tap1 coefficient The value equals to coefficient*2^6
07:00	R/W	0	Vertical tap0 coefficient The value equals to coefficient*2^6

3.1.4.47. PALETTE TABLE

Offset: 0x400-0x7FF			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:08	R/W	UDF	Green value
07:00	R/W	UDF	Blue value

3.1.4.48. INPUT DATA PIXEL SEQUENCE TABLE

1-bpp mode

PS=xx00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23
P08	P09	P10	P11	P12	P13	P14	P15	P00	P01	P02	P03	P04	P05	P06	P07
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07	P06	P05	P04	P03	P02	P01	P00	P15	P14	P13	P12	P11	P10	P09	P08
P23	P22	P21	P20	P19	P18	P17	P16	P31	P30	P29	P28	P27	P26	P25	P24
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15
P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2-bpp mode

PS=xx00

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P15	P14	P13	P12	P11	P10	P09	P08
P07	P06	P05	P04	P03	P02	P01	P00
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=xx01

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P12	P13	P14	P15	P08	P09	P10	P11
P04	P05	P06	P07	P00	P01	P02	P03
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=xx10

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P03	P02	P01	P00	P07	P06	P05	P04
P11	P10	P09	P08	P15	P14	P13	P12
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=xx11

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P00	P01	P02	P03	P04	P05	P06	P07
P08	P09	P10	P11	P12	P13	P14	P15
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

4-bpp mode

PS=xx00

Bit

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16
P07	P06	P05	P04
P03	P02	P01	P00
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

PS=xx01

Bit

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16
P06	P07	P04	P05
P02	P03	P00	P01
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

PS=xx10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P01				P00				P03				P02			
P05				P04				P07				P06			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00				P01				P02				P03			
P04				P05				P06				P07			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

8-bpp mode

PS=xx00 / xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx01 / xx10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0								P1							
P2								P3							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

16-bpp @ A4R4G4B4 mode

PS=0x00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A1				R1				G1				B1			
A0				R0				G0				B0			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A0				R0				G0				B0			
A1				R1				G1				B1			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B1				G1				R1				A1			
B0				G0				R0				A0			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B0				G0				R0				A0			
B1				G1				R1				A1			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

16-bpp @ A1R5G5B5 mode

PS=0x00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A1	R1					G1					B1				
A0	R0					G0					B0				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A0	R0					G0					B0				
A1	R1					G1					B1				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B1					G1					R1					A1
B0					G0					R0					A0
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B0					G0					R0					A0

B1					G1					R1					A1
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

16-bpp @ R5G6B5 mode

PS=0x00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R1					G1						B1				
R0					G0						B0				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0					G0						B0				
R1					G1						B1				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

16-bpp @ interleaved YUV422 mode

PS=xx00 / xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V0								Y1							
U0								Y0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx01 / xx10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y1								V0							
Y0								U0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

16-bpp @ U8V8 mode

PS=xxxx

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V1								U1							

V0								U0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

32-bpp ARGB or AYUV mode

PS=xx00 / xx01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A								R (Y)							
G (U)								B (V)							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx10 / xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B (V)								G (U)							
R (Y)								A							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

3.1.4.49. OUTPUT DATA PIXEL SEQUENCE

32bpp – A8R8G8B8 or interleaved AYUV8888
16bpp – A4R4G4B4
16bpp – A1R5G5B5
16bpp – R5G6B5
16bpp – interleaved YUV422
Planar YUV422 (UV combined)
8bpp – MONO
4bpp – MONO
2bpp – MONO
1bpp – MONO
Planar YUV420 (UV combined)
Planar YUV411 (UV combined)

The above 13 kinds of output format is same as respective input format PS.

Planar YUV422
Planar YUV420
Planar YUV411

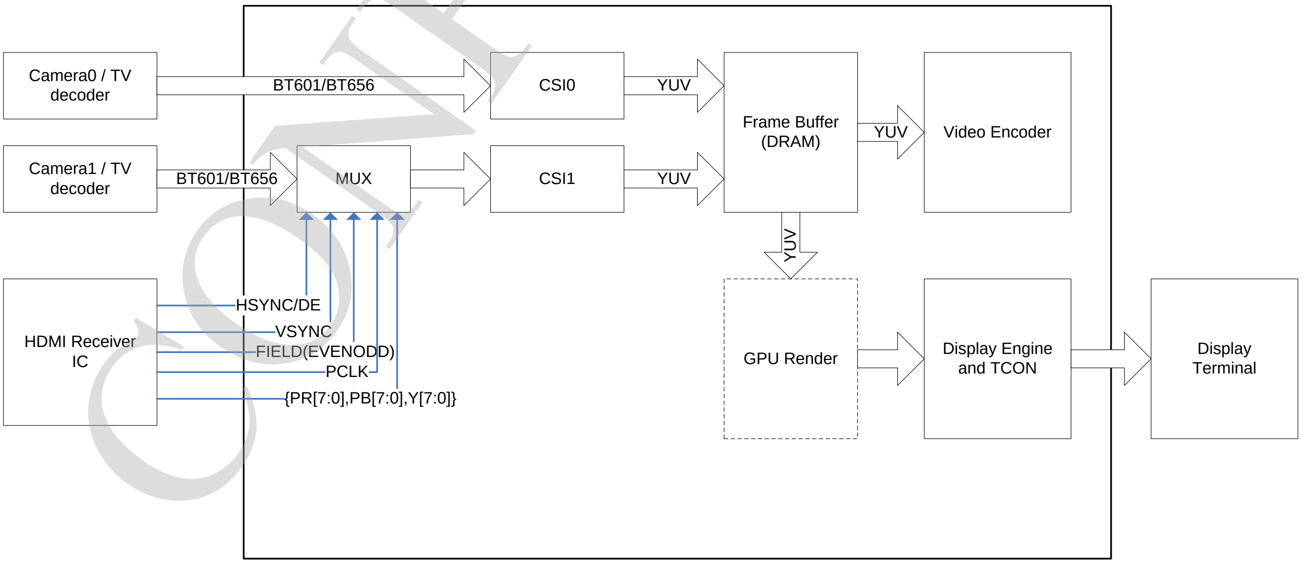
The above 3 kinds of output format are the same as input 8bpp format PS.

Chapter 4 Image

This chapter introduces the image section of A20 processor, including:

- CSI0
- CSI1
- TVD

Here is the CMOS sensor and TV decoder with YUV data process diagram：



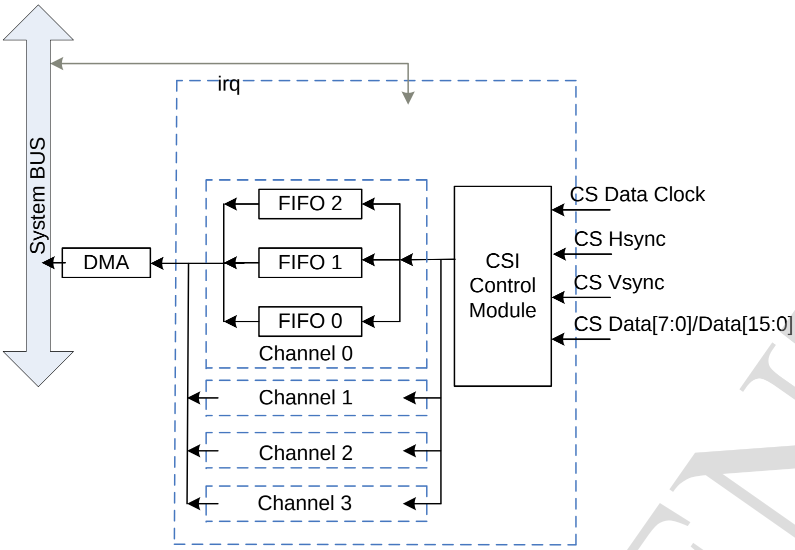
4.1. CSI0

4.1.1. Overview

CSI0 features:

- 8 bits input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Received data double buffer support
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or tiled Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software
- Support multi-channel ITU-R BT656 time-multiplexed format
- Luminance statistical value
- Support 8-bit raw data input
- Support 16-bit YUV422 data input

4.1.2. CSI0 Block Diagram



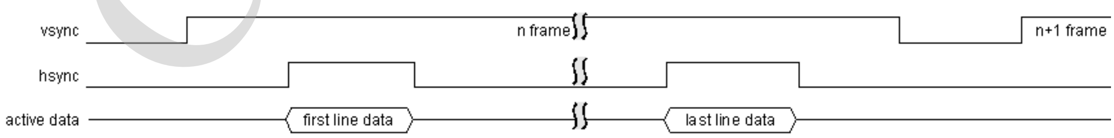
4.1.3. CSI0 Description

4.1.3.1. CSI DATA PORTS

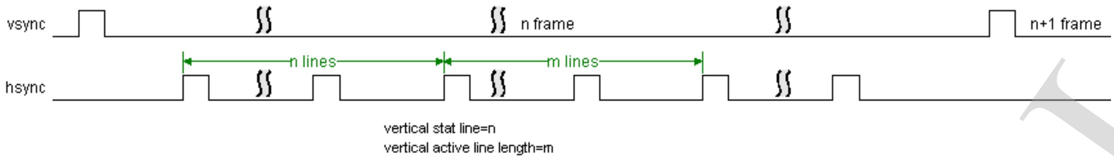
	Bayer	YCbCr (YUV)	Interlaced	Pass-through
FIFO0	Red pixel data	Y pixel data	All field 1 pixel data	All pixel data
FIFO1	Green pixel data	Cb (U) pixel data	All field 2 pixel data	-
FIFO2	Blue pixel data	Cr (V) pixel data	-	-

4.1.3.2. TIMING DIAGRAM

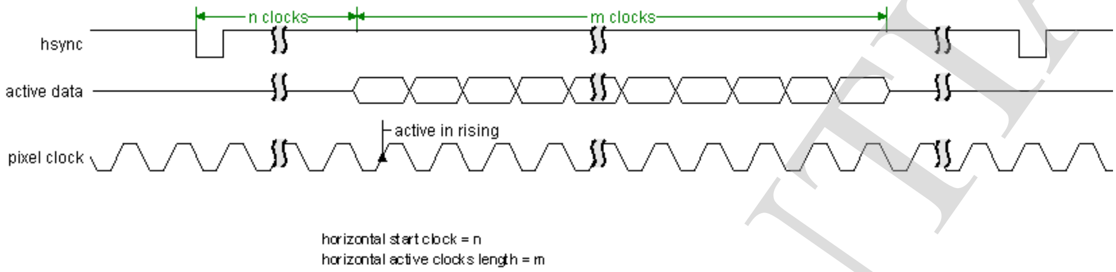
CSI timing



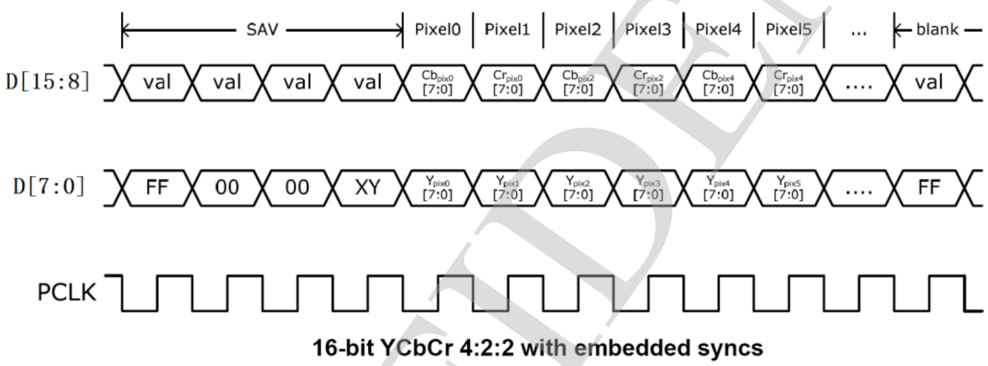
Vref= positive; Href= positive



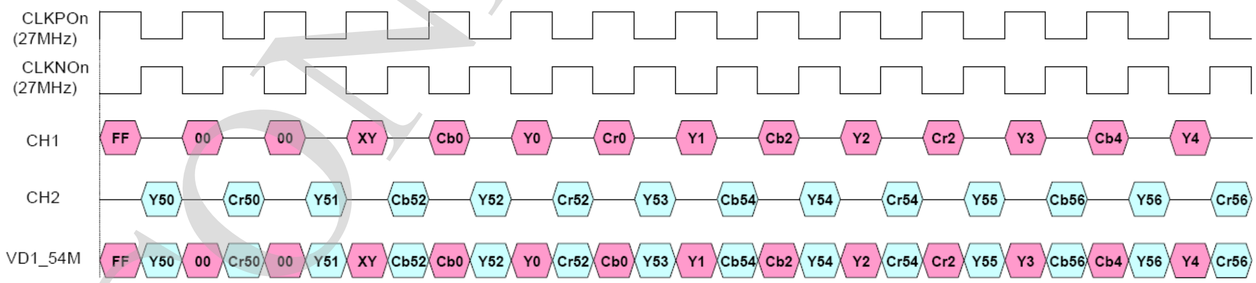
vertical size setting



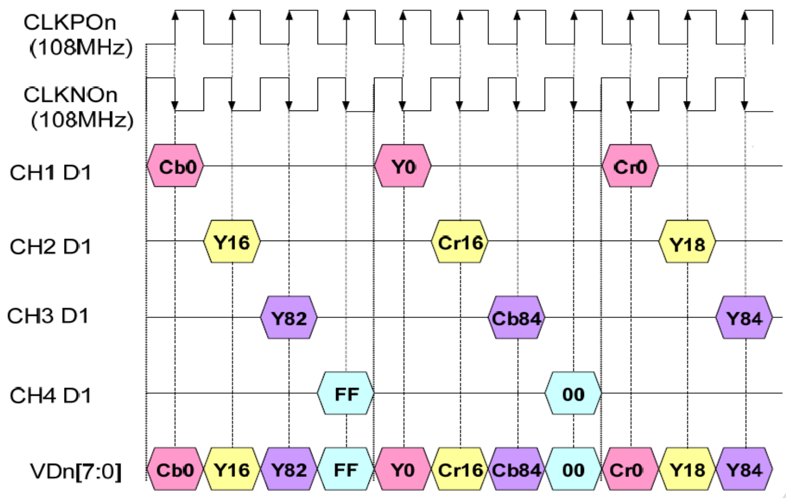
horizontal size setting and pixel clock timing(Href= positive)



16bit YUV422 Timing



CCIR656 2 channel Timing



CCIR656 4 channel Timing

CCIR656 Header Code

CCIR656 Header Data Bit Definition

Data Bit	**First Word(0xFF)**	**Second Word(0x00)**	**Third Word(0x00)**	**Fourth Word**
CS D[9] (MSB)	1	0	0	1
CS D[8]	1	0	0	F
CS D[7]	1	0	0	V
CS D[6]	1	0	0	H
CS D[5]	1	0	0	P3
CS D[4]	1	0	0	P2
CS D[3]	1	0	0	P1
CS D[2]	1	0	0	P0
CS D[1]	x	x	x	x
CS D[0]	x	x	x	x

For compatibility with an 8-bit interface, CS D[1] and CS D[0] are not defined.

Decode	**F**	**V**	**H**	**P3**	**P2**	**P1**	**P0**
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1

Decode	F	V	H	P3	P2	P1	P0
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

Multi-Channel:

Condition			656 FVH Value			SAV-EAV Code						
									Fourth			
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

4.1.4. CSI0 Register List

Module Name	Base Address
CSI0	0x01C09000

Register Name	Offset	Description
CSI0_EN_REG	0X000	CSI enable register
CSI0_CFG_REG	0X004	CSI configuration register
CSI0_CAP_REG	0X008	CSI capture control register
CSI0_SCALE_REG	0X00C	CSI scale register
CSI0_C0_F0_BUFA_REG	0X010	CSI Channel_0 FIFO 0 output buffer-A address register
CSI0_C0_F0_BUFB_REG	0X014	CSI Channel_0 FIFO 0 output buffer-B address register

Register Name	Offset	Description
CSI0_C0_F1_BUFA_REG	0X018	CSI Channel_0 FIFO 1 output buffer-A address register
CSI0_C0_F1_BUFB_REG	0X01C	CSI Channel_0 FIFO 1 output buffer-B address register
CSI0_C0_F2_BUFA_REG	0X020	CSI Channel_0 FIFO 2 output buffer-A address register
CSI0_C0_F2_BUFB_REG	0X024	CSI Channel_0 FIFO 2 output buffer-B address register
CSI0_C0_BUF_CTL_REG	0X028	CSI Channel_0 output buffer control register
CSI0_C0_BUF_STA_REG	0X02C	CSI Channel_0 status register
CSI0_C0_INT_EN_REG	0X030	CSI Channel_0 interrupt enable register
CSI0_C0_INT_STA_REG	0X034	CSI Channel_0 interrupt status register
CSI0_C0_HSIZE_REG	0X040	CSI Channel_0 horizontal size register
CSI0_C0_VSIZE_REG	0X044	CSI Channel_0 vertical size register
CSI0_C0_BUF_LEN_REG	0X048	CSI Channel_0 line buffer length register
CSI0_C1_F0_BUFA_REG	0X110	CSI Channel_1 FIFO 0 output buffer-A address register
CSI0_C1_F0_BUFB_REG	0X114	CSI Channel_1 FIFO 0 output buffer-B address register
CSI0_C1_F1_BUFA_REG	0X118	CSI Channel_1 FIFO 1 output buffer-A address register
CSI0_C1_F1_BUFB_REG	0X11C	CSI Channel_1 FIFO 1 output buffer-B address register
CSI0_C1_F2_BUFA_REG	0X120	CSI Channel_1 FIFO 2 output buffer-A address register
CSI0_C1_F2_BUFB_REG	0X124	CSI Channel_1 FIFO 2 output buffer-B address register
CSI0_C1_BUF_CTL_REG	0X128	CSI Channel_1 output buffer control register
CSI0_C1_BUF_STA_REG	0X12C	CSI Channel_1 status register
CSI0_C1_INT_EN_REG	0X130	CSI Channel_1 interrupt enable register
CSI0_C1_INT_STA_REG	0X134	CSI Channel_1 interrupt status register
CSI0_C1_HSIZE_REG	0X140	CSI Channel_1 horizontal size register
CSI0_C1_VSIZE_REG	0X144	CSI Channel_1 vertical size register
CSI0_C1_BUF_LEN_REG	0X148	CSI Channel_1 line buffer length register
CSI0_C2_F0_BUFA_REG	0X210	CSI Channel_2 FIFO 0 output buffer-A address register
CSI0_C2_F0_BUFB_REG	0X214	CSI Channel_2 FIFO 0 output buffer-B address register
CSI0_C2_F1_BUFA_REG	0X218	CSI Channel_2 FIFO 1 output buffer-A address register
CSI0_C2_F1_BUFB_REG	0X21C	CSI Channel_2 FIFO 1 output buffer-B address register
CSI0_C2_F2_BUFA_REG	0X220	CSI Channel_2 FIFO 2 output buffer-A address register
CSI0_C2_F2_BUFB_REG	0X224	CSI Channel_2 FIFO 2 output buffer-B address register

Register Name	Offset	Description
CSI0_C2_BUF_CTL_REG	0X228	CSI Channel_2 output buffer control register
CSI0_C2_BUF_STA_REG	0X22C	CSI Channel_2 status register
CSI0_C2_INT_EN_REG	0X230	CSI Channel_2 interrupt enable register
CSI0_C2_INT_STA_REG	0X234	CSI Channel_2 interrupt status register
CSI0_C2_HSIZE_REG	0X240	CSI Channel_2 horizontal size register
CSI0_C2_VSIZE_REG	0X244	CSI Channel_2 vertical size register
CSI0_C2_BUF_LEN_REG	0X248	CSI Channel_2 line buffer length register
CSI0_C3_F0_BUFA_REG	0X310	CSI Channel_3 FIFO 0 output buffer-A address register
CSI0_C3_F0_BUFB_REG	0X314	CSI Channel_3 FIFO 0 output buffer-B address register
CSI0_C3_F1_BUFA_REG	0X318	CSI Channel_3 FIFO 1 output buffer-A address register
CSI0_C3_F1_BUFB_REG	0X31C	CSI Channel_3 FIFO 1 output buffer-B address register
CSI0_C3_F2_BUFA_REG	0X320	CSI Channel_3 FIFO 2 output buffer-A address register
CSI0_C3_F2_BUFB_REG	0X324	CSI Channel_3 FIFO 2 output buffer-B address register
CSI0_C3_BUF_CTL_REG	0X328	CSI Channel_3 output buffer control register
CSI0_C3_BUF_STA_REG	0X32C	CSI Channel_3 status register
CSI0_C3_INT_EN_REG	0X330	CSI Channel_3 interrupt enable register
CSI0_C3_INT_STA_REG	0X334	CSI Channel_3 interrupt status register
CSI0_C3_HSIZE_REG	0X340	CSI Channel_3 horizontal size register
CSI0_C3_VSIZE_REG	0X344	CSI Channel_3 vertical size register
CSI0_C3_BUF_LEN_REG	0X348	CSI Channel_3 line buffer length register

4.1.5. CSI0 Register Description

4.1.5.1. CSI ENABLE REGISTER

Offset: 0x0000			Register Name: CSI0_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:10	/	/	/

Offset: 0x0000			Register Name: CSI0_EN_REG
Bit	Read/ Write	Default/Hex	Description
9	R/W	0	PCLK_CNT Pclk count per frame
8	R/W	0	LUMA_EN Luma enable
7:5	/	/	/
4	R/W	0	NON16_ADD Non-16 add 0x00
3	R/W	0	RD_FIFO_EN Read fifo [3]fifo enable, fifo address[01c09800~01c09ffc]
2	R/W	0	FIELD_REV Ccir656 field_reverse
1	/	/	/
0	R/W	0	CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module

4.1.5.2. CSI CONFIGURATION REGISTER

Offset Address: 0X0004			Register Name: CSI0_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:20	R/W	3	INPUT_FMT Input data format 000: RAW stream 001: reserved 010: CCIR656(one channel) 011: YUV422 100: YUV422 16bit data bus 101: two channel CCIR656 110: reserved 111: four channel CCIR656

Offset Address: 0X0004			Register Name: CSI0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: pass-through When the input format is set CCIR656 interface 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1111: interlaced interleaved YCbCr422. In this mode, capturing interlaced input and output the interlaced fields from individual ports. Field 1 data will be wrote to FIFO0 output buffer and field 2 data will be wrote to FIFO1 output buffer. 1000: field tiled YCbCr 422 1001: field tiled YCbCr 420 1010: frame tiled YCbCr 420 1011: frame tiled YCbCr 422 When the input format is set YUV422 0000: planar YUV 422 0001: planar YUV 420 0100: planar YUV 422 UV combined 0101: planar YUV 420 UV combined 1000: tiled YUV 422 1001: tiled YUV 420
15:12	/	/	/
11:10	R/W	0	FIELD_SEL Field selection. Applies to CCIR656 interface only. 00: start capturing with field 1. 01: start capturing with field 2. 10: start capturing with either field.

Offset Address: 0X0004			Register Name: CSI0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 mode.
07:03	/	/	/
02	R/W	1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
01	R/W	0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
00	R/W	1	CLK_POL Data clock type 0: active in falling edge 1: active in rising edge

4.1.5.3. CSI CAPTURE CONTROL REGISTER

Offset Address: 0X0008			Register Name: CSI0_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:02	/	/	/
01	R/W	0	VCAP_ON Video capture control: Capture the video image data stream. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.

Offset Address: 0X0008			Register Name: CSI0_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
00	W	0	SCAP_ON Still capture control: Capture a single still image frame. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

4.1.5.4. CSI HORIZONTAL SCALE REGISTER

Offset Address: 0X000C			Register Name: CSI0_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	F	VER_MASK Vertical (line) mask. Every 4-line is a mask group. Bit 24 mask the first line, bit 25 mask the second line, and so on. Mask bit = 0 means discarding this line data.
23:16	/	/	/
15:00	R/W	FFFF	HOR_MASK Horizontal (datastream) mask. Every 16-byte is a mask group. Bit 0 mask the firest byte, bit 1 mask the second byte, and so on. Mask bit = 0 means discarding this byte from the datastream.

4.1.5.5. CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0010			Register Name: CSI0_C0_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F0_BUFA FIFO 0 output buffer-A address

4.1.5.6. CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0014			Register Name: CSI0_C0_F0_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F0_BUFB FIFO 0 output buffer-B address

4.1.5.7. CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0018			Register Name: CSI0_C0_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F1_BUFA FIFO 1 output buffer-A address

4.1.5.8. CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X001C			Register Name: CSI0_C0_F1_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F1_BUFB FIFO 1 output buffer-B address

4.1.5.9. CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0020			Register Name: CSI0_C0_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F2_BUFA FIFO 2 output buffer-A address

4.1.5.10. CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0024	Register Name: CSI0_C0_F2_BUFB_REG

Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C0F2_BUFB FIFO 2 output buffer-B address

4.1.5.11. CSI CHANNEL_0 OUTPUT BUFFER CONTROL REGISTER

Offset Address: 0X0028			Register Name: CSI0_C0_BUF_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R/W	0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
01	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
00	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

4.1.5.12. CSI CHANNEL_0 STATUS REGISTER

Offset Address: 0X002C			Register Name: CSI0_C0_BUF_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	R	0	LUM_STATIS luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done.

Offset Address: 0X002C			Register Name: CSI0_C0_BUF_STA_REG
Bit	Read/Write	Default/Hex	Description
			For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
07:02	/	/	/
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

4.1.5.13. CSI CHANNEL_0 INTERRUPT ENABLE REGISTER

Offset Address: 0X0030			Register Name: CSI0_C0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	/	PRTC_ERR_INT_EN
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow

Offset Address: 0X0030			Register Name: CSI0_C0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

4.1.5.14. CSI CHANNEL_0 INTERRUPT STATUS REGISTER

Offset Address: 0X0034			Register Name: CSI0_C0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	/	PRTC_ERR_PD

Offset Address: 0X0034			Register Name: CSI0_C0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

4.1.5.15. CSI CHANNEL_0 HORIZONTAL SIZE REGISTER

Offset Address: 0X0040			Register Name: CSI0_C0_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

4.1.5.16. CSI CHANNEL_0 VERTICAL SIZE REGISTER

Offset Address: 0X0044			Register Name: CSI0_C0_VSIZE_REG
Bit	Read/Write	Default/Hex	Description

Offset Address: 0X0044			Register Name: CSI0_C0_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

4.1.5.17. CSI CHANNEL_0 BUFFER LENGTH REGISTER

Offset Address: 0X0048			Register Name: CSI0_C0_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

4.1.5.18. CSI CHANNEL_1 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0110			Register Name: CSI0_C1_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F0_BUFA FIFO 0 output buffer-A address

4.1.5.19. CSI CHANNEL_1 FIFO 0 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0114			Register Name: CSI0_C1_F0_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F0_BUFB FIFO 0 output buffer-B address

4.1.5.20. CSI CHANNEL_1 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0118			Register Name: CSI0_C1_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C1F1_BUFA FIFO 1 output buffer-A address

4.1.5.21. CSI CHANNEL_1 FIFO 1 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X011C			Register Name: CSI0_C1_F1_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C1F1_BUFB FIFO 1 output buffer-B address

4.1.5.22. CSI CHANNEL_1 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0120			Register Name: CSI0_C1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C1F2_BUFA FIFO 2 output buffer-A address

4.1.5.23. CSI CHANNEL_1 FIFO 2 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0124			Register Name: CSI0_C1_F2_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C1F2_BUFB FIFO 2 output buffer-B address

4.1.5.24. CSI CHANNEL_1 OUTPUT BUFFER CONTROL REGISTER

Offset Address: 0X0128	Register Name: CSI0_C1_BUF_CTL_REG

Bit	Read/Write	Default/Hex	Description
31:03	/	/	/
02	R/W	0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
01	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
00	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

4.1.5.25. CSI CHANNEL_1 STATUS REGISTER

Offset Address: 0X012C			Register Name: CSI0_C1_BUF_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	R	0	LUM_STATIS luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
07:02	/	/	/
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress

Offset Address: 0X012C			Register Name: CSI0_C1_BUF_STA_REG
Bit	Read/Write	Default/Hex	Description
			Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

4.1.5.26. CSI CHANNEL_1 INTERRUPT ENABLE REGISTER

Offset Address: 0X0130			Register Name: CSI0_C1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	PRTC_ERR_INT_EN
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame

Offset Address: 0X0130			Register Name: CSI0_C1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			capturing data is wrote to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

4.1.5.27. CSI CHANNEL_1 INTERRUPT STATUS REGISTER

Offset Address: 0X0134			Register Name: CSI0_C1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	PRTC_ERR_PD
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

4.1.5.28. CSI CHANNEL_1 HORIZONTAL SIZE REGISTER

Offset Address: 0X0140			Register Name: CSI0_C1_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

4.1.5.29. CSI CHANNEL_1 VERTICAL SIZE REGISTER

Offset Address: 0X0144			Register Name: CSI0_C1_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

4.1.5.30. CSI CHANNEL_1 BUFFER LENGTH REGISTER

Offset Address: 0X0148			Register Name: CSI0_C1_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

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4.1.5.31. CSI CHANNEL_2 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0210			Register Name: CSI0_C2_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F0_BUFA FIFO 0 output buffer-A address

4.1.5.32. CSI CHANNEL_2 FIFO 0 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0214			Register Name: CSI0_C2_F0_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F0_BUFB FIFO 0 output buffer-B address

4.1.5.33. CSI CHANNEL_2 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0218			Register Name: CSI0_C2_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F1_BUFA FIFO 1 output buffer-A address

4.1.5.34. CSI CHANNEL_2 FIFO 1 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X021C			Register Name: CSI0_C2_F1_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F1_BUFB FIFO 1 output buffer-B address

4.1.5.35. CSI CHANNEL_2 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0220			Register Name: CSI0_C2_F2_BUFA_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F2_BUFA FIFO 2 output buffer-A address

4.1.5.36. CSI CHANNEL_2 FIFO 2 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0224			Register Name: CSI0_C2_F2_BUFB_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F2_BUFB FIFO 2 output buffer-B address

4.1.5.37. CSI CHANNEL_2 OUTPUT BUFFER CONTROL REGISTER

Offset Address: 0X0228			Register Name: CSI0_C2_BUF_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R/W	0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
01	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
00	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always

Offset Address: 0X0228			Register Name: CSI0_C2_BUF_CTL_REG
Bit	Read/Write	Default/Hex	Description
			selected by CSI module.

4.1.5.38. CSI CHANNEL_2 STATUS REGISTER

Offset Address: 0X022C			Register Name: CSI0_C2_BUF_STA_REG
Bit	Read/Write	Default/Hex	Description
31:08	R	0	LUM_STATIS luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
07:02	/	/	/
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

4.1.5.39. CSI CHANNEL_2 INTERRUPT ENABLE REGISTER

Offset Address: 0X0230			Register Name: CSI0_C2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description

Offset Address: 0X0230			Register Name: CSI0_C2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	PRTC_ERR_INT_EN
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

4.1.5.40. CSI CHANNEL_2 INTERRUPT STATUS REGISTER

Offset Address: 0X0234			Register Name: CSI0_C2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	~~0~~	PRTC_ERR_PD ~~Protection error~~
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

4.1.5.41. CSI CHANNEL_2 HORIZONTAL SIZE REGISTER

Offset Address: 0X0240			Register Name: CSI0_C2_HSIZE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**

Offset Address: 0X0240			Register Name: CSI0_C2_HSIZE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

4.1.5.42. CSI CHANNEL_2 VERTICAL SIZE REGISTER

Offset Address: 0X0244			Register Name: CSI0_C2_VSIZE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

4.1.5.43. CSI CHANNEL_2 BUFFER LENGTH REGISTER

Offset Address: 0X0248			Register Name: CSI0_C2_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

4.1.5.44. CSI CHANNEL_3 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0310	Register Name: CSI0_C3_F0_BUFA_REG

Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C3F0_BUFA FIFO 0 output buffer-A address

4.1.5.45. CSI CHANNEL_3 FIFO 0 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0314			Register Name: CSI0_C3_F0_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C3F0_BUFB FIFO 0 output buffer-B address

4.1.5.46. CSI CHANNEL_3 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0318			Register Name: CSI0_C3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C3F1_BUFA FIFO 1 output buffer-A address

4.1.5.47. CSI CHANNEL_3 FIFO 1 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X031C			Register Name: CSI0_C3_F1_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C3F1_BUFB FIFO 1 output buffer-B address

4.1.5.48. CSI CHANNEL_3 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0320	Register Name: CSI0_C3_F2_BUFA_REG

Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	C3F2_BUFA FIFO 2 output buffer-A address

4.1.5.49. CSI CHANNEL_3 FIFO 2 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0324			Register Name: CSI0_C3_F2_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F2_BUFB FIFO 2 output buffer-B address

4.1.5.50. CSI CHANNEL_3 OUTPUT BUFFER CONTROL REGISTER

Offset Address: 0X0328			Register Name: CSI0_C3_BUF_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R/W	0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
01	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
00	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

4.1.5.51. CSI CHANNEL_3 STATUS REGISTER

Offset Address: 0X032C			Register Name: CSI0_C3_BUF_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	R	0	LUM_STATIS luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
07:02	/	/	/
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

4.1.5.52. CSI CHANNEL_3 INTERRUPT ENABLE REGISTER

Offset Address: 0X0330			Register Name: CSI0_C3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN

Offset Address: 0X0330			Register Name: CSI0_C3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	PRTC_ERR_INT_EN
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

4.1.5.53. CSI CHANNEL_3 INTERRUPT STATUS REGISTER

Offset Address: 0X0334			Register Name: CSI0_C3_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/

Offset Address: 0X0334			Register Name: CSI0_C3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	/	/
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

4.1.5.54. CSI CHANNEL_3 HORIZONTAL SIZE REGISTER

Offset Address: 0X0340			Register Name: CSI0_C3_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

4.1.5.55. CSI CHANNEL_3 VERTICAL SIZE REGISTER

Offset Address: 0X0344			Register Name: CSI0_C3_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

4.1.5.56. CSI CHANNEL_3 BUFFER LENGTH REGISTER

Offset Address: 0X0348			Register Name: CSI0_C3_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

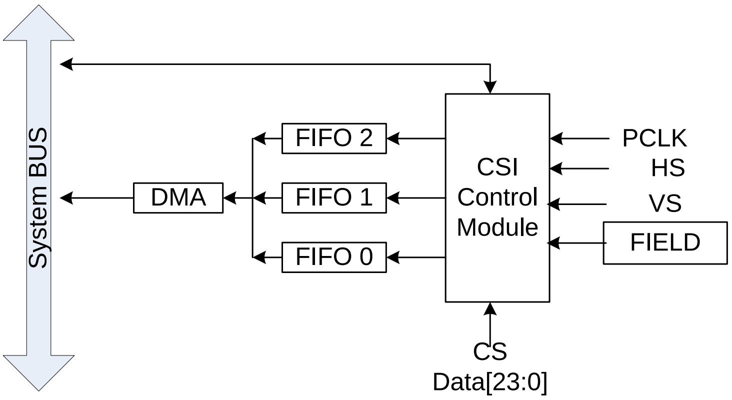
4.2. CSI1

4.2.1. Overview

The CSI1 module features:

- 8 bits input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Received data double buffer support
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or tiled Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software
- Support multi-channel ITU-R BT.656 time-multiplexed format
- Luminance statistical value
- Support 10-bit raw data input
- Support 24-bit RGB/YUV 444 input, interlace/progressive mode, pixel clock up to 148.5(1080p)

4.2.2. CSI1 Block Diagram

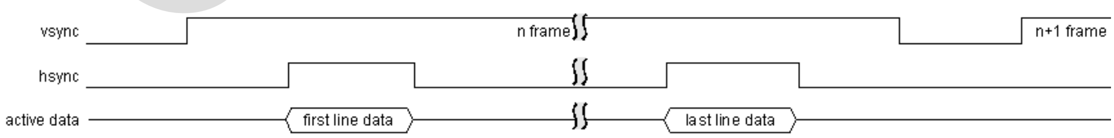


4.2.3. CSI1 Description

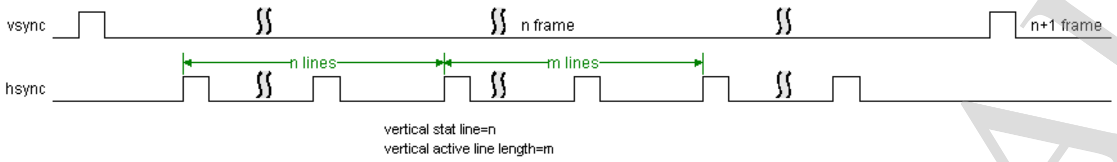
4.2.3.1. CSI DATA PORTS

	Bayer	YCbCr (YUV)	Interlaced	Pass-through
FIFO0	Red pixel data	Y pixel data	All field 1 pixel data	All pixel data
FIFO1	Green pixel data	Cb (U) pixel data	All field 2 pixel data	-
FIFO2	Blue pixel data	Cr (V) pixel data	-	-

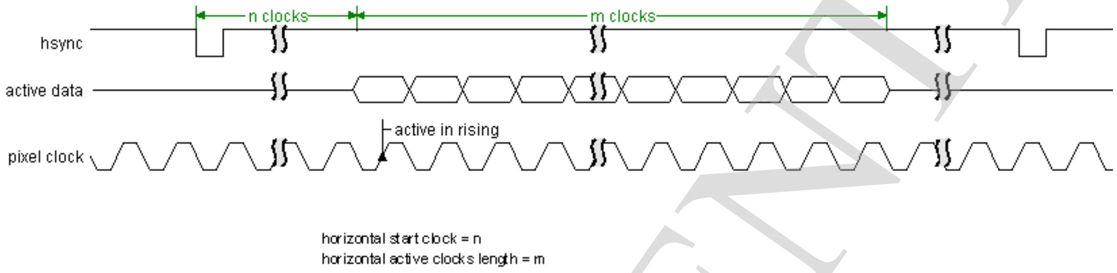
4.2.4. CSI1 Timing Diagram



Vref= positive; Href= positive



vertical size setting



horizontal size setting and pixel clock timing(Href= positive)

4.2.5. CSI1 Register List

Module Name	Base Address
CSI1	0x01C1D000

Register Name	Offset	Description
CSI1_EN_REG	0X000	CSI enable register
CSI1_CFG_REG	0X004	CSI configuration register
CSI1_CAP_REG	0X008	CSI capture control register
CSI1_SCALE_REG	0X00C	CSI scale register
CSI1_F0_BUFA_REG	0X010	CSI FIFO 0 output buffer-A address register
CSI1_F0_BUFB_REG	0X014	CSI FIFO 0 output buffer-B address register
CSI1_F1_BUFA_REG	0X018	CSI FIFO 1 output buffer-A address register

Register Name	Offset	Description
CSI1_F1_BUFB_REG	0X01C	CSI FIFO 1 output buffer-B address register
CSI1_F2_BUFA_REG	0X020	CSI FIFO 2 output buffer-A address register
CSI1_F2_BUFB_REG	0X024	CSI FIFO 2 output buffer-B address register
CSI1_BUF_CTL_REG	0X028	CSI output buffer control register
CSI1_BUF_STA_REG	0X02C	CSI status register
CSI1_INT_EN_REG	0X030	CSI interrupt enable register
CSI1_INT_STA_REG	0X034	CSI interrupt status register
CSI1_HSIZE_REG	0X040	CSI horizontal size register
CSI1_VSIZE_REG	0X044	CSI vertical size register
CSI1_BUF_LEN_REG	0X048	CSI line buffer length register

4.2.6. CSI1 Register Description

4.2.6.1. CSI ENABLE REGISTER

Offset: 0x0000			Register Name: CSI1_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0	PCLK_CNT Pclk count per frame
8	R/W	0	LUMA_EN Luma enable
7:5	/	/	/
4	R/W	0	NON16_ADD Non-16 add 0x00
3	R/W	0	RD_FIFO_EN

Offset: 0x0000			Register Name: CSI1_EN_REG
Bit	Read/ Write	Default/Hex	Description
			Read fifo [3]fifo enable, fifo address[01c09800~01c09ffc]
2	R/W	0	FIELD_REV Ccir656 field_reverse
1	/	/	/
0	R/W	0	CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module

4.2.6.2. CSI CONFIGURATION REGISTER

Offset Address: 0X0004			Register Name: CSI1_CFG_REG
Bit	Read/Write	Default/ Hex	Description
31:23	/	/	/
22:20	R/W	3	INPUT_FMT Input data format 000: RAW stream 001: reserved 010: CCIR656(one channel) 011: YUV422 100: YUV444({R, B, G} or {Pr, Pb, Y}) others: reserved

Offset Address: 0X0004			Register Name: CSI1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: pass-through When the input format is set CCIR656 interface 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1111: interlaced interleaved YCbCr422. In this mode, capturing interlaced input and output the interlaced fields from individual ports. Field 1 data will be wrote to FIFO0 output buffer and field 2 data will be wrote to FIFO1 output buffer. 1000: field tiled YCbCr 422 1001: field tiled YCbCr 420 1010: frame tiled YCbCr 420 1011: frame tiled YCbCr 422 When the input format is set YUV422 0000: planar YUV 422 0001: planar YUV 420 0100: planar YUV 422 UV combined 0101: planar YUV 420 UV combined 1000: tiled YUV 422 1001: tiled YUV 420 When the input format is set YUV444 1100: field planar YUV 444 1101: field planar YUV 422 UV combined 1110: frame planar YUV 444 1111: frame planar YUV 422 UV combined

Offset Address: 0X0004			Register Name: CSI1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	/	/	/
11:10	R/W	0	FIELD_SEL Field selection. Applies to CCIR656 interface only. 00: start capturing with field 1. 01: start capturing with field 2. 10: start capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 mode. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
07:05	/	/	/
4	R/W	0	FPS_DS Fps down sample(failed, no this code) 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames
3	R/W	0	FIELD_POL Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) This register is not applied to CCIR656 interface.
02	R/W	1	VREF_POL Vref polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
01	R/W	0	HERF_POL Href polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
00	R/W	1	CLK_POL

Offset Address: 0X0004			Register Name: CSI1_CFG_REG
Bit	Read/Write	Default/Hex	Description
			Data clock type 0: active in falling edge 1: active in rising edge

4.2.6.3. CSI CAPTURE CONTROL REGISTER

Offset Address: 0X0008			Register Name: CSI1_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:02	/	/	/
01	R/W	0	VCAP_ON Video capture control: Capture the video image data stream. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
00	W	0	SCAP_ON Still capture control: Capture a single still image frame. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

4.2.6.4. CSI HORIZONTAL SCALE REGISTER

Offset Address: 0X000C			Register Name: CSI0_SCALE_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

Offset Address: 0X000C			Register Name: CSI0_SCALE_REG
Bit	Read/Write	Default/Hex	Description
27:24	R/W	F	VER_MASK Vertical (line) mask. Every 4-line is a mask group. Bit 24 mask the first line, bit 25 mask the second line, and so on. Mask bit = 0 means discarding this line data.
23:16	/	/	/
15:00	R/W	FFFF	HOR_MASK Horizontal (datastream) mask. Every 16-byte is a mask group. Bit 0 mask the firest byte, bit 1 mask the second byte, and so on. Mask bit = 0 means discarding this byte from the datastream.

4.2.6.5. CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0010			Register Name: CSI1_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	F0_BUFA FIFO 0 output buffer-A address

4.2.6.6. CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0014			Register Name: CSI1_F0_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	F0_BUFB FIFO 0 output buffer-B address

4.2.6.7. CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0018	Register Name: CSI1_F1_BUFA_REG

Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	F1_BUFA FIFO 1 output buffer-A address

4.2.6.8. CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X001C			Register Name: CSI1_F1_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	F1_BUFB FIFO 1 output buffer-B address

4.2.6.9. CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0020			Register Name: CSI1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	F2_BUFA FIFO 2 output buffer-A address

4.2.6.10. CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-B ADDRESS REGISTER

Offset Address: 0X0024			Register Name: CSI1_F2_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	F2_BUFB FIFO 2 output buffer-B address

4.2.6.11. CSI CHANNEL_0 OUTPUT BUFFER CONTROL REGISTER

Offset Address: 0X0028			**Register Name: CSI1_BUF_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R/W	0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
01	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
00	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

4.2.6.12. CSI CHANNEL_0 STATUS REGISTER

Offset Address: 0X002C			**Register Name: CSI1_BUF_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	R	0	LUM_STATIS luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
07:02	/	/	/
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling

Offset Address: 0X002C			Register Name: CSI1_BUF_STA_REG
Bit	Read/Write	Default/Hex	Description
			video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

4.2.6.13. CSI CHANNEL_0 INTERRUPT ENABLE REGISTER

Offset Address: 0X0030			Register Name: CSI1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	PRTC_ERR_INT_EN
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset Address: 0X0030			Register Name: CSI1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

4.2.6.14. CSI CHANNEL_0 INTERRUPT STATUS REGISTER

Offset Address: 0X0034			Register Name: CSI1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	PRTC_ERR_PD
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow

Offset Address: 0X0034			Register Name: CSI1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

4.2.6.15. CSI CHANNEL_0 HORIZONTAL SIZE REGISTER

Offset Address: 0X0040			Register Name: CSI1_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

4.2.6.16. CSI CHANNEL_0 VERTICAL SIZE REGISTER

Offset Address: 0X0044			Register Name: CSI1_VSIZE_REG
Bit	Read/Write	Default/Hex	Description

Offset Address: 0X0044			Register Name: CSI1_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

4.2.6.17. CSI CHANNEL_0 BUFFER LENGTH REGISTER

Offset Address: 0X0048			Register Name: CSI1_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

4.3. TV Decoder

4.3.1. Overview

The TV decoder features:

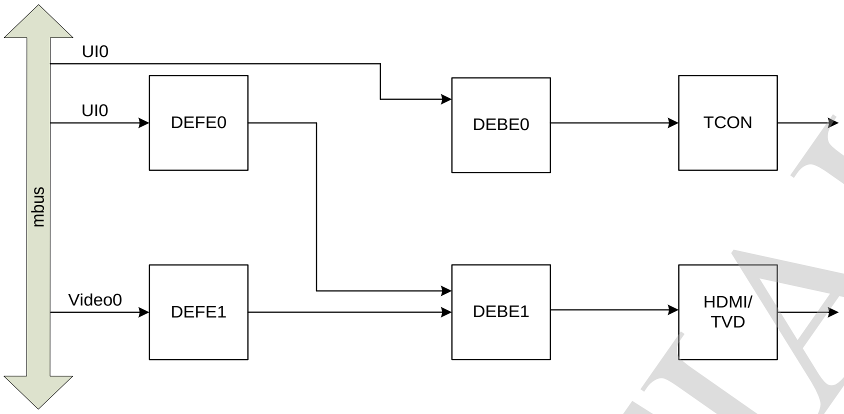
- All variations of analog PAL/NTSC standard supported
- CVBS, 480i, 576i, 480p, 576p supported
- 4-channel CVBS input with 1-channel 3D filter

Chapter 5 Display

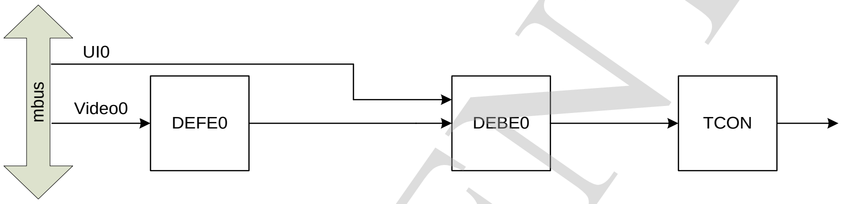
This chapter provides a detailed description of the display feature of A20 processor from following aspects:

- TCON
- HDMI
- DISPLAY ENGINE FRONTEND
- DISPLAY ENGINE FRONTEND
- TVE

Here is the application block diagram of display module:



DUAL DISPLAY



SINGLE DISPLAY

Allwinner Technology

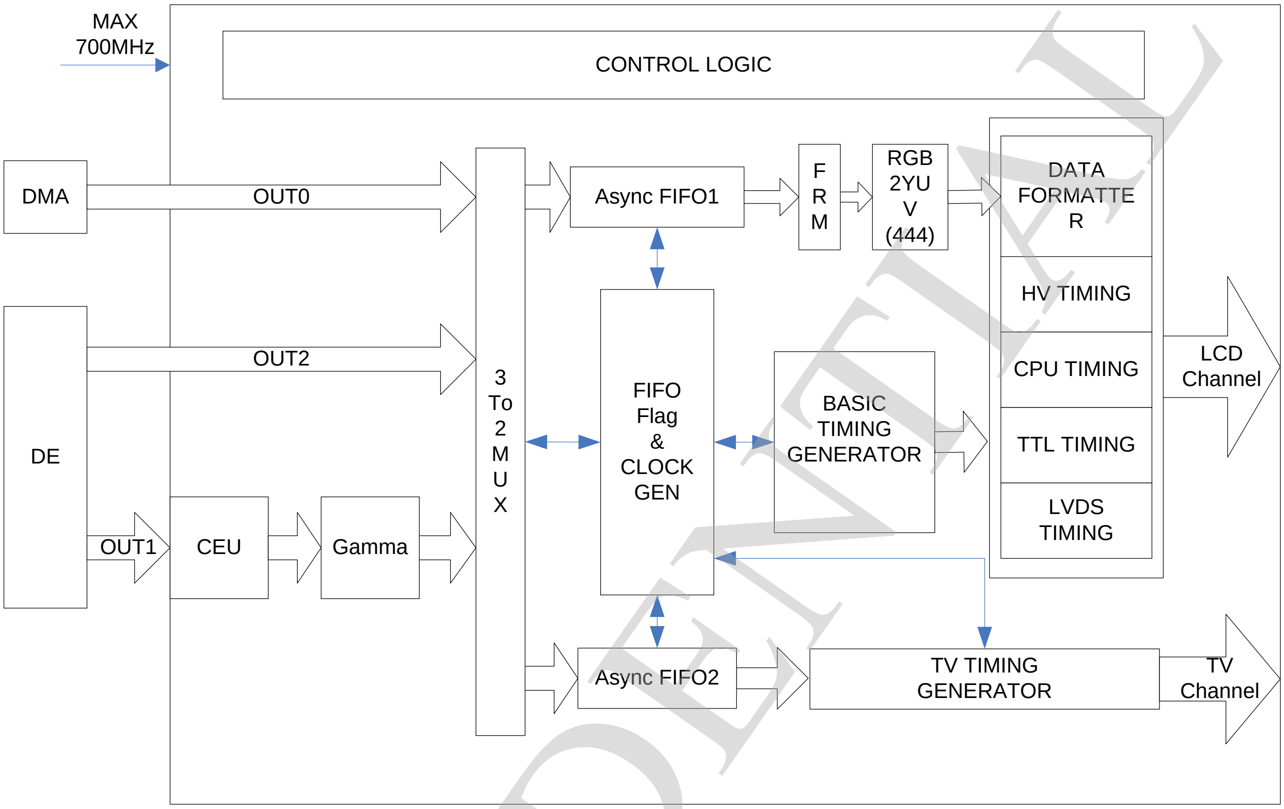
5.1. TCON

5.1.1. Overview

TheTCON features:

- Support dual-channel LCD output
- Support LVDS interface with single/dual link, up to 1920x1080@60fps
- Support RGB interface with DE/SYNC mode, up to 2048x1536@60fps
- Support serial RGB/dummy RGB/CCIR656 interface, up to 1280x720@60fps
- Support i80 interface with 18/16/9/8 bits, up to 1280x720@60fps
- Dither function for RGB666/RGB565/RGB888
- Gamma correction with R/G/B channel independence

5.1.2. TCON Block Diagram



5.1.3. TCON Register List

Module Name	Base Address
TCON0	0x01C0C000
TCON1	0x01C0D000

Register Name	Offset	Description
TCON_GCTL_REG	0x0000	TCON global control register
TCON_GINT0_REG	0x0004	TCON global interrupt register0
TCON_GINT1_REG	0x0008	TCON global interrupt register1
TCON_FRM_CTL_REG	0x0010	TCON FRM control register
TCON0_CTL_REG	0x0040	TCON0 control register
TCON0_DCLK_REG	0x0044	TCON0 data clock register
TCON0_BASIC0_REG	0x0048	TCON0 basic timing register0
TCON0_BASIC1_REG	0x004C	TCON0 basic timing register1
TCON0_BASIC2_REG	0x0050	TCON0 basic timing register2
TCON0_BASIC3_REG	0x0054	TCON0 basic timing register3
TCON0_HV_IF_REG	0x0058	TCON0 hv panel interface register
TCON0_CPU_IF_REG	0x0060	TCON0 cpu panel interface register
TCON0_CPU_WR_REG	0x0064	TCON0 cpu panel write data register
TCON0_CPU_RD0_REG	0x0068	TCON0 cpu panel read data register0
TCON0_CPU_RD1_REG	0x006C	TCON0 cpu panel read data register1
TCON0_TTL0_REG	0x0070	TCON0 ttl timing register0
TCON0_TTL1_REG	0x0074	TCON0 ttl timing register1
TCON0_TTL2_REG	0x0078	TCON0 ttl timing register2
TCON0_TTL3_REG	0x007C	TCON0 ttl timing register3
TCON0_TTL4_REG	0x0080	TCON0 ttl timing register4
TCON0_LVDS_IF_REG	0x0084	TCON0 lvds panel interface register
TCON0_IO_POL_REG	0x0088	TCON0 IO polarity register
TCON0_IO_TRI_REG	0x008C	TCON0 IO control register

Register Name	Offset	Description
TCON1_CTL_REG	0x0090	TCON1 control register
TCON1_BASIC0_REG	0x0094	TCON1 basic timing register0
TCON1_BASIC1_REG	0x0098	TCON1 basic timing register1
TCON1_BASIC2_REG	0x009C	TCON1 basic timing register2
TCON1_BASIC3_REG	0x00A0	TCON1 basic timing register3
TCON1_BASIC4_REG	0x00A4	TCON1 basic timing register4
TCON1_BASIC5_REG	0x00A8	TCON1 basic timing register5
TCON1_IO_POL_REG	0x00F0	TCON1 IO polarity register
TCON1_IO_TRI_REG	0x00F4	TCON1 IO control register
TCON_CEU_CTL_REG	0x0100	TCON CEU control register
TCON_CEU_MUL_RR_REG	0x0110	TCON CEU coefficient register0
TCON_CEU_MUL_RG_REG	0x0114	TCON CEU coefficient register1
TCON_CEU_MUL_RB_REG	0x0118	TCON CEU coefficient register2
TCON_CEU_ADD_RC_REG	0x011C	TCON CEU coefficient register3
TCON_CEU_MUL_GR_REG	0x0120	TCON CEU coefficient register4
TCON_CEU_MUL_GG_REG	0x0124	TCON CEU coefficient register5
TCON_CEU_MUL_GB_REG	0x0128	TCON CEU coefficient register6
TCON_CEU_ADD_GC_REG	0x012C	TCON CEU coefficient register7
TCON_CEU_MUL_BR_REG	0x0130	TCON CEU coefficient register8
TCON_CEU_MUL_BG_REG	0x0134	TCON CEU coefficient register9
TCON_CEU_MUL_BB_REG	0x0138	TCON CEU coefficient register10
TCON_CEU_ADD_BC_REG	0x013C	TCON CEU coefficient register11
TCON_CEU_RANGE_R_REG	0x0140	TCON CEU coefficient register12
TCON_CEU_RANGE_G_REG	0x0144	TCON CEU coefficient register13
TCON_CEU_RANGE_B_REG	0x0148	TCON CEU coefficient register14
TCON1_FILL_CTL_REG	0x0300	TCON1 fill data control register
TCON1_FILL_BEG0_REG	0x0304	TCON1 fill data begin register0
TCON1_FILL_END0_REG	0x0308	TCON1 fill data end register0
TCON1_FILL_DATA0_REG	0x030C	TCON1 fill data value register0
TCON1_FILL_BEG1_REG	0x0310	TCON1 fill data begin register1
TCON1_FILL_END1_REG	0x0314	TCON1 fill data end register1
TCON1_FILL_DATA1_REG	0x0318	TCON1 fill data value register1

Register Name	Offset	Description
TCON1_FILL_BEG2_REG	0x031C	TCON1 fill data begin register2
TCON1_FILL_END2_REG	0x0320	TCON1 fill data end register2
TCON1_FILL_DATA2_REG	0x0324	TCON1 fill data value register2
TCON1_GAMMA_TABLE_REG	0x0400	TCON1 gamma table register 0x400-0x7FF

5.1.4. TCON Register Description

5.1.4.1. TCON GLOBAL CONTROL REGISTER

Offset: 0x000			Register Name: TCON_GCTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**TCON_En** 0: disable 1: enable When it's disabled, the module will be reset to idle state.
30	R/W	0	**TCON_Gamma_En** 0: disable 1: enable
29:1	/	/	/
0	R/W	0	**IO_Map_Sel** 0: TCON0 1: TCON1 Note: this bit determined which IO_INV/IO_TRI are valid

5.1.4.2. TCON GLOBAL INTERRUPT REGISTER0

Offset: 0x004			Register Name: TCON_GINT0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**

Offset: 0x004			Register Name: TCON_GINT0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**TCON0_Vb_Int_En** 0: disable 1: enable
30	R/W	0	**TCON1_Vb_Int_En** 0: disable 1: enable
29	R/W	0	**TCON0_Line_Int_En** 0: disable 1: enable
28	R/W	0	**TCON1_Line_Int_En** 0: disable 1: enable
27:16	/	/	/
15	R/W	0	**TCON0_Vb_Int_Flag** Asserted during vertical no-display period every frame. Write 0 to clear it.
14	R/W	0	**TCON1_Vb_Int_Flag** Asserted during vertical no-display period every frame. Write 0 to clear it.
13	R/W	0	**TCON0_Line_Int_Flag** trigger when SY0 match the current TCON0 scan line Write 0 to clear it.
12	R/W	0	**TCON1_Line_Int_Flag** trigger when SY1 match the current TCON1 scan line Write 0 to clear it.
11:0	/	/	/

5.1.4.3. TCON GLOBAL INTERRUPT REGISTER1

Offset: 0x008			Register Name: TCON_GINT1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**

Offset: 0x008			Register Name: TCON_GINT1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:27	/	/	/
26:16	R/W	0	**TCON0_Line_Int_Num** scan line for TCON0 line trigger(including inactive lines) Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:11	/	/	/
10:0	R/W	0	**TCON1_Line_Int_Num** scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable.

5.1.4.4. TCON FRM CONTROL REGISTER

Offset: 0x010			Register Name: TCON_FRM_CTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**TCON0_Frm_En** 0:disable 1:enable
30:7	/	/	/
6	R/W	0	**TCON0_Frm_Mode_R** 0: 6bit frm output 1: 5bit frm output
5	R/W	0	**TCON0_Frm_Mode_G** 0: 6bit frm output 1: 5bit frm output
4	R/W	0	**TCON0_Frm_Mode_B** 0: 6bit frm output 1: 5bit frm output
3:2	/	/	/
1:0	R/W	0	/

5.1.4.5. TCON0 DATA CLOCK REGISTER

Offset: 0x044			Register Name: TCON0_DCLK REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:28	R/W	0	**TCON0_Dclk_En** LCLK_EN[3:0] :TCON0 clock enable 4'h0, 'h4,4'h6,4'ha7:dclk_en=0;dclk1_en=0;dclk2_en=0;dclkm2_en=0; 4'h1: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 4'h2: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 4'h3: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 4'h5: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 4'h8,4'h9,4'ha,4'hb,4'hc,4'hd,4'he,4'hf: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1;
27:7	/	/	/
6:0	R/W	0	**TCON0_Dclk_Div** Tdclk = Tsclk * DCLKDIV Note: 1.if dclk1&dclk2 used,DCLKDIV >=6 2.if dclk only,DCLKDIV >=4

5.1.4.6. TCON0 BASIC TIMING REGISTER0

Offset: 0x048			Register Name: TCON0_BASIC0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:27	/	/	/
26:16	R/W	0	**TCON0_X** Panel width is X+1
15:11	/	/	/

Offset: 0x048			Register Name: TCON0_BASIC0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
10:0	R/W	0	**TCON0_Y** Panel height is Y+1

5.1.4.7. TCON0 BASIC TIMING REGISTER1

Offset: 0x04C			Register Name: TCON0_BASIC1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**UF_En** 0: default 1: delay next line sync(Hsync in basic timing) until the FIFO1 is full Note: it must be used when FIFO depth is less than one line active pixels.
30:28	/	/	/
27:16	R/W	0	**HT** Thcycle = (HT+1) * Tdclk Note:1) parallel :HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:10	/	/	/
9:0	R/W	0	**HBP** horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

5.1.4.8. TCON0 BASIC TIMING REGISTER2

Offset: 0x050			Register Name: TCON0_BASIC2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**VT** TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2

Offset: 0x050			Register Name: TCON0_BASIC2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
15:10	/	/	/
9:0	R/W	0	**VBP** Tvbp = (VBP +1) * Thsync

5.1.4.9. TCON0 BASIC TIMING REGISTER3

Offset: 0x054			Register Name: TCON0_BASIC3_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:26	/	/	/
25:16	R/W	0	**HSPW** Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	**VSPW** Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

5.1.4.10. TCON0 HV PANEL INTERFACE REGISTER

Offset: 0x058			Register Name: TCON0_HV_IF_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**HV_Mode** 0: 24bit parallel mode 1: 8bit serial mode
30	R/W	0	**Serial_Mode** 0: 8bit/3cycle RGB serial mode(RGB888) 1: 8bit/2cycle YUV serial mode(CCIR656)
29:28	/	/	/
27:26	R/W	0	**RGB888_SM0**

Offset: 0x058			Register Name: TCON0_HV_IF_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
			serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7…) 00: R-->G-->B 01: B-->R-->G 10: G-->B-->R 11: R-->G-->B
25:24	R/W	0	**RGB888_SM1** serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…) 00: R-->G-->B 01: B-->R-->G 10: G-->B-->R 11: R-->G-->B
23:22	R/W	0	**YUV_SM** serial YUV mode Output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0	**YUV EAV/SAV F line delay** 0:F toggle right after active video line 1:delay 2 line(CCIR NTSC) 2:delay 3 line(CCIR PAL) 3:reserved
19:0	/	/	/

5.1.4.11. TCON0 CPU PANEL INTERFACE REGISTER

Offset: 0x060			Register Name: TCON0_CPU_IF_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	R/W	0	**CPU_MOD** 000: 18bit/256K mode 001: 16bit mode0

Offset: 0x060			Register Name: TCON0_CPU_IF_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
			010: 16bit mode1 011: 16bit mode2 100: 16bit mode3 101: 9bit mode 110: 8bit 256K mode 111: 8bit 65K mode
28	R/W	0	**AUTO** auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by Vsync
27	R/W	0	**FLUSH** direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
26	R/W	0	**DA** pin A1 value in 8080 mode auto/flash states
25	R/W	0	**CA** pin A1 value in 8080 mode WR/RD execute
24	R/W	0	**VSYNC_Cs_Sel** 0:CS 1:VSYNC
23	R	0	**Wr_Flag** 0:write operation is finishing 1:write operation is pending
22	R	0	**Rd_Flag** 0:read operation is finishing 1:read operation is pending
21:0	/	/	/

5.1.4.12. TCON0 CPU PANEL WRITE DATA REGISTER

Offset: 0x064	Register Name: TCON0_CPU_WR_REG

Bit	Read/ Write	Default/ Hex	Description
31:24	/	/	/
23:0	W	0	**Data_Wr** data write on 8080 bus, launch a write operation on 8080 bus

5.1.4.13. TCON0 CPU PANEL READ DATA REGISTER0

Offset: 0x068			Register Name: TCON0_CPU_RD0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R	/	**Data_Rd0** data read on 8080 bus, launch a new read operation on 8080 bus

5.1.4.14. TCON0 CPU PANEL READ DATA REGISTER1

Offset: 0x06C			Register Name: TCON0_CPU_RD1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R	/	**Data_Rd1** data read on 8080 bus, without a new read operation on 8080 bus

5.1.4.15. TCON0 TTL PANEL TIMING REGISTER 0

Offset: 0x070			Register Name: TCON0_TTL0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:20	R/W	0	**STVH** STV high plus width (in dclk) Tstvh = (STVH +1) * Tdclk Note: STV has a period of one frame

Offset: 0x070			Register Name: TCON0_TTL0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
19:0	R/W	0	**STVD** VSYNC-STV delay time Tstvd = STVD[19:10] * Thsync + STVD[9:0] * Tdclk

5.1.4.16. TCON0 TTTL PANEL TIMING REGISTER 1

Offset: 0x074			Register Name: TCON0_TTL1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:30	R/W	0	**CKVT** CKV period (in line) Tckvt = (CKVT +1) * Thsync
29:20	/	/	/
19:10	R/W	0	**CKVH** CKV high plus width (in dclk) Tckvh = (CKVH +1) * Tdclk
9:0	R/W	0	**CKVD** VSYNC –CKV delay time(in dclk) Tdskv = CKVD * Tdclk

5.1.4.17. TCON0 TTL PANEL TIMING REGISTER 2

Offset: 0x078			Register Name: TCON0_TTL2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:30	R/W	0	**OEVT** OEV period (in line) Toevt = (OEVT +1) * Thsync
29:20	/	/	/
19:10	R/W	0	**OEVH** OEV high plus width (in dclk)

Offset: 0x078			Register Name: TCON0_TTL2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
			Toevh = (OEVH + 1) * Tdclk
9:0	R/W	0	**OEVD** VSYNC –OEV delay time(in dclk) Toevd = OEVD * Tdclk

5.1.4.18. TCON0 TTL PANEL TIMING REGISTER3

Offset: 0x07C			Register Name: TCON0_TTL3_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:26	R/W	0	**STHH** STH high plus time(in dclk) Tsthh = (STHH+1) * Tdclk Note: STH has a period of one line
25:16	R/W	0	**STHD** HSYNC-STH delay time(in dclk) Tsthd = STHD * Tdclk
15:10	R/W	0	**OEHH** OEH high plus time(in dclk) Tldh = (OEHH+1) * Tdclk
9:0	R/W	0	**OEHD** HSYNC -OEH delay time(in dclk) Tldd = OEHD * Tdclk

5.1.4.19. TCON0 TTL PANEL TIMING REGISTER3

Offset: 0x080			Register Name: TCON0_TTL4_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23	R/W	0	**Output_Data_Rate**

Offset: 0x080			Register Name: TCON0_TTL4_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
			0: single data rate (SDR). LCD read data at the rising edge of clock 1: Double data rate (DDR). (The first data of every line must be ready at rising edge of CKH/CKH1/CKH2.) Note: When DATA_RATE = 1, HT and HBP had better be even number; CKH-CKH1 and CKH1-CKH2 delay time is always 1/3 Tdclk
22	R/W	0	**Rev_Sel** REV toggle mode 0:1H time toggle mode with frame inversion 1: Frame toggle mode Note: no matter in which mode, make sure REV has different polarity at the beginning of every frame (take VSYNC as reference).
21	R/W	0	**TTL_Data_Inv_En** 0: disable 1: data inverted ref to REV signal
20	R/W	0	**TTL_Data_Inv_Sel** TTL data invert mode 0: bit inverted when REV is 1 1: bit inverted when REV is 0
19:10	/	/	/
9:0	R/W	0	**REVD** HSYNC-REV delay time(in dclk) T_{revd} = REVD * T_{dclk} Note: 1. When **REV_SEL** is 0, REV has a 2H period with 50% duty. 2. When **REV_SEL** is 1, REV has a 2 Frame period with 50% duty. 3. Make sure REV has different polarity at the beginning of every frame(take VSYNC as reference).

5.1.4.20. TCON0 LVDS PANEL INTERFACE REGISTER

Offset: 0x084			Register Name: TCON0_LVDS_IF_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	TCON0_LVDS_En 0: disable 1: enable
30:29	/	/	/
28	R/W	0	TCON0_LVDS_Dir 1: normal 2: reverse NOTE: LVDS direction
27	R/W	0	TCON0_LVDS_Mode 0: NS mode 1: JEIDA mode
26	R/W	0	TCON0_LVDS_BitWidth 0: 24bit 1: 18bit
25:24	R/W	0	/
23	R/W	0	TCON0_LVDS_Correct_Mode 0: mode0 1: mode1
22:0	/	/	/

5.1.4.21. TCON0 IO POLARITY REGISTER

Offset: 0x088			Register Name: TCON0_IO_POL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:30	/	/	/
29:28	R/W	0	**DCLK_Sel** 00: used DCLK0(normal phase offset) 01: used DCLK1(1/3 phase offset) 10: used DCLK2(2/3 phase offset) 11: reserved

Offset: 0x088			Register Name: TCON0_IO_POL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
27	R/W	0	**IO3_Inv** 0: not invert 1: invert
26	R/W	0	**IO2_ Inv** 0: not invert 1: invert
25	R/W	0	**IO1_Inv** 0: not invert 1: invert
24	R/W	0	**IO0_Inv** 0: not invert 1: invert
23:0	R/W	0	**Data_Inv** TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

5.1.4.22. TCON0 IO CONTROL REGISTER

Offset: 0x08C			Register Name: TCON0_IO_TRI_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	1	**IO3_Output_Tri_En** 1: disable 0: enable
26	R/W	1	**IO2_Output_Tri_En** 1: disable 0: enable
25	R/W	1	**IO1_Output_Tri_En** 1: disable 0: enable

Offset: 0x08C			Register Name: TCON0_IO_TRI_REG
Bit	**Read/ Write**	**Default/H ex**	**Description**
24	R/W	1	**IO0_Output_Tri_En** 1: disable 0: enable
23:0	R/W	0xFFFFFF	**Data_Output_Tri_En** TCON0 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

5.1.4.23. TCON1 CONTROL REGISTER

Offset: 0x090			Register Name: TCON1_CTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**TCON1_En** 0: disable 1: enable
30:21	/	/	/
20	R/W	0	**Interlace_En** 0:disable 1:enable
19:9	/	/	/
8:4	R/W	0	**Start_Delay** This is for DE1 and DE2
3:2	/	/	/
1:0	R/W	0	**TCON1_Src_Sel** 00: DE CH1(FIFO2 enable) 01: DE CH2(FIFO2 enable) 1x: BLUE data(FIFO2 disable, RGB=0000FF)

5.1.4.24. TCON1 BASIC TIMING REGISTER0

Offset: 0x094			Register Name: TCON1_BASIC0_REG
Bit	Read/ Write	Default/ Hex	Description
31:28	/	/	/
27:16	R/W	0	**TCON1_XI** source width is X+1
15:12	/	/	/
11:0	R/W	0	**TCON1_YI** source height is Y+1

5.1.4.25. TCON1 BASIC TIMING REGISTER1

Offset: 0x098			Register Name: TCON1_BASIC1_REG
Bit	Read/ Write	Default/ Hex	Description
31:28	/	/	/
27:16	R/W	0	**LS_XO** width is LS_XO+1
15:12	/	/	/
11:0	R/W	0	**LS_YO** width is LS_YO+1 NOTE: this version LS_YO = TCON1_YI

5.1.4.26. TCON1 BASIC TIMING REGISTER2

Offset: 0x09C			Register Name: TCON1_BASIC2_REG
Bit	Read/ Write	Default/ Hex	Description
31:28	/	/	/
27:16	R/W	0	**TCON1_XO** width is TCON1_XO+1
15:12	/	/	/

Offset: 0x09C			Register Name: TCON1_BASIC2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
11:0	R/W	0	**TCON1_YO** height is TCON1_YO+1

5.1.4.27. TCON1 BASIC TIMING REGISTER3

Offset: 0x0A0			Register Name: TCON1_BASIC3_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**HT** horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0	**HBP** horizontal back porch Thbp = (HBP +1) * Thdclk

5.1.4.28. TCON1 BASIC TIMING REGISTER4

Offset: 0x0A4			Register Name: TCON1_BASIC4_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**VT** horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0	**VBP** horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

5.1.4.29. TCON1 BASIC TIMING REGISTER5

Offset: 0x0A8			Register Name: TCON1_BASIC5_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:26	/	/	/
25:16	R/W	0	**HSPW** horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	**VSPW** vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th Note: VT/2 > (VSPW+1)

5.1.4.30. TCON1 IO POLARITY REGISTER

Offset: 0x0F0			Register Name: TCON1_IO_POL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:28	/	/	/
27	R/W	0	**IO3_Inv** 0: not invert 1: invert
26	R/W	0	**IO2 Inv** 0: not invert 1: invert
25	R/W	0	**IO1_Inv** 0: not invert 1: invert
24	R/W	0	**IO0_Inv** 0: not invert 1: invert

Offset: 0x0F0			Register Name: TCON1_IO_POL_REG
Bit	Read/ Write	Default/ Hex	Description
23:0	R/W	0	**Data_Inv:**TCON1 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

5.1.4.31. TCON1 IO CONTROL REGISTER

Offset: 0x0F4			Register Name: TCON1_IO_TRI_REG
Bit	Read/ Write	Default/Hex	Description
31:28	/	/	/
27	R/W	1	**IO3_Output_Tri_En** 1: disable 0: enable
26	R/W	1	**IO2_Output_Tri_En** 1: disable 0: enable
25	R/W	1	**IO1_Output_Tri_En** 1: disable 0: enable
24	R/W	1	**IO0_Output_Tri_En** 1: disable 0: enable
23:0	R/W	0xFFFFFF	**Data_Output_Tri_En** TCON1 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

5.1.4.32. TCON CEU CONTROL REGISTER

Offset: 0x100			Register Name: TCON_CEU_CTL_REG
Bit	Read/ Write	Default/Hex	Description

Offset: 0x100			Register Name: TCON_CEU_CTL_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0	**CEU_en** 0: bypass 1: enable
30:0	/	/	/

5.1.4.33. TCON CEU COEFFICENT REGISTER

Offset: 0x110			Register Name: TCON_CEU_MUL_RR_REG
Bit	Read/ Write	Default/ Hex	Description
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x114			Register Name: TCON_CEU_MUL_RG_REG
Bit	Read/ Write	Default/ Hex	Description
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x118			Register Name: TCON_CEU_MUL_RB_REG
Bit	Read/ Write	Default/ Hex	Description
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x11c			Register Name: TCON_CEU_ADD_RC_REG
Bit	Read/ Write	Default/ Hex	Description
31:19	/	/	/

Offset: 0x11c			Register Name: TCON_CEU_ADD_RC_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
18:0	R/W	0	**Coef_Value** signed 19bit value, range of (-16384, 16384)

Offset: 0x120			Register Name: TCON_CEU_MUL_GR_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x124			Register Name: TCON_CEU_MUL_GG_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x128			Register Name: TCON_CEU_MUL_GB_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x12C			Register Name: TCON_CEU_ADD_GC_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:19	/	/	/
18:0	R/W	0	**Coef_Value** signed 19bit value, range of (-16384, 16384)

Offset: 0x130	Register Name: TCON_CEU_MUL_BR_REG

Bit	Read/ Write	Default/ Hex	Description
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x134			Register Name: TCON_CEU_MUL_BG_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x138			Register Name: TCON_CEU_MUL_BB_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0	**Coef_Value** signed 13bit value, range of (-16,16)

Offset: 0x13C			Register Name: TCON_CEU_ADD_BC_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:19	/	/	/
18:0	R/W	0	**Coef_Value** signed 19bit value, range of (-16384, 16384)

Offset: 0x140			Register Name: TCON_CEU_RANGE_R_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**Coef_Range_Min** unsigned 8bit value, range of [0,255]

Offset: 0x140			Register Name: TCON_CEU_RANGE_R_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
15:8	/	/	/
7:0	R/W	0	**Coef_Range_Max** unsigned 8bit value, range of [0,255]

Offset: 0x144			Register Name: TCON_CEU_RANGE_G_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**Coef_Range_Min** unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0	**Coef_Range_Max** unsigned 8bit value, range of [0,255]

Offset: 0x148			Register Name: TCON_CEU_RANGE_B_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**Coef_Range_Min** unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0	**Coef_Range_Max** unsigned 8bit value, range of [0,255]

5.1.4.34. TCON1 FILL DATA CONTROL REGISTER

Offset: 0x300			Register Name: TCON1_FILL_CTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	**TCON1_Fill_En:**

Offset: 0x300			Register Name: TCON1_FILL_CTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
			0: bypass 1: enable
30:0	/	/	/

5.1.4.35. TCON1 FILL DATA BEGIN REGISTER

Offset: 0x304			Register Name: TCON1_FILL_BEG0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_Begin

5.1.4.36. TCON1 FILL DATA END REGISTER

Offset: 0x308			Register Name: TCON1_FILL_END0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_End

5.1.4.37. TCON1 FILL DATA VALUE REGISTER

Offset: 0x30C			Register Name: TCON1_FILL_DATA0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_Value

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5.1.4.38. TCON1 FILL DATA BEGIN REGISTER

Offset: 0x310			Register Name: TCON1_FILL_BEG1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_Begin

5.1.4.39. TCON1 FILL DATA END REGISTER

Offset: 0x314			Register Name: TCON1_FILL_END1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_End

5.1.4.40. TCON1 FILL DATA VALUE REGISTER

Offset: 0x318			Register Name: TCON1_FILL_DATA1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_Value

5.1.4.41. TCON1 FILL DATA BEGIN REGISTER

Offset: 0x31C			Register Name: TCON1_FILL_BEG2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_Begin

5.1.4.42. TCON1 FILL DATA END REGISTER

Offset: 0x320			Register Name: TCON1_FILL_END2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_End

5.1.4.43. TCON1 FILL DATA VALUE REGISTER

Offset: 0x324			Register Name: TCON1_FILL_DATA2_REG
Bit	**Read/ Write**	**Default/H ex**	**Description**
31:24	/	/	/
23:0	R/W	0	Fill_Value

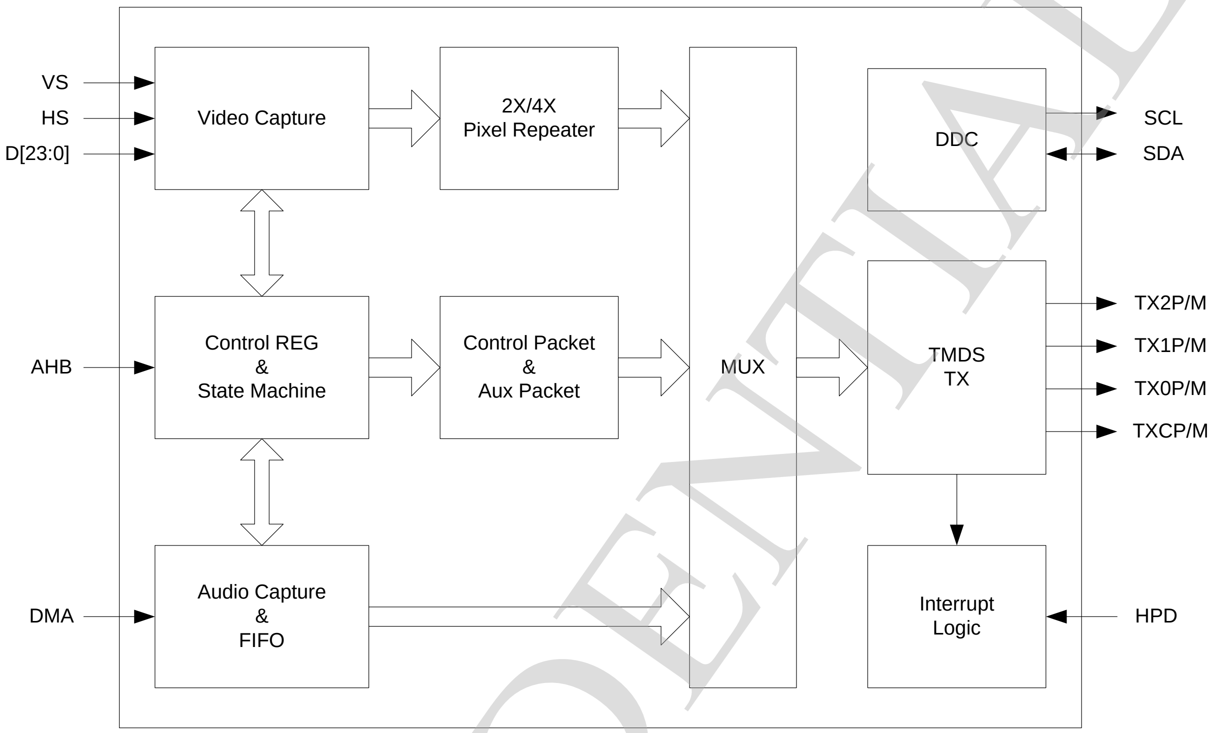
5.2. HDMI

5.2.1. Overview

The basic video and audio features:

- Comply with the HDMI v1.3 with HDCP
- Support up to 165M pixel per second
- Support 480i/576i/480p/576p/720p/1080i/1080p at 24/25/30/50/59.9Hz
- Support 1080p/24 3D output
- Support up to 8 channels, 24-bit PCM(IEC60958)
- Support IEC61937 compress audio formats
- Hardware receiver active sense and hot plug detection

5.2.2. HDMI Block Diagram



5.2.3. HDMI Control Register Description

Module Name	Base Address
HDMI	0x01C16000

Base address:

Register Name	Offset	Description
Version_ID	0x000	Version ID register
Ctrl	0x004	System control register
Int_Status	0x008	Interrupt register
HPD	0x00c	HDMI hot plug detect register
VID_Ctrl	0x010	Video control register
VID_Timing_0	0x014	Video timing register 0

Register Name	Offset	Description
VID_Timing_1	0x018	Video timing register 1
VID_Timing_2	0x01c	Video timing register 2
VID_Timing_3	0x020	Video timing register 3
VID_Timing_4	0x024	Video timing register 4
Aud_Ctrl	0x040	Audio control register
ADMA_Ctrl	0x044	Audio DMA&FIFO control register
Aud_Fmt	0x048	Audio Format control register
Aud_PCM_Ctrl	0x04c	Audio PCM control register
Aud_CTS	0x050	ACR CTS
Aud_N	0x054	ACR N
Aud_CH_Status0	0x058	Audio channel Status register 0
Aud_CH_Status1	0x05c	Audio channel Status register 1
AVI_Info_Pkt	0x080	AVI Info Frame
Aud_info_Pkt	0x0a0	Audio Info Frame
ACP_Pkt	0x0c0	ACP packet
GP_Pkt	0x0e0	General Control Packet
Pad Ctrl0	0x200	PLL/DRV Setting 0
Pad Ctrl1	0x204	PLL/DRV Setting 1
PLL_Ctrl	0x208	PLL/DRV Setting 2
PLL_Dbg0	0x20c	PLL/DRV Setting 3
PLL_Dbg1	0x210	PLL/DRV Setting 4
HPD_CEC	0x214	PLL/DRV Setting 5
SPD_Pkt	0x240	SPD packet
Pkt_Ctrl0	0x2f0	PACKET_CONTROL0
Pkt_Ctrl0	0x2f4	PACKET_CONTROL1
HDMI_DBG4	0x310	Audio sample counter
Aud_TX_FIFO	0x400	Audio Normal DMA Port
DDC_Ctrl	0x500	DDC Control Register
DDC_Slave_Addr	0x504	DDC Slave Address Register
DDC_Int_Mask	0x508	DDC Interrupt Mask Register
DDC_Int_Status	0x50C	DDC Interrupt Status Register
DDC_FIFO _Ctrl	0x510	DDC FIFO Control Register

Register Name	Offset	Description
DDC_FIFO_Status	0x514	DDC FIFO Status Register
DDC_FIFO_Access	0x518	DDC FIFO Access Register
DDC_Byte_Counter	0x51C	DDC Access Data Byte Number
DDC_Command	0x520	DDC Access Command Register
DDC_ExREG	0x524	DDC Extended Register
DDC_Clock	0x528	DDC Clock Register
DDC_DBG	0x540	DDC Slave Address Register

5.2.4. HDMI Register Description

5.2.4.1. HDMI VERSION ID

Offset: 0x000			Register name: Version_ID
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:16	R	0x0001	VER_ID_H: Version number of the core
15:0	R	0x0003	VER_ID_L: Version number of the core

5.2.4.2. SYSTEM CONTROL REGISTER

Offset: 0x004			Register name: Ctrl
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	R/W	0	MODULE_EN 0:disable 1:enable
30	R/W	0	HDCP_EN: 0:disable 1:reserved
29:2	/	/	reserved

Offset: 0x004			Register name: Ctrl
Bit	**Read/ Write**	**Default/ Hex**	**Description**
1	R/W	0	CLR_AVMUTE: General control packet Clear_AVMUTE flag
0	R/W	0	SET_AVMUTE: General control packet Set_AVMUTE flag

5.2.4.3. INTERRUPT STATUS REGISTER

Offset: 0x008			Register name: Int_Status
Bits	**Read /Write**	**Default /Hex**	**Description**
31:23	/	/	reserved
22	R/W	0	AUD_FIFO_UNDER_FLOW Mask 0: interrupt disable 1: interrupt enable
21	R/W	0	AUD_FIFO_OVER_FLOW Mask 0: interrupt disable 1: interrupt enable
20	R/W	0	AUD_TRANS_BUSY Mask 0: interrupt disable 1: interrupt enable
19:18	-	-	-
17	R/W	0	VID_FIFO_OVER_FLOW Mask 0: interrupt disable 1: interrupt enable
16	R/W	0	VID_FIFO_UNDER_FLOW Mask 0: interrupt disable 1: interrupt enable
15:7	/	/	reserved
6	R/Clea r	0	AUD_FIFO_UNDER_FLOW Audio input fifo under flow flag 0: normal 1: under flow happen

Offset: 0x008			Register name: Int_Status
Bits	Read /Write	Default /Hex	Description
5	R/Clear	0	AUD_FIFO_OVER_FLOW Audio input fifo over flow flag 0: normal 1: over flow happen
4	R/Clear	0	AUD_TRANS_BUSY Audio output transmit flag 0: audio data are transmitted as request 1: audio data are not transmitted as request
3:2	/	/	reserved
1	R/Clear	0	VID_FIFO_OVER_FLOW Video input fifo over flow flag 0: normal 1: over flow happen
0	R/Clear	0	VID_FIFO_UNDER_FLOW Video input fifo under flow flag 0: normal 1: under flow happen

5.2.4.4. HDMI HOT PLUG REGISTER

Offset: 0x00c			Register name: HPD
Bits	Read /Write	Default /Hex	Description
31:16	/	/	reserved
15	R	/	RX_ACTIVE_SENSE(PIN TX2+) 1: RX pull high 0: RX pull low
14	R	/	RX_ACTIVE_SENSE(PIN TX2-) 1: RX pull high 0: RX pull low
13	R	/	RX_ACTIVE_SENSE(PIN TX1+) 1: RX pull high

Offset: 0x00c			Register name: HPD
Bits	Read /Write	Default /Hex	Description
			0: RX pull low
12	R	/	RX_ACTIVE_SENSE(PIN TX1-) 1: RX pull high 0: RX pull low
11	R	/	RX_ACTIVE_SENSE(PIN TX0+) 1: RX pull high 0: RX pull low
10	R	/	RX_ACTIVE_SENSE(PIN TX0-) 1: RX pull high 0: RX pull low
9	R	/	RX_ACTIVE_SENSE(PIN TXC+) 1: RX pull high 0: RX pull low
8	R	/	RX_ACTIVE_SENSE(PIN TXC-) 1: RX pull high 0: RX pull low
7:1	/	/	reserved
0	R	0	HotPlug_DET 1: HPD Detect high 0: HPD Detect low

5.2.4.5. VIDEO CONTROL REGISTER

Offset: 0x010			Register name: VID_Ctrl
Bits	Read /Write	Default /Hex	Description
31	R/W	0	VIDEO_EN 0:Video module disable 1:Video module operating
30	R/W	0	HDMI_MODE: 0:DVI 1:HDMI

Offset: 0x010			Register name: VID_Ctrl
Bits	**Read /Write**	**Default /Hex**	**Description**
29:6	/	/	reserved
5	R/W	0	Video Source Selection 0: Video data from RGB inputs 1: Video data from embedded ColorBar Generator
4	R/W	0	VID_OUTPUT_FMT: video output format 0: progress 1: interlace
3:2	R/W	00	VID_COLOR_MODE: video output color mode 00: 24-bit RGB 01: 30-bit RGB 10: 36-bit RGB 11: 48-bit RGB
1:0	R/W	00	REPEATER_SEL: pixel repeater selection 00: normal 01: 2X 10: 4X 11: reserved

5.2.4.6. VIDEO TIMING REGISTER0

Offset: 0x014			Register name: VID_Timing_0
Bits	**Read /Write**	**Default /Hex**	**Description**
31:28	/	/	reserved
27:16	R/W	0	VID_ACT_V: Video active vertical resolution is : VID_ACT_V+1 pixels
15:12	/	/	reserved
11:0	R/W	0	VID_ACT_H:

Offset: 0x014			Register name: VID_Timing_0
Bits	Read /Write	Default /Hex	Description
			Video active horizontal resolution is: VID_ACT_H+1 pixels

5.2.4.7. VIDEO TIMING REGISTER1

Offset: 0x018			Register name: VID_Timing_1
Bits	Read /Write	Default /Hex	Description
31:28	/	/	reserved
27:16	R/W	0	VID_VBP: Vertical back porch is VID_VBP+1 TMDS clock
15:12	/	/	reserved
11:0	R/W	0	VID_HBP: Horizontal back porch is: VID_HBP+1 TMDS clock

5.2.4.8. VIDEO TIMING REGISTER2

Offset: 0x01c			Register name: VID_Timing_2
Bits	Read /Write	Default /Hex	Description
31:28	/	/	reserved
27:16	R/W	0	VID_VFP: Vertical front porch is: VID_VFP+1 TMDS clock
15:12	/	/	reserved
11:0	R/W	0	VID_HFP: Horizontal front porch is: VID_HFP+1 TMDS clock

5.2.4.9. VIDEO TIMING REGISTER3

Offset: 0x020			Register name: VID_Timing_3
Bits	Read /Write	Default /Hex	Description
31:28	/	/	reserved
27:16	R/W	0	VID_VSPW: Vertical sync plus width is: VID_VSPW+1 TMDS clock
15:12	/	/	reserved
11:0	R/W	0	VID_HSPW: Horizontal sync plus width is: VID_HSPW+1 TMDS clock

5.2.4.10. VIDEO TIMING REGISTER4

Offset: 0x024			Register name: VID_Timing_4
Bits	Read /Write	Default /Hex	Description
31:26	/	/	reserved
25:16	R/W	0	TX_CLOCK Note: normal 10'b11_1110_0000
15:2	/	/	reserved
1	R/W	0	VID_VSYNC_ACTIVE_SEL: Vsync priority selection 0: active low 1: active high
0	R/W	0	VID_HSYNC_ACTIVE_SEL: Hsync priority selection 0: active low 1: active high

5.2.4.11. AUDIO CONTROL REGISTER:

Offset: 0x040			Register name: Aud_Ctrl
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	AUD_EN: 0:disable 1:enable Audio module enable
30	R/W	0	AUD_RST: 0: normal 1: reset Audio module soft reset Write 1 to reset Audio module, and automatically clear to 0 after reset. Write 0 to this bit has no effect. Note: before change the audio parameters, first disable the AUD_EN, then write 1 to AUD_RST to reset the audio module, when this reset bit return to 0, then configure the parameters and enable the AUD_EN.
29:0	/	/	reserved

5.2.4.12. AUDIO DMA&FIFO CONTROL REGISTER:

Offset: 0x044			Register name: ADMA_Ctrl
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	Audio Source DMA Mode 0: dedicated DMA 1: normal DMA
30:26	/	/	reserved
25:24	R/W	0	DMA REQ CRTL 00: 1/2 FIFO empty

Offset: 0x044			Register name: ADMA_Ctrl
Bits	**Read /Write**	**Default /Hex**	**Description**
			01: 1/4 FIFO empty 10: 1/8 FIFO empty 11: reserved
23:20	/	/	reserved
19	R/W	0	AUD_SRC_DMA_SAMPLE_RATE: 0: 2 sample per transfer(only AUD_SRC_WORD_LEN = 00) 1: 1 sample per transfer
18	R/W	0	AUD_SRC SAMPLE_LAYOUT 0: LSB Align 1: MSB Align
17:16	R/W	0	AUD_SRC_WORD_LEN: 00: 16-bit 01: 20-bit 10: 24-bit 11: reserved
15	R/W	0	AUD_FIFO_CLEAR: Audio FIFO flush enable 0:normal 1:clear the audio input FIFO
14:1	/	/	reserved
0	R/W	0	AUD_DATA_SEL: 0: last sample 1: all 0's Audio data to send when FIFO is underflow

5.2.4.13. AUDIO FORMAT CONTROL REGISTER

Offset: 0x048			Register name: Aud_Fmt
Bits	**Read /Write**	**Default /Hex**	**Description**

Offset: 0x048			Register name: Aud_Fmt
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	Audio Source Selection 0: Audio data from DMA inputs 1: Audio data from embedded Audio Signal Generator Note: DMA input should be 32bit wide
30:26	/	/	reserved
26:24	R/W	0	AUD_FMT_SEL: Audio format selection 000: liner PCM 001: IEC61937 compress formats 010: HBR audio 011: one bit audio 1xx: reserved
23:5	/	/	reserved
4	R/W	0	DSD_FMT 0: LSB first 1:MSB first
3	R/W	0	AUD_LAYOUT: PCM/1-bit Audio layout selection 0: layout 0 (2 channels) 1: layout 1 (up to 8 channels)
2:0	R/W		PCM_SRC_CH_CFG(LPCM & One Bit Audio) Source pcm/1-bit audio configuration 000: 1channel 001: 2 channel 010: 3 channel 011: 4 channel 100: 5 channel 101: 6 channel 110: 7 channel 111: 8 channel Note: this only indicates how many channels of input PCM stream; it does not mean the sink can accept it. So the source should check the CA field of the audio info-frame to decide which channel will be output.

5.2.4.14. AUDIO PCM CONTROL REGISTER

Offset: 0x04c			Register name: Aud_PCM_Ctrl
Bits	**Read /Write**	**Default /Hex**	**Description**
31	/	/	reserved
30:28	R/W	7	PCM_CH7_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
27	/	/	reserved
26:24	R/W	6	PCM_CH6_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
23	/	/	reserved
22:20	R/W	5	PCM_CH5_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
19	/	/	reserved
18:16	R/W	4	PCM_CH4_MAP:

Offset: 0x04c			Register name: Aud_PCM_Ctrl
Bits	Read /Write	Default /Hex	Description
			000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
15	/	/	reserved
14:12	R/W	3	PCM_CH3_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
11	/	/	reserved
10:8	R/W	2	PCM_CH2_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
7	/	/	reserved
6:4	R/W	1	PCM_CH1_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample

Offset: 0x04c			Register name: Aud_PCM_Ctrl
Bits	Read /Write	Default /Hex	Description
			100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
3	/	/	reserved
2:0	R/W	0	PCM_CH0_MAP: 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample

5.2.4.15. AUDIO CTS REGISTER

Offset: 0x050			Register name: Aud_CTS
Bits	Read /Write	Default /Hex	Description
31:20	/	/	reserved
19:0	R/W	0	AUDIO_CLK_GEN_CTS Audio clock regeneration factor CTS

5.2.4.16. AUDIO N REGISTER

Offset: 0x054			Register name: Aud_N
Bits	Read /Write	Default /Hex	Description
31:20	/	/	reserved
19:0	R/W	0	AUDIO_CLK_GEN_N

Offset: 0x054			Register name: Aud_N
Bits	Read /Write	Default /Hex	Description
			Audio clock regeneration factor N

5.2.4.17. AUDIO PCM CHANNEL STATUS 0

Offset: 0x058			Register name: Aud_CH_Status0
Bits	Read /Write	Default /Hex	Description
31:30	R/W	0x00	CHNL_BIT1 (reserved)
29:28	R/W	0x00	CLK_ACCUR: Clock accuracy tolerance
27:24	R/W	0x00	FS_FREQ: Sampling frequency setting 0000 = 44.1 KHz 0010 = 48 KHz 0011 = 32 KHz 1000 = 88.2 KHz 1010 = 96 KHz 1100 =176.4 KHz 1110 = 192 KHz others = reserved
23:20	R/W	0x00	CH_NUM Channel number
19:16	R/W	0x00	SOURCE_NUM Source number
15:8	R/W	0x00	CATEGORY CODE Category code
7:6	R/W	0x00	MODE 00: Default Mode 01~11: Reserved
5:3	R/W	0x00	EMPHASIS Additional format information

Offset: 0x058			Register name: Aud_CH_Status0
Bits	Read /Write	Default /Hex	Description
			For bit 1 = "0", Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs / 15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = "1", other than Linear PCM applications: 000: Default state 001~111: Reseved
2	R/W	0x00	CP Copyright 0: copyright is asserted 1: no copyright is asserted
1	R/W	0x00	AUD_DATA_TYPE Audio Data Type 0: Linear PCM Samples 1: For none-linear PCM audio such as AC3, DTS, MPEG audio
0	R/W	0x00	APP_TYPE Application type 0: Consumer Application 1: Professional Application Note: This bit must be fixed to "0"

5.2.4.18. AUDIO PCM CHANNEL STATUS 1

Offset: 0x05c			Register name: Aud_CH_Status1
Bits	Read /Write	Default /Hex	Description
31:10	/	/	reserved
9:8	R/W	0x00	CGMS-A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used

Offset: 0x05c			Register name: Aud_CH_Status1
Bits	**Read /Write**	**Default /Hex**	**Description**
			11: No copying is permitted
7:4	R/W	0x00	ORIGINAL_FS Original sampling frequency 0000: not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x00	WORD_LEN Sample word length For bit 0 = “0”: 000: not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: not indicated 001: 20 bits 010: 22 bits 100: 23 bits

Offset: 0x05c			Register name: Aud_CH_Status1
Bits	**Read /Write**	**Default /Hex**	**Description**
			101: 24 bits 110: 21 bits
0	R/W	0x00	WORD_LEN_MAX Max word length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

Note: channel status is 192-bit, bits that not list above should set to 0

5.2.4.19. AVI_INFO_FRMAE_PACKET

Offset: 0x080			Register name: AVI_Info_Pkt
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x00	R/W	0x00	AVI_HB0 Packet type
0x01	R/W	0x00	AVI_HB1 Packet version
0x02	R/W	0x00	AVI_HB2 Packet length
0x03	R/W	0x00	AVI_PB0 checksum
0x04	R/W	0x00	AVI_PB1 AVI data byte 1
0x05	R/W	0x00	AVI_PB2 AVI data byte 2
0x06	R/W	0x00	AVI_PB3 AVI data byte 3
0x07	R/W	0x00	AVI_PB4 AVI data byte 4
0x08	R/W	0x00	AVI_PB5 AVI data byte 5
0x09	R/W	0x00	AVI_PB6

Offset: 0x080			Register name: AVI_Info_Pkt
BYTE	Read /Write	Default /Hex	Description
			AVI data byte 6
0x0a	R/W	0x00	AVI_PB7 AVI data byte 7
0x0b	R/W	0x00	AVI_PB8 AVI data byte 8
0x0c	R/W	0x00	AVI_PB9 AVI data byte 9
0x0d	R/W	0x00	AVI_PB10 AVI data byte 10
0x0e	R/W	0x00	AVI_PB11 AVI data byte 11
0x0f	R/W	0x00	AVI_PB12 AVI data byte 12
0x10	R/W	0x00	AVI_PB13 AVI data byte 13

5.2.4.20. AUDIO_INFO_FRMAE_PACKET

Offset: 0x0a0			Register name: Aud_info_Pkt
BYTE	Read /Write	Default /Hex	Description
0x00	R/W	0x00	**AUD_HB0** Packet type
0x01	R/W	0x00	**AUD_HB1** Packet version
0x02	R/W	0x00	**AUD_HB2** Packet length
0x03	R/W	0x00	**AUD_PB0** checksum
0x04	R/W	0x00	**AUD_PB1** AUD data byte 1

Offset: 0x0a0			Register name: Aud_info_Pkt
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x05	R/W	0x00	**AUD_PB2** AUD data byte 2
0x06	R/W	0x00	**AUD_PB3** AUD data byte 3
0x07	R/W	0x00	**AUD_PB4** AUD data byte 4
0x08	R/W	0x00	**AUD_PB5** AUD data byte 5
0x09	R/W	0x00	**AUD_PB6** AUD data byte 6
0x0a	R/W	0x00	**AUD_PB7** AUD data byte 7
0x0b	R/W	0x00	**AUD_PB8** AUD data byte 8
0x0c	R/W	0x00	**AUD_PB9** AUD data byte 9
0x0d	R/W	0x00	**AUD_PB10** AUD data byte 10

5.2.4.21. ACP_PACKET

Offset: 0x0c0			Register name: ACP_Pkt
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x00	R/W	0x00	ACP_HB1 ACP_Type
0x01	R/W	0x00	ACP_HB2 Reseved
0x02	R/W	0x00	ACP_PB0
0x03	R/W	0x00	ACP_PB1
0x04	R/W	0x00	ACP_PB2

Offset: 0x0c0			Register name: ACP_Pkt
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x05	R/W	0x00	ACP_PB3
0x06	R/W	0x00	ACP_PB4
0x07	R/W	0x00	ACP_PB5
0x08	R/W	0x00	ACP_PB6
0x09	R/W	0x00	ACP_PB7
0x0a	R/W	0x00	ACP_PB8
0x0b	R/W	0x00	ACP_PB9
0x0c	R/W	0x00	ACP_PB10
0x0d	R/W	0x00	ACP_PB11
0x0e	R/W	0x00	ACP_PB12
0x0f	R/W	0x00	ACP_PB13
0x10	R/W	0x00	ACP_PB14
0x11	R/W	0x00	ACP_PB15
0x12	R/W	0x00	ACP_EN 0: disable ACP packet TX 1: enable ACP packet TX

5.2.4.22. GENERAL_CONTROL_PACKET

Offset: 0x0e0-0x0e9			Register name: GP_Pkt
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x00	R/W	0x00	GCP_HB0 Packet type
0x01	R/W	0x00	GCP _HB1 Packet version
0x02	R/W	0x00	GCP _HB2 Packet length
0x03	R/W	0x00	GCP _PB0
0x04	R/W	0x00	GCP _PB1
0x05	R/W	0x00	GCP _PB2

Offset: 0x0e0-0x0e9			Register name: GP_Pkt
BYTE	Read /Write	Default /Hex	Description
0x06	R/W	0x00	GCP _PB3
0x07	R/W	0x00	GCP _PB4
0x08	R/W	0x00	GCP _PB5
0x09	R/W	0x00	GCP _PB6

5.2.4.23. SPD_PACKET

Offset: 0x240			Register name: SPD_Pkt
BYTE	Read /Write	Default /Hex	Description
0x00	R/W	0x00	USER_HB1
0x01	R/W	0x00	USER_HB2
0x02	R/W	0x00	USER_HB3
0x03	R/W	0x00	USER_PB0
0x04	R/W	0x00	USER_PB1
0x05	R/W	0x00	USER_PB2
0x06	R/W	0x00	USER_PB3
0x07	R/W	0x00	USER_PB4
0x08	R/W	0x00	USER_PB5
0x09	R/W	0x00	USER_PB6
0x0a	R/W	0x00	USER_PB7
0x0b	R/W	0x00	USER_PB8
0x0c	R/W	0x00	USER_PB9
0x0d	R/W	0x00	USER_PB10
0x0e	R/W	0x00	USER_PB11
0x0f	R/W	0x00	USER_PB12
0x10	R/W	0x00	USER_PB13
0x11	R/W	0x00	USER_PB14
0x12	R/W	0x00	USER_PB15

Offset: 0x240			Register name: SPD_Pkt
BYTE	Read /Write	Default /Hex	Description
0x13	R/W	0x00	USER_PB16
0x14	R/W	0x00	USER_PB17
0x15	R/W	0x00	USER_PB18
0x16	R/W	0x00	USER_PB19
0x17	R/W	0x00	USER_PB20
0x18	R/W	0x00	USER_PB21
0x19	R/W	0x00	USER_PB22
0x1a	R/W	0x00	USER_PB23
0x1b	R/W	0x00	USER_PB24
0x1c	R/W	0x00	USER_PB25
0x1d	R/W	0x00	USER_PB26
0x1e	R/W	0x00	USER_PB27

5.2.4.24. PLL/DRV SETTING 0: PAD CTRL0

Offset: 0x200			Register name: Pad_Ctrl0
Bits	Read /Write	Default /Hex	Description
31	R/W	0	BIASEN
30	R/W	0	LDOCEN
29	R/W	0	LDODEN
28	R/W	0	PWENC
27	R/W	0	PWEND
26	R/W	0	PWENG
25	R/W	0	CKEN
24	R/W	0	SEN
23	R/W	0	TXEN
22	R/W	0	Autosync_dis 0: enable auto sync 1:

Offset: 0x200			Register name: Pad_Ctrl0
Bits	**Read /Write**	**Default /Hex**	**Description**
21	R/W	0	Lsb_msb
20:0	/	/	reserved

5.2.4.25. PLL/DRV SETTING 1: PAD CTRL1

Offset: 0x204			Register name: Pad_Ctrl1
Bits	**Read /Write**	**Default /Hex**	**Description**
31:24	/	/	reserved
23	R/W	0	AMP_OPT
22	R/W	0	AMPCK_OPT
21	R/W	0	DMPOPT
20	R/W	0	EMP_OPT
19	R/W	0	EMPCK_OPT
18	R/W	0	PWSCK
17	R/W	0	PWSDT
16	R/W	0	REG_CSMPS
15	R/W	0	REG_DEN
14	R/W	0	REG_DENCK
13	R/W	0	REG_PLRCK
12:10	R/W	0	REG_EMP
9:8	R/W	0	REG_CD
7:6	R/W	0	REG_CKSS
5:3	R/W	0	REG_AMP
2:0	R/W	0	REG_PLR

5.2.4.26. PLL/DRV SETTING 2: PLL CTRL0

Offset: 0x208			Register name: PLL_Ctrl
Bits	Read /Write	Default /Hex	Description
31	R/W	0	PLL_EN
30	R/W	0	BWS
29	R/W	0	HV_IS_33
28	R/W	0	LDO1_EN
27	R/W	0	LDO2_EN
26	R/W	0	S6P25_7P5
25	R/W	0	SDIV2
24	R/W	0	SINT_FRAC
23	R/W	0	VCO_GAIN_EN
22:20	R/W	0	VCO_GAIN
19:17	R/W	0	S
16:12	R/W	0	CP_S
11:8	R/W	0	CS
7:4	R/W	0	PREDIV
3:0	R/W	0	VCO_S

5.2.4.27. PLL/DRV SETTING 3: PLL DBG0

Offset: 0x20c			Register name: PLL_Dbg0
Bits	Read /Write	Default /Hex	Description
31	R/W	0	PLL_DBG_EN
30:28	R/W	0	PSET
27:26	R/W	0	CLKSTEP
25:24	R/W	0	PDCLKSEL
23	R/W	0	S5_7
22	R/W	0	/
21	R/W	0	CKIN_SEL

Offset: 0x20c			Register name: PLL_Dbg0
Bits	Read /Write	Default /Hex	Description
20	R/W	0	VCO_RST_IN
19	R/W	0	VREG2_OUT_EN
18	R/W	0	VREG1_OUT_EN
17	R/W	0	REG_OD1
16	R/W	0	REG_OD
15:14	/	/	reserved
13:8	R/W	0	B_IN
7:6	/	/	reserved
5:0	R/W	0	CNT_INT

5.2.4.28. PLL/DRV SETTING 4: PLL DBG0

Offset: 0x210			Register name: PLL_Dbg1
Bits	Read /Write	Default /Hex	Description
31:25	/	/	reserved
24	R/W	0	Lock_flag2
23:17	/	/	reserved
16	R/W	0	Lock_flag1
15:10	/	/	reserved
9	R/W	0	Error_sf
8	R/W	0	Error_sfdet
7:6	/	/	reserved
5:0	R/W	0	PLL_BNSI

5.2.4.29. PLL/DRV SETTING 5: HPD/CEC

Offset: 0x214	Register name: HPD_CEC

Bits	Read /Write	Default /Hex	Description
31:12	/	/	reserved
11	R/W	0	REG_CEC_EN
10	R/W	0	REG_CECPS
9	R/W	0	W_CEC
8	R	/	R_CEC
7:4	/	/	reserved
3	R/W	0	REG_HPD_EN
2	R/W	0	REG_HPDPD
1	R/W	0	W_HPD
0	R	/	R_HPD

5.2.4.30. PACKET_CONTROL0

Offset: 0x2f0			Register name: Pkt_Ctrl0
Bits	**Read /Write**	**Default /Hex**	**Description**
31:28	R/W	0	Pkt_4_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved
27:24	R/W	0	Pkt_3_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32

Offset: 0x2f0			Register name: Pkt_Ctrl0
Bits	**Read /Write**	**Default /Hex**	**Description**
			6: 64 7: 128 Others: reserved
23:20	R/W	0	Pkt_2_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved
19:16	R/W	0	Pkt_1_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved
15:12	R/W	0	Pkt_4: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved

Offset: 0x2f0			Register name: Pkt_Ctrl0
Bits	**Read /Write**	**Default /Hex**	**Description**
11:8	R/W	0	Pkt_3: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
7:4	R/W	0	Pkt_2: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
3:0	R/W	0	Pkt_1: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end

Offset: 0x2f0			Register name: Pkt_Ctrl0
Bits	**Read /Write**	**Default /Hex**	**Description**
			Others: reserved

5.2.4.31. PACKET CONTROL1

Offset address: 0x2f4			Register name: Pkt_Ctrl1
Bits	**Read /Write**	**Default /Hex**	**Description**
31:28	R/W	0	Pkt_8_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved
27:24	R/W	0	Pkt_7_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved
23:20	R/W	0	Pkt_6_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16

Offset address: 0x2f4			Register name: Pkt_Ctrl1
Bits	**Read /Write**	**Default /Hex**	**Description**
			5: 32 6: 64 7: 128 Others: reserved
19:16	R/W	0	Pkt_5_freq(frame): 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved
15:12	R/W	0	Pkt_8: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
11:8	R/W	0	Pkt_7: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved)

Offset address: 0x2f4			Register name: Pkt_Ctrl1
Bits	**Read /Write**	**Default /Hex**	**Description**
			8: mpeg_info(reserved) 15:arbiter table end Others: reserved
7:4	R/W	0	Pkt_6: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
3:0	R/W	0	Pkt_5: 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved

5.2.4.32. AUDIO NORMAL DMA PORT

Offset: 0x400			Register name: Aud_TX_FIFO
Bits	**Read /Write**	**Default /Hex**	**Description**

Offset: 0x400			Register name: Aud_TX_FIFO
Bits	**Read /Write**	**Default /Hex**	**Description**
31:0	W	/	TX_FIFO Audio input FIFO port for normal DMA

Note: DMA assume that all sample data are organized as 32-bit/sub-frame.

5.2.4.33. DDC CONTROL REGISTER

Offset: 0x500			Register name: DDC_Ctrl
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	DDC_En
30	R/W	0	DDC Access Command Start Write 1 to this bit will start the DDC Access Command, and will auto clear when the command complete. Write '0' to this bit has no effect.
29:9	/	/	reserved
8	R/W	0	DDC_FIFO_Dir 0: read (HOST<=FIFO<=DEVICE) 1: write (HOST=>FIFO=>DEVICE) Note: This bit must be set before operation FIFO.
7:1	R	0	Reserved
0	R/W	0	DDC_SW_RST Write "1" to this bit will clear the DDC controller, and clear to 0 when completing soft reset operation

5.2.4.34. DDC SLAVE ADDRESS REGISTER

Offset: 0x504			Register name: DDC_Slave_Addr
Bits	**Read /Write**	**Default /Hex**	**Description**
31:24	R/W	0	Addr0 Segment pointer for E-DDC read operation

Offset: 0x504			Register name: DDC_Slave_Addr
Bits	**Read /Write**	**Default /Hex**	**Description**
23:16	R/W	0	Addr1 DDC address for E-DDC read operation
15:8	R/W	0	Addr2 Offset address to be sent for non-implicit read。「write operation.
6:0	R/W	0	Addr3 Slave Address

5.2.4.35. DDC INTERRUPT MASK REGISTER

Offset: 0x508			Register name: DDC_Int_Mask
Bits	**Read /Write**	**Default /Hex**	**Description**
31:6	/	/	reserved
7	R/W	0	Illegal_FIFO_Op_Int_Msk 0: disable 1: enable Illegal FIFO operation interrupt mask
6	R/W	0	DDC_FIFO_Underflow_Int_Mask 0: not underflow 1: underflow DDC FIFO underflow interrupt mask This bit is set when FIFO underflow in read operation. Write 1 to this bit will clear it
5	R/W	0	DDC_FIFO_Overflow_Int_Mask 0: not overflow 1: overflow This bit is set when FIFO overflow in write operation. Write 1 to this bit will clear it
4	R	0	DDC_FIFO_Request_Int_En This bit is set when FIFO level is below the TX trigger thresh in write operation, or when FIFO level is above the RX trigger thresh in read operation, write 1 to this bit will clear it. Note: this bit can only be set when correct FIFO direction is set.

Offset: 0x508			Register name: DDC_Int_Mask
Bits	**Read /Write**	**Default /Hex**	**Description**
3	R/W	0	DDC_Arbitration_Error_Int_Mask 0: disable 1: enable
2	R/W	0	DDC_ACK_Error_Int_Mask 0: disable 1: enable
1	R/W	0	DDC_Bus_Error_Int_Mask 0: disable 1: enable
0	R/W	0	DDC_Transfer_Complete_Int_Mask 0: disable 1: enable

5.2.4.36. DDC INTERRUPT STATUS REGISTER:

Offset: 0x50C			Register name: DDC_Int_Status
Bits	**Read /Write**	**Default /Hex**	**Description**
31:8	/	/	reserved
8	R	0	Interrupt_Clear_Status 0: Interrupt have be cleared 1: Interrupt clear is in process Note : When clear interrupt, must check this bit for clear complete
7	R/W	0	Illegal_FIFO_operation_interrupt_status_bit
6	R/W	0	DDC_RX FIFO_Underflow_Interrupt_Status_Bit 0: not underflow 1: underflow This bit is set when FIFO underflow Write 1 to this bit will clear it
5	R/W	0	DDC_TX FIFO_Overflow_Interrupt_Status_Bit 0: not overflow 1: overflow

Offset: 0x50C			Register name: DDC_Int_Status
Bits	Read /Write	Default /Hex	Description
			This bit is set when FIFO overflow Write 1 to this bit will clear it
4	R	0	DDC_FIFO_Request_Interrupt_Status_Bit This bit is set when TX FIFO level is below the TX trigger thresh in write operation, or when RX FIFO level is above the RX trigger thresh in read operation, write 1 to this bit will clear it.
3	R/W	0	DDC_ Arbitration_Error_Interrupt_Status_Bit
2	R/W	0	DDC_ACK_Error_Interrupt_Status_Bit
1	R/W	0	DDC_Bus_Error_Interrupt_Status_Bit
0	R/W	0	DDC_Transfer_Complete_Interrupt_Status_Bit

5.2.4.37. DDC FIFO CONTROL REGISTER

Offset: 0x510			Register name: DDC_FIFO _Ctrl
Bits	Read /Write	Default /Hex	Description
31	R/W	0	FIFO_Address_Clear Write ‘1’ to this bit will clear FIFO address, and auto clear to 0 when completing FIFO addresses clear operation.
30:9	/	/	Reserved
8	R/W	0	DMA_Request_En 0: disable 1: enable Note: this bit can only be set when correct FIFO direction is set
7:4	R/W	0	FIFO_RX_TRIGGER_THRESH When FIFO level is above this value in read mode, DMA request and FIFO request interrupt is assert if relative enable is on.
3:0	R/W	0	FIFO_TX_TRIGGER_THRESH When FIFO level is below this value in write mode, DMA request and FIFO request interrupt is assert if relative enable is on.

5.2.4.38. DDC FIFO STATUS REGISTER

Offset: 0x514			Register name: DDC_FIFO_Status
Bits	**Read /Write**	**Default /Hex**	**Description**
31:8	/	/	reserved
7	R	0	FIFO_Request_Ready FIFO level is below FIFO_TX_TRIGGER_THRESH in write mode or is above FIFO_RX_TRIGGER_THRESH in read mode,
6	R	0	FIFO_FULL
5	R	1	FIFO_EMPTY
4:0	R	0	FIFO_LEVEL

5.2.4.39. DDC FIFO ACCESS REGISTER

Offset: 0x518			Register name: DDC_FIFO_Access
Bits	**Read /Write**	**Default /Hex**	**Description**
31:0	R/W	0	DDC_FIFO_Access_Register Write only in DDC write operation, and read only in DDC read operation

5.2.4.40. DDC ACCESS DATA BYTE NUMBER

Offset: 0x51C			Register name: DDC_Byte_Counter
Bits	**Read /Write**	**Default /Hex**	**Description**
31:10	/	/	Reserved
9:0	R/W	0	DDC_Access_Data_Byte_Number

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5.2.4.41. DDC ACCESS COMMAND REGISTER

Offset: 0x520			Register name: DDC_Command
Bits	**Read /Write**	**Default /Hex**	**Description**
31:3	/	/	Reserved
2:0	R/W	0	DDC_Access_Command 000 = Abort Current Operation 001 = Special Offset Address Read 010 = Explicit Offset Address Write 011 = Implicit Offset Address Write 100 =Explicit Offset Address Read 101 =Implicit Offset Address Read 110 = Explicit Offset Address E-DDC Read 111 = Implicit Offset Address E-DDC Read

5.2.4.42. DDC EXTENDED REGISTER

Offset: 0x524			Register name: DDC_ExREG
Bits	**Read /Write**	**Default /Hex**	**Description**
31:11	/	/	Reserved
10	R	0	Bus_Busy
9	R	0	SDA_status
8	R	0	SCL_status
7:4	/	/	Reserved
3	R/W	0	DDC_SCL_LineState_Control_En 0: disable 1: enable
2	R/W	0	DDC_SCL_LineState_Control_Bit When DDC_SCL line state control enable is set to ‘1’, the value of this bit decide the output level of DDC_SCL 0: output low level 1: output high level
1	R/W	0	DDC_SDA _LineState_Control_Bit

Offset: 0x524			Register name: DDC_ExREG
Bits	Read /Write	Default /Hex	Description
			0: disable 1: enable
0	R/W	0	DDC_SDA_LineState_Control_Bit When DDC_ SDA line state control enable is set to '1', the value of this bit decide the output level of DDC_ SDA 0: output low level 1: output high level

5.2.4.43. DDC CLOCK REGISTER

Offset: 0x528			Register name: DDC_Clock
Bits	Read /Write	Default /Hex	Description
31:7	/	/	reserved
6:3	R/W	0	M Note: M is recommend set to value greater than 0.
2:0	R/W	0	N The DDC bus is sampled by the DCC at the frequency defined by F0: Fs =F0 = Fin/2^N The DDC output frequency is F1/10/: F1 = F0/(M+1) Foscl = F1/10 = Fin/(2^N * (M+1) *10 The source clock frequency is the f_{TMDS} /2.

5.3. Display Engine Frontend

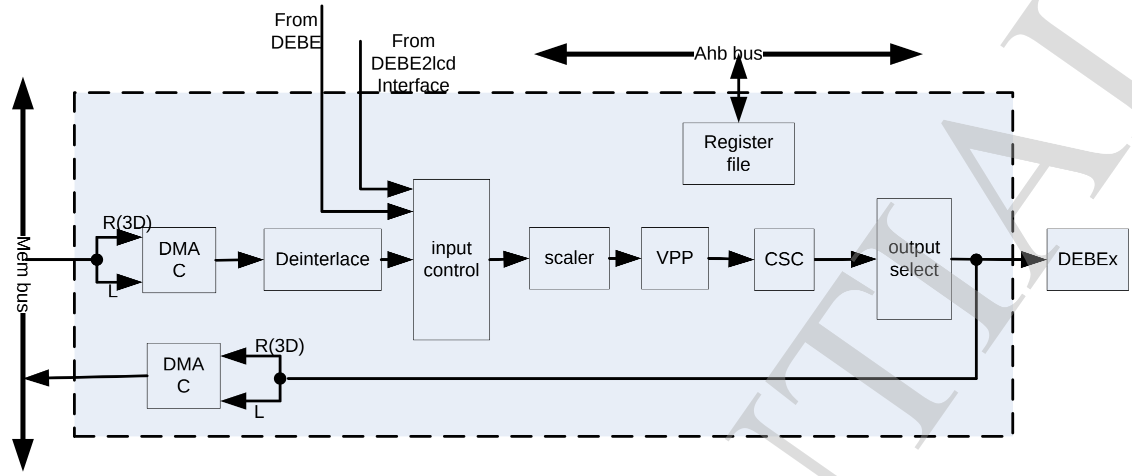
5.3.1. Overview

The DEFE performs image capture/driver, video/graphic scaling, format conversion and color space conversion. It is composed of DMA controller, input controller, deinterlacing, scaler, color space conversion, post process and output controller.

The DEFE features:

- Support interlace/progressive output scan types
- De-interlace method: weave/bob/motion-adaptive/motion-adaptive-bob
- Input format: YUV444/YUV422/YUV420/YUV411/RGB
- Direct display output format: RGB
- Write back output format: RGB/YUV444/YUV420/YUV422/YUV411
- 3-channel scaling pipelines for scaling up/down
- Programmable source image size from 8x4 to 8192x8192 resolution
- Programmable destination image size from 8x4 to 8192x8192 resolution
- 8 tap scale filter in horizontal and 4 tap in vertical direction
- 32 programmable coefficients for each tap
- Color space conversion between YUV and RGB
- Output support directly display and write back to memory
- Input support from DRAM, DEBE and interface of LCD with DEBE
- Support 3D format content input/output format convert/display(including HDMI)

5.3.2. DEFE Block Diagram



5.3.3. DEFE Register List

Module Name	Base Address
DEFE0	0x01E00000
DEFE1	0x01E20000

Register Name	Offset	Description
DEFE_EN_REG	0x0000	DEFE Module Enable Register
DEFE_FRM_CTRL_REG	0x0004	DEFE Frame Process Control Register
DEFE_BYPASS_REG	0x0008	DEFE CSC By-Pass Register
DEFE_AGTH_SEL_REG	0x000C	DEFE Algorithm Selection Register
DEFE_LINT_CTRL_REG	0x0010	DEFE Line Interrupt Control Register
DEFE_BUF_ADDR0_REG	0x0020	DEFE Input Channel 0 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0024	DEFE Input Channel 1 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0028	DEFE Input Channel 2 Buffer Address Register

Register Name	Offset	Description
DEFE_FIELD_CTRL_REG	0x002C	DEFE Field Sequence Register
DEFE_TB_OFF0_REG	0x0030	DEFE Channel 0 Tile-Based Offset Register
DEFE_TB_OFF1_REG	0x0034	DEFE Channel 1 Tile-Based Offset Register
DEFE_TB_OFF2_REG	0x0038	DEFE Channel 2 Tile-Based Offset Register
DEFE_LINESTRD0_REG	0x0040	DEFE Channel 0 Line Stride Register
DEFE_LINESTRD1_REG	0x0044	DEFE Channel 1 Line Stride Register
DEFE_LINESTRD2_REG	0x0048	DEFE Channel 2 Line Stride Register
DEFE_INPUT_FMT_REG	0x004C	DEFE Input Format Register
DEFE_WB_ADDR0_REG	0x0050	DEFE Channel 3 Write Back Address Register
DEFE_WB_ADDR1_REG	0x0054	DEFE Channel 4 Write Back Address Register
DEFE_WB_ADDR2_REG	0x0058	DEFE Channel 5 Write Back Address Register
DEFE_OUTPUT_FMT_REG	0x005C	DEFE Output Format Register
DEFE_INT_EN_REG	0x0060	DEFE Interrupt Enable Register
DEFE_INT_STATUS_REG	0x0064	DEFE Interrupt Status Register
DEFE_STATUS_REG	0x0068	DEFE Status Register
DEFE_CSC_COEF00_REG	0x0070	DEFE CSC Coefficent 00 Register
DEFE_CSC_COEF01_REG	0x0074	DEFE CSC Coefficent 01 Register
DEFE_CSC_COEF02_REG	0x0078	DEFE CSC Coefficent 02 Register
DEFE_CSC_COEF03_REG	0x007C	DEFE CSC Coefficent 03 Register
DEFE_CSC_COEF10_REG	0x0080	DEFE CSC Coefficent 10 Register
DEFE_CSC_COEF11_REG	0x0084	DEFE CSC Coefficent 11 Register
DEFE_CSC_COEF12_REG	0x0088	DEFE CSC Coefficent 12 Register
DEFE_CSC_COEF13_REG	0x008C	DEFE CSC Coefficent 13 Register
DEFE_CSC_COEF20_REG	0x0090	DEFE CSC Coefficent 20 Register
DEFE_CSC_COEF21_REG	0x0094	DEFE CSC Coefficent 21 Register
DEFE_CSC_COEF22_REG	0x0098	DEFE CSC Coefficent 22 Register
DEFE_CSC_COEF23_REG	0x009C	DEFE CSC Coefficent 23 Register
DEFE_DI_CTRL_REG	0x00A0	DEFE De-interlacing Control Register
DEFE_DI_DIAGINTP_REG	0x00A4	DEFE De-interlacing Diag-Interpolate Register
DEFE_DI_TEMPDIFF_REG	0x00A8	DEFE De-interlacing Temp-Difference Register
DEFE_DI_SAWTOOTH_REG	0x00AC	DEFE De-interlaing Sawtooth Register

Register Name	Offset	Description
DEFE_DI_SPATCOMP_REG	0x00B0	DEFE De-interlacing Spatial Compare Register
DEFE_DI_BURSTLEN_REG	0x00B4	DEFE De-interlacing DMA Burst Length Register
DEFE_DI_PRELUMA_REG	0x00B8	DEFE De-interlacing Pre-Frame Luma Address Register
DEFE_DI_TILEFLAG_REG	0x00BC	DEFE De-interlacing Tile Flag Address Register
DEFE_DI_FLAGLINESTRD_REG	0x00C0	DEFE De-interlacing Tile Flag LineStride Register
DEFE_WB_LINESTRD_EN_REG	0x00D0	DEFE Write Back Line Stride Enable Register
DEFE_WB_LINESTRD0_REG	0x00D4	DEFE Write Back Channel 3 Line Stride Register
DEFE_WB_LINESTRD1_REG	0x00D8	DEFE Write Back Channel 4 Line Stride Register
DEFE_WB_LINESTRD2_REG	0x00DC	DEFE Write Back Channel 5 Line Stride Register
DEFE_3D_CTRL_REG	0x00E0	DEFE 3D Mode Control Register
DEFE_3D_BUF_ADDR0_REG	0x00E4	DEFE 3D Channel 0 Buffer Address Register
DEFE_3D_BUF_ADDR1_REG	0x00E8	DEFE 3D Channel 1 Buffer Address Register
DEFE_3D_BUF_ADDR2_REG	0x00EC	DEFE 3D Channel 2 Buffer Address Register
DEFE_3D_TB_OFF0_REG	0x00F0	DEFE 3D Channel 0 Tile-Based Offset Register
DEFE_3D_TB_OFF1_REG	0x00F4	DEFE 3D Channel 1 Tile-Based Offset Register
DEFE_3D_TB_OFF2_REG	0x00F8	DEFE 3D Channel 2 Tile-Based Offset Register
DEFE_CH0_INSIZE_REG	0x0100	DEFE Channel 0 Input Size Register
DEFE_CH0_OUTSIZE_REG	0x0104	DEFE Channel 0 Output Size Register
DEFE_CH0_HORZFACT_REG	0x0108	DEFE Channel 0 Horizontal Factor Register
DEFE_CH0_VERTFACT_REG	0x010C	DEFE Channel 0 Vertical factor Register
DEFE_CH0_HORZPHASE_REG	0x0110	DEFE Channel 0 Horizontal Initial Phase Register
DEFE_CH0_VERTPHASE0_REG	0x0114	DEFE Channel 0 Vertical Initial Phase 0 Register

Register Name	Offset	Description
DEFE_CH0_VERTPHASE1_REG	0x0118	DEFE Channel 0 Vertical Initial Phase 1 Register
DEFE_CH0_HORZTAP0_REG	0x0120	DEFE Channel 0 Horizontal Tap Offset 0 Register
DEFE_CH0_HORZTAP1_REG	0x0124	DEFE Channel 0 Horizontal Tap Offset 1 Register
DEFE_CH0_VERTTAP_REG	0x0128	DEFE Channel 0 Vertical Tap Offset Register
DEFE_CH1_INSIZE_REG	0x0200	DEFE Channel 1 Input Size Register
DEFE_CH1_OUTSIZE_REG	0x0204	DEFE Channel 1 Output Size Register
DEFE_CH1_HORZFACT_REG	0x0208	DEFE Channel 1 Horizontal Factor Register
DEFE_CH1_VERTFACT_REG	0x020C	DEFE Channel 1 Vertical factor Register
DEFE_CH1_HORZPHASE_REG	0x0210	DEFE Channel 1 Horizontal Initial Phase Register
DEFE_CH1_VERTPHASE0_REG	0x0214	DEFE Channel 1 Vertical Initial Phase 0 Register
DEFE_CH1_VERTPHASE1_REG	0x0218	DEFE Channel 1 Vertical Initial Phase 1 Register
DEFE_CH1_HORZTAP0_REG	0x0220	DEFE Channel 1 Horizontal Tap Offset 0 Register
DEFE_CH1_HORZTAP1_REG	0x0224	DEFE Channel 1 Horizontal Tap Offset 1 Register
DEFE_CH1_VERTTAP_REG	0x0228	DEFE Channel 1 Vertical Tap Offset Register
DEFE_CH0_HORZCOEF0_REGN	0x0400+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register N=0:31
DEFE_CH0_HORZCOEF1_REGN	0x0480+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register N=0:31
DEFE_CH0_VERTCOEF_REGN	0x0500+N*4	DEFE Channel 0 Vertical Filter Coeffient Register N=0:31
DEFE_CH1_HORZCOEF0_REGN	0x0600+N*4	DEFE Channel 1 Horizontal Filter Coeffient Register N=0:31
DEFE_CH1_HORZCOEF1_REGN	0x0680+N*4	DEFE Channel 1 Horizontal Filter Coeffient Register N=0:31
DEFE_CH1_VERTCOEF_REGN	0x0700+N*4	DEFE Channel 1 Vertical Filter Coeffient Register N=0:31
DEFE_VPP_EN_REG	0x0A00	DEFE Video Post Process Enable Register
DEFE_VPP_DCTI_REG	0x0A04	DEFE Video Post Process Digital Chroma

Register Name	Offset	Description
		Transition Improve Configuration Register
DEFE_VPP_LP1_REG	0x0A08	DEFE Video Post Process Luminance Peaking Configuration 1 Register
DEFE_VPP_LP2_REG	0x0A0C	DEFE Video Post Process Luminance Peaking Configuraion 2 Register
DEFE_VPP_WLE_REG	0x0A10	DEFE Video Post Process White Level Extension Configuration Register
DEFE_VPP_BLE_REG	0x0A14	DEFE Video Post Process Black Level Extension Configuration Register

5.3.4. DEFE Register Description

5.3.4.1. DEFE_EN_REG

Offset: 0x0			Register Name: DEFE_EN_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EN DEFE enable 0: Disable 1: Enable When DEFE enable bit is disabled, the clock of DEFE module will be disabled If this bit is transition from 0 to 1, the frame process control register and the interrupt enable register will be initialed to default value, and the state machine of the module is reset

5.3.4.2. DEFE_FRM_CTRL_REG

Offset: 0x4			Register Name: DEFE_FRM_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:17	/	/	/

Offset: 0x4			Register Name: DEFE_FRM_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
16	R/W	0x0	FRM_START Frame start & reset control 0: reset 1: start If the bit is written to zero, the whole state machine and data paths of DEFE module will be reset. When the bit is written to 1, DEFE will start a new frame process.
15	/	/	/
14:12	R/W	0x0	IN_CTRL DEFE input source control 000: from dram 100: from DEBE0 interface of DEBE2lcd (don't influence the interface timing of DEBE) 101: from DEBE1 interface of DEBE2lcd(don't influence the interface timing of DEBE) 110: from DEBE0(influence the interface timing of DEBE) 111: from DEBE1(influence the interface timing of DEBE) Other: reserved
11	R/W	0x0	OUT_CTRL DEFE output control 0: enable DEFE output to DEBE 1: disable DEFE output to DEBE If DEFE write back function is enable, DEFE output to DEBE isn't recommended.
10	/	/	/
9:8	R/W	0x0	OUT_PORT_SEL DEFE output port select 00: DEBE0 01: DEBE1 other: reserved
7:3	/	/	/
2	R/W	0x0	WB_EN Write back enable

Offset: 0x4			Register Name: DEFE_FRM_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			0: Disable 1: Enable If output to DEBE is enable, the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be self-cleared when writing-back frame process starts.
1	R/W	0x0	COEF_RDY_EN Filter coefficients ready enable 0: not ready 1: filter coefficients configuration ready In order to avoid the noise, you have to ensure the same set filter coefficients are used in one frame, so the filter coefficients are buffered, the programmer can change the coefficients in any time. When the filter coefficients setting is finished, the programmer should set the bit if the programmer need the new coefficients in next scaling frame. When the new frame start, the bit will be self-cleared.
0	R/W	0x0	REG_RDY_EN Register ready enable 0: not ready 1: registers configuration ready As same as filter coefficients configuration, in order to ensure the display be correct, the correlative display configuration registers are buffered too, the programmer also can change the value of correlative registers in any time. When the registers setting is finished, the programmer should set the bit if the programmer need the new configuration in next scaling frame. When the new frame starts, the bit will also be self-cleared.

5.3.4.3. DEFE_BYPASS_REG

Offset: 0x8			Register Name: DEFE_BYPASS_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**

Offset: 0x8			Register Name: DEFE_BYPASS_REG
Bit	Read/ Write	Default/ Hex	Description
31:2	/	/	/
1	R/W	0x0	CSC_BYPASS_EN CSC by-pass enable 0: CSC enable 1: CSC will be by-passed Actually, in order ensure the module working be correct, This bit only can be set when input data format is the same as output data format (both YUV or both RGB)
0	/	/	/

5.3.4.4. DEFE_AGTH_SEL_REG

Offset: 0xC			Register Name: DEFE_AGTH_SEL_REG
Bit	Read/ Write	Default/ Hex	Description
31:9	/	/	/
8	R/W	0x0	LINEBUF_AGTH DEFE line buffer algorithm select 0: horizontal filtered result 1: original data
7:0	/	/	/

5.3.4.5. DEFE_LINT_CTRL_REG

Offset: 0x10			Register Name: DEFE_LINT_CTRL_REG
Bit	Read/ Write	Default/He x	Description
31:28	/	/	/
27:16	R	0x0	CURRENT_LINE
15	R/W	0x0	FIELD_SEL

Offset: 0x10			Register Name: DEFE_LINT_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
			Field select 0: each field 1: end field(field counter in reg0x2c)
14:13	/	/	/
12:0	R/W	0x0	TRIG_LINE Trigger line number of line interrupt

5.3.4.6. DEFE_BUF_ADDR0_REG

Offset: 0x20			Register Name: DEFE_BUF_ADDR0_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

5.3.4.7. DEFE_BUF_ADDR1_REG

Offset: 0x24			Register Name: DEFE_BUF_ADDR1_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used

Offset: 0x24			Register Name: DEFE_BUF_ADDR1_REG
Bit	Read/ Write	Default/Hex	Description
			to generating output frame. In non-tile-based type: The address is the start address of the first line.

5.3.4.8. DEFE_BUF_ADDR2_REG

Offset: 0x28			Register Name: DEFE_BUF_ADDR2_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non- tile-based type: The address is the start address of the first line.

5.3.4.9. DEFE_FIELD_CTRL_REG

Offset: 0x2C			Register Name: DEFE_FIELD_CTRL_REG
Bit	Read/ Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	FIELD_LOOP_MOD Field loop mode 0:the last field; 1:the full frame
11	/	/	/
10:8	R/W	0x0	VALID_FIELD_CNT Valid field counter bit the valid value = this value + 1；

Offset: 0x2C			Register Name: DEFE_FIELD_CTRL_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
7:0	R/W	0x0	FIELD_CNT Field counter each bit specify a field to display, 0:top field,1:bottom field

5.3.4.10. DEFE_TB_OFF0_REG

Offset: 0x30			Register Name: DEFE_TB_OFF0_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

5.3.4.11. DEFE_TB_OFF1_REG

Offset: 0x34			Register Name: DEFE_TB_OFF1_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile

Offset: 0x34			Register Name: DEFE_TB_OFF1_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

5.3.4.12. DEFE_TB_OFF2_REG

Offset: 0x38			Register Name: DEFE_TB_OFF2_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

5.3.4.13. DEFE_LINESTRD0_REG

Offset: 0x40	Register Name: DEFE_LINESTRD0_REG

Bit	Read/ Write	Default/ Hex	Description
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the start of the next line.

5.3.4.14. DEFE_LINESTRD1_REG

Offset: 0x44			Register Name: DEFE_LINESTRD1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the start of the next line.

5.3.4.15. DEFE_LINESTRD2_REG

Offset: 0x48			Register Name: DEFE_LINESTRD2_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction)

Offset: 0x48			Register Name: DEFE_LINESTRD2_REG
Bit	Read/ Write	Default/Hex	Description
			In non-tile-based type The stride length is the distance from the start of one line to the start of the next line.

5.3.4.16. DEFE_INPUT_FMT_REG

Offset: 0x4C			Register Name: DEFE_INPUT_FMT_REG
Bit	Read/ Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	BYTE_SEQ Input data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word)
15:13	/	/	/
12	R/W	0x0	SCAN_MOD Scanning Mode selection 0: non-interlace 1: interlace
11	/	/	/
10:8	R/W	0x0	DATA_MOD Input data mode selection 000: non-tile-based planar data 001: interleaved data 010: non-tile-based UV combined data 100: tile-based planar data 110: tile-based UV combined data other: reserved
7	/	/	/

Offset: 0x4C			Register Name: DEFE_INPUT_FMT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
6:4	R/W	0x0	DATA_FMT Input component data format **In non-tile-based planar data mode:** 000: YUV 4:4:4 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 100: CSI RGB data 101: RGB888 Other: Reserved **In interleaved data mode:** 000: YUV 4:4:4 001: YUV 4:2:2 101: ARGB8888 Other: reserved **In non-tile-based UV combined data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved **In tile-based planar data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: Reserved **In tile-based UV combined data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved
3:2	/	/	/
1:0	R/W	0x0	DATA_PS

Offset: 0x4C			Register Name: DEFE_INPUT_FMT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			Pixel sequence **In interleaved YUV422 data mode:** 00: Y1V0Y0U0 01: V0Y1U0Y0 10: Y1U0Y0V0 11: U0Y1V0Y0 **In interleaved YUV444 data mode:** 00: VUYA 01: AYUV Other: reserved **In UV combined data mode: (UV component)** 00: V1U1V0U0 01: U1V1U0V0 Other: reserved **In interleaved ARGB8888 data mode:** 00: BGRA 01: ARGB Other: reserved

5.3.4.17. DEFE_WB_ADDR0_REG

Offset: 0x50			Register Name: DEFE_WB_ADDR0_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	WB_ADDR Write-back address setting for scaled data.

5.3.4.18. DEFE_WB_ADDR1_REG

Offset: 0x54			Register Name: DEFE_WB_ADDR1_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	WB_ADDR Write-back address setting for scaled data.

5.3.4.19. DEFE_WB_ADDR2_REG

Offset: 0x58			Register Name: DEFE_WB_ADDR2_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	WB_ADDR Write-back address setting for scaled data.

5.3.4.20. DEFE_OUTPUT_FMT_REG

Offset: 0x5C			Register Name: DEFE_OUTPUT_FMT_REG
Bit	Read/ Write	Default/ Hex	Description
31:9	/	/	/
8	R/W	0x0	BYTE_SEQ Output data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word) For ARGB, when this bit is 0, the byte sequence is BGRA, and when this bit is 1, the byte sequence is ARGB;
7:5	/	/	/
4	R/W	0x0	SCAN_MOD Output interlace enable 0: disable 1: enable

Offset: 0x5C			Register Name: DEFE_OUTPUT_FMT_REG
Bit	Read/ Write	Default/ Hex	Description
			When output interlace enable, scaler selects YUV initial phase according to LCD field signal
3	/	/	/
2:0	R/W	0x0	DATA_FMT Data format 000: planar RGB888 conversion data format 001: interleaved BGRA8888 conversion data format(A component always be pad 0xff) 010: interleaved ARGB8888 conversion data format(A component always be pad 0xff) 100: planar YUV 444 101: planar YUV 420(only support YUV input and not interleaved mode) 110: planar YUV 422(only support YUV input) 111: planar YUV 411(only support YUV input) Other: reserved

5.3.4.21. DEFE_INT_EN_REG

Offset: 0x60			Register Name: DEFE_INT_EN_REG
Bit	Read/ Write	Default/H ex	Description
31:11	/	/	/
10	R/W	0x0	REG_LOAD_EN Register ready load interrupt enable
9	R/W	0x0	LINE_EN Line interrupt enable
8	/	/	/
7	R/W	0x0	WB_EN Write-back end interrupt enable 0: Disable 1: Enable
6:0	/	/	/

5.3.4.22. DEFE_INT_STATUS_REG

Offset: 0x64			Register Name: DEFE_INT_STATUS_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	REG_LOAD_STATUS Register ready load interrupt status
9	R/W	0x0	LINE_STATUS Line interrupt status
8	/	/	/
7	R/W	0x0	WB_STATUS Write-back end interrupt status
6:0	/	/	/

5.3.4.23. DEFE_STATUS_REG

Offset: 0x68			Register Name: DEFE_STATUS_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	/	/	/
28:16	R	0x0	LINE_ON_SYNC Line number(when sync reached)
15	R/W	0x0	WB_ERR_SYNC Sync reach flag when capture in process
14	R/W	0x0	WB_ERR_LOSEDATA Lose data flag when capture in process
13	/	/	/
12	R	0x0	WB_ERR_STATUS write-back error status 0: valid write back 1: un-valid write back This bit is cleared through write 0 to reset/start bit in frame control

Offset: 0x68			Register Name: DEFE_STATUS_REG
Bit	Read/ Write	Default/ Hex	Description
			register
11:6	/	/	/
5	R	0x0	LCD_FIELD LCD field status 0: top field 1: bottom field
4	R	0x0	DRAM_STATUS Access dram status 0: idle 1: busy This flag indicates whether scaler is accessing dram
3	/	/	/
2	R	0x0	CFG_PENDING Register configuration pending 0: no pending 1: configuration pending This bit indicates the registers for the next frame has been configured. This bit will be set when configuration ready bit is set and this bit will be cleared when a new frame process begin.
1	R	0x0	WB_STATUS Write-back process status 0: write-back end or write-back disable 1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
0	R	0x0	FRM_BUSY Frame busy. This flag indicates that the frame is being processed. The bit will be set when frame process reset & start is set, and be cleared when frame process reset or disabled.

5.3.4.24. DEFE_CSC_COEF00_REG

Offset: 0x70			Register Name: DEFE_CSC_COEF00_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

5.3.4.25. DEFE_CSC_COEF01_REG

Offset: 0x74			Register Name: DEFE_CSC_COEF01_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

5.3.4.26. DEFE_CSC_COEF02_REG

Offset: 0x78			Register Name: DEFE_CSC_COEF02_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

5.3.4.27. DEFE_CSC_COEF03_REG

Offset: 0x7C	Register Name: DEFE_CSC_COEF03_REG

Bit	Read/ Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	CONT the Y/G constant the value equals to coefficient*2^4

5.3.4.28. DEFE_CSC_COEF10_REG

Offset: 0x80			Register Name: DEFE_CSC_COEF10_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

5.3.4.29. DEFE_CSC_COEF11_REG

Offset: 0x84			Register Name: DEFE_CSC_COEF11_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

5.3.4.30. DEFE_CSC_COEF12_REG

Offset: 0x88			Register Name: DEFE_CSC_COEF12_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/

Offset: 0x88			Register Name: DEFE_CSC_COEF12_REG
Bit	Read/ Write	Default/ Hex	Description
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

5.3.4.31. DEFE_CSC_COEF13_REG

Offset: 0x8C			Register Name: DEFE_CSC_COEF13_REG
Bit	Read/ Write	Default/ Hex	Description
31:14	/	/	/
13:00	R/W	0x0	CONT the U/R constant the value equals to coefficient*2^4

5.3.4.32. DEFE_CSC_COEF20_REG

Offset: 0x90			Register Name: DEFE_CSC_COEF20_REG
Bit	Read/ Write	Default /Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

5.3.4.33. DEFE_CSC_COEF21_REG

Offset: 0x94			Register Name: DEFE_CSC_COEF21_REG
Bit	Read/ Write	Default/ Hex	Description
31:13	/	/	/

Offset: 0x94			Register Name: DEFE_CSC_COEF21_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

5.3.4.34. DEFE_CSC_COEF22_REG

Offset: 0x98			Register Name: DEFE_CSC_COEF22_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

5.3.4.35. DEFE_CSC_COEF23_REG

Offset: 0x9C			Register Name: DEFE_CSC_COEF23_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:14	/	/	/
13:00	R/W	0x0	CONT the V/B constant the value equals to coefficient*2^4

5.3.4.36. DEFE_DI_CTRL_REG

Offset: 0xA0			Register Name: DEFE_DI_CTRL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:26	/	/	/

Offset: 0xA0			Register Name: DEFE_DI_CTRL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
25	R/W	0x0	TEMPDIFF_EN Temporal difference compare enable 0: disable 1: enable
24	R/W	0x0	DIAGINTP_EN De-interlacing diagonal interpolate enable 0: disable 1: enable
23:18	/	/	/
17:16	R/W	0x0	MOD De-interlacing mode select 00: weave 01: bob 10: motion-adaptive 11: motion-adaptive-bob
15:1	/	/	/
0	R/W	0x0	EN De-interlacing enable 0: de-interlacing disable 1: de-interlacing enable

5.3.4.37. DEFE_DI_DIAGINTP_REG

Offset: 0xA4			Register Name: DEFE_DI_DIAGINTP_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	R/W	0x8	TH3 Diagintp_th3
23:16	R/W	0x10	TH2 Diagintp_th2
15	/	/	/
14:8	R/W	0x5	TH1

Offset: 0xA4			Register Name: DEFE_DI_DIAGINTP_REG
Bit	Read/ Write	Default/ Hex	Description
			Diagintp_th1
7	/	/	/
6:0	R/W	0x4F	TH0 Diagintp_th0

5.3.4.38. DEFE_DI_TEMPDIFF_REG

Offset: 0xA8			Register Name: DEFE_DI_TEMPDIFF_REG
Bit	Read/ Write	Default/H ex	Description
31:13	/	/	/
12:8	R/W	0xF	TH Temporal_th
7:0	/	/	/

5.3.4.39. DEFE_DI_SAWTOOTH_REG

Offset: 0xAC			Register Name: DEFE_DI_SAWTOOTH_REG
Bit	Read/ Write	Default/ Hex	Description
31:16	/	/	/
15:8	R/W	0x8	TH2 sawtooth_th2
7:0	R/W	0x14	TH1 Sawtooth_th1

5.3.4.40. DEFE_DI_SPATCOMP_REG

Offset: 0xB0	Register Name: DEFE_DI_SPATCOMP_REG

Bit	Read/ Write	Default/ Hex	Description
31:25	/	/	/
24:16	R/W	0xA	TH1 spatial_th1
15:9	/	/	/
8:0	R/W	0x64	TH0 spatial_th0

5.3.4.41. DEFE_DI_BURSTLEN_REG

Offset: 0xB4			Register Name: DEFE_DI_BURSTLEN_REG
Bit	Read/ Write	Default/ Hex	Description
31:14	/	/	/
13:8	R/W	0x1F	CHROMA Chroma burst length
7:6	/	/	/
5:0	R/W	0x1F	LUMA Luma burst length

5.3.4.42. DEFE_DI_PRELUMA_REG

Offset: 0xB8			Register Name: DEFE_DI_PRELUMA_REG
Bit	Read/ Write	Default/ Hex	Description
31:0	R/W	0x0	PREFRM_ADDR Pre-frame buffer address of luma

5.3.4.43. DEFE_DI_TILEFLAG_REG

Offset: 0xBC	Register Name: DEFE_DI_TILEFLAG_REG

Bit	Read/ Write	Default/ Hex	Description
31:0	R/W	0x0	TILE_FLAG_ADDR Current frame tile flag buffer address

5.3.4.44. DEFE_DI_FLAGLINESTRD_REG

Offset: 0xC0			Register Name: DEFE_DI_FLAGLINESTRD_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x40	TILE_FLAG_LINESTRD tile flag line-stride

5.3.4.45. DEFE_WB_LINESTRD_EN_REG

Offset: 0xD0			Register Name: DEFE_WB_LINESTRD_EN_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EN Write back line-stride enable 0: disable 1: enable

5.3.4.46. DEFE_WB_LINESTRD0_REG

Offset: 0xD4			Register Name: DEFE_WB_LINESTRD0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x0	LINE_STRD Ch3 write back line-stride

5.3.4.47. DEFE_WB_LINESTRD1_REG

Offset: 0xD8			Register Name: DEFE_WB_LINESTRD1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x0	LINE_STRD Ch4 write back line-stride

5.3.4.48. DEFE_WB_LINESTRD2_REG

Offset: 0xDC			Register Name: DEFE_WB_LINESTRD2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x0	LINE_STRD Ch5 write back line-stride

5.3.4.49. DEFE_3D_CTRL_REG

Offset: 0xE0			Register Name: DEFE_3D_CTRL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	TB_OUT_MOD_FIELD Top/bottom output mode field number 0: left or left 1st field(determined by reg0x2c) 1: right or right 1st field 2: left 2nd field 3: right 2nd field
23:19	/	/	/
18:16	R/W	0x0	CI_OUT_MOD 3D column interleaved mode 0: CI_1 1: CI_2 2: CI_3 3: CI_4

Offset: 0xE0			Register Name: DEFE_3D_CTRL_REG
Bit	Read/ Write	Default/ Hex	Description
			Other: reserved
15:13	/	/	/
12	R/W	0x0	TB_OUT_SCAN_MOD Output top/bottom scan mode selection 0: progressive 1: interlace
11	R/W	0x0	LI_IN_EN 3D input line interleaved enable
10	R/W	0x0	SS_OUT_EN 3D output side by side mode enable
9	/	/	/
8	R/W	0x0	CI_OUT_EN 3D Column interleaved mode output enable
7:2	/	/	/
1:0	R/W	0x0	MOD_SEL 3D mode select 00: normal output mode(2D mode) 01: 3D side by side/line interleaved/column interleaved output mode 10: 3D top/bottom output mode 11: reserved When 3D mode is enable, DEFE will enter 3D mode(source will be composed of left and right frame, output will be composed of left and right frame).

5.3.4.50. DEFE_3D_BUF_ADDR0_REG

Offset: 0xE4			Register Name: DEFE_3D_BUF_ADDR0_REG
Bit	Read/ Write	Default/ Hex	Description
31:0	R/W	0x0	RIGHT_CH0_ADDR 3D mode channel 0 buffer address This address is the start address of right image in 3D mode

5.3.4.51. DEFE_3D_BUF_ADDR1_REG

Offset: 0xE8			Register Name: DEFE_3D_BUF_ADDR1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x0	RIGHT_CH1_ADDR 3D mode channel 1 buffer address This address is the start address of right image in 3D mode

5.3.4.52. DEFE_3D_BUF_ADDR2_REG

Offset: 0xEC			Register Name: DEFE_3D_BUF_ADDR2_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:0	R/W	0x0	RIGHT_CH2_ADDR 3D mode channel 2 buffer address This address is the start address of right image in 3D mode

5.3.4.53. DEFE_3D_TB_OFF0_REG

Offset: 0xF0			Register Name: DEFE_3D_ TB_OFF0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the first tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

Offset: 0xF0			Register Name: DEFE_3D_ TB_OFF0_REG
Bit	Read/ Write	Default/ Hex	Description
			This value is the start offset of right image in 3D mode

5.3.4.54. DEFE_3D_TB_OFF1_REG

Offset: 0xF4			Register Name: DEFE_3D_ TB_OFF1_REG
Bit	Read/ Write	Default/ Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the first tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile This value is the start offset of right image in 3D mode

5.3.4.55. DEFE_3D_TB_OFF2_REG

Offset: 0xF8			Register Name: DEFE_3D_ TB_OFF2_REG
Bit	Read/ Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the first tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/

Offset: 0xF8			Register Name: DEFE_3D_ TB_OFF2_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile This value is the start offset of right image in 3D mode

5.3.4.56. DEFE_CH0_INSIZE_REG

Offset: 0x100			Register Name: DEFE_CH0_INSIZE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image Y/G component height Input image height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image Y/G component width The image width = The value of these bits add 1 When line buffer result selection is original data, the maximum width is 2048.

5.3.4.57. DEFE_CH0_OUTSIZE_REG

Offset: 0x104			Register Name: DEFE_CH0_OUTSIZE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer Y/G component height The output layer height = The value of these bits add 1

Offset: 0x104			Register Name: DEFE_CH0_OUTSIZE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output layer Y/G component width The output layer width = The value of these bits add 1 When line buffer result selection is horizontal filtered result, the maximum width is 2048

5.3.4.58. DEFE_CH0_HORZFACT_REG

Offset: 0x108			Register Name: DEFE_CH0_HORZFACT_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

5.3.4.59. DEFE_CH0_VERTFACT_REG

Offset: 0x10C			Register Name: DEFE_CH0_VERTFACT_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT

Offset: 0x10C			Register Name: DEFE_CH0_VERTFACT_REG
Bit	Read/ Write	Default/ Hex	Description
			The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

5.3.4.60. DEFE_CH0_HORZPHASE_REG

Offset: 0x110			Register Name: DEFE_CH0_HORZPHASE_REG
Bit	Read/ Write	Default/ Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

5.3.4.61. DEFE_CH0_VERTPHASE0_REG

Offset: 0x114			Register Name: DEFE_CH0_VERTPHASE0_REG
Bit	Read/ Write	Default/ Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in vertical for top field (complement) This value equals to initial phase * 2^{16}

5.3.4.62. DEFE_CH0_VERTPHASE1_REG

Offset: 0x118			Register Name: DEFE_CH0_VERTPHASE1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in vertical for bottom field (complement) This value equals to initial phase * 2^{16}

5.3.4.63. DEFE_CH0_HORZTAP0_REG

Offset: 0x120			Register Name: DEFE_CH0_HORZTAP0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in horizontal
7	/	/	/
6:0	R/W	0x7D	TAP0 Tap 0 offset in horizontal

5.3.4.64. DEFE_CH0_HORZTAP1_REG

Offset: 0x124			Register Name: DEFE_CH0_HORZTAP1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**

Offset: 0x124			Register Name: DEFE_CH0_HORZTAP1_REG
Bit	Read/ Write	Default/ Hex	Description
31	/	/	/
30:24	R/W	0x1	TAP7 Tap 7 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP6 Tap 6 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP5 Tap 5 offset in horizontal
7	/	/	/
6:0	R/W	0x1	TAP4 Tap 4 offset in horizontal

5.3.4.65. DEFE_CH0_VERTTAP_REG

Offset: 0x128			Register Name: DEFE_CH0_VERTTAP_REG
Bit	Read/ Write	Default/ Hex	Description
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in vertical
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in vertical
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in vertical
7	/	/	/
6:0	R/W	0x7F	TAP0 Tap 0 offset in vertical

5.3.4.66. DEFE_CH1_INSIZE_REG

Offset: 0x200			Register Name: DEFE_CH1_INSIZE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image U/R component height Input image height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image U/R component width The image width = The value of these bits add 1 When line buffer result selection is original data, the maximum width is 2048

5.3.4.67. DEFE_CH1_OUTSIZE_REG

Offset: 0x204			Register Name: DEFE_CH1_OUTSIZE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer U/R component height The output layer height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output layer U/R component width The output layer width = The value of these bits add 1 When line buffer result selection is horizontal filtered result, the maximum width is 2048

5.3.4.68. DEFE_CH1_HORZFACT_REG

Offset: 0x208			Register Name: DEFE_CH1_HORZFACT_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

5.3.4.69. DEFE_CH1_VERTFACT_REG

Offset: 0x20C			Register Name: DEFE_CH1_VERTFACT_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

5.3.4.70. DEFE_CH1_HORZPHASE_REG

Offset: 0x210			Register Name: DEFE_CH1_HORZPHASE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

5.3.4.71. DEFE_CH1_VERTPHASE0_REG

Offset: 0x214			Register Name: DEFE_CH1_VERTPHASE0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in vertical for top field (complement) This value equals to initial phase * 2^{16}

5.3.4.72. DEFE_CH1_VERTPHASE1_REG

Offset: 0x218			Register Name: DEFE_CH1_VERTPHASE1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in vertical for bottom field (complement) This value equals to initial phase * 2^{16}

5.3.4.73. DEFE_CH1_HORZTAP0_REG

Offset: 0x220			Register Name: DEFE_CH1_HORZTAP0_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in horizontal
7	/	/	/
6:0	R/W	0x7D	TAP0 Tap 0 offset in horizontal

5.3.4.74. DEFE_CH1_HORZTAP1_REG

Offset: 0x224			Register Name: DEFE_CH1_HORZTAP1_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP7 Tap 7 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP6 Tap 6 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP5 Tap 5 offset in horizontal
7	/	/	/
6:0	R/W	0x1	TAP4

Offset: 0x224			Register Name: DEFE_CH1_HORZTAP1_REG
Bit	Read/ Write	Default/ Hex	Description
			Tap 4 offset in horizontal

5.3.4.75. DEFE_CH1_VERTTAP_REG

Offset: 0x228			Register Name: DEFE_CH1_VERTTAP_REG
Bit	Read/ Write	Default/ Hex	Description
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in vertical
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in vertical
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in vertical
7	/	/	/
6:0	R/W	0x7F	TAP0 Tap 0 offset in vertical

5.3.4.76. DEFE_CH0_HORZCOEF0_REGN (N=0 :31)

Offset: 0x400+N*4			Register Name: DEFE_CH0_HORZCOEF0_REGN
Bit	Read/ Write	Default/Hex	Description
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient

Offset: 0x400+N*4			Register Name: DEFE_CH0_HORZCOEF0_REGN
Bit	Read/ Write	Default/Hex	Description
			The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

5.3.4.77. DEFE_CH0_HORZCOEF1_REGN (N=0 :31)

Offset: 0x480+N*4			Register Name: DEFE_CH0_HORZCOEF1_REGN
Bit	Read/ Write	Default/ Hex	Description
31:24	R/W	0x0	TAP7 Horizontal tap7 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP6 Horizontal tap6 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP5 Horizontal tap5 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP4 Horizontal tap4 coefficient The value equals to coefficient*2^6

5.3.4.78. DEFE_CH0_VERTCOEF_REGN (N=0 :31)

Offset: 0x500+N*4			Register Name: DEFE_CH0_VERTCOEF_REGN
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

5.3.4.79. DEFE_CH1_HORZCOEF0_REGN (N=0 :31)

Offset: 0x600+N*4			Register Name: DEFE_CH1_HORZCOEF0_REGN
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

5.3.4.80. DEFE_CH1_HORZCOEF1_REGN (N=0 :31)

Offset: 0x680+N*4			Register Name: DEFE_CH1_HORZCOEF1_REGN
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	R/W	0x0	TAP7 Horizontal tap7 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP6 Horizontal tap6 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP5 Horizontal tap5 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP4 Horizontal tap4 coefficient The value equals to coefficient*2^6

5.3.4.81. DEFE_CH1_VERTCOEF_REGN (N=0 :31)

Offset: 0x700+N*4			Register Name: DEFE_CH1_VERTCOEF_REGN
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient

Offset: 0x700+N*4			Register Name: DEFE_CH1_VERTCOEF_REGN
Bit	Read/ Write	Default/ Hex	Description
			The value equals to coefficient*2^6

5.3.4.82. DEFE_VPP_EN_REG

Offset: 0xA00			Register Name: DEFE_VPP_EN_REG
Bit	Read/ Write	Default/ Hex	Description
31:1	/	/	/
0	R/W	0x0	EN VPP enable 0: Disable 1: Enable

5.3.4.83. DEFE_VPP_DCTI_REG

Offset: 0xA04			Register Name: DEFE_VPP_DCTI_REG
Bit	Read/ Write	Default/Hex	Description
31	R/W	0x0	UV_SEPARATE_EN UV separate enable 0: U/V will be under direction detection control 1: U/V wont be under direction detection control
30	/	/	/
29	R/W	0x0	UV_SAME_SIGN_MAX/MIN_MODE_SEL UV direction detection using max or min of |U|/|V| in same sign condition when related separate mode select “Using Max/Min mode” and U/V path shift are in the same sign, path shift use 0: min(|U|,|V|) 1: max(|U|,|V|)
28	R/W	0x0	UV_DIFF_SIGN_ MAX/MIN_MODE_SEL UV direction detection using max or min of |U|/|V| in different sign

Offset: 0xA04			Register Name: DEFE_VPP_DCTI_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
			condition when related separate mode select “Using Max/Min mode” and U/V path shift are in the different sign, path shift use 0: min(|U|,|V|) 1: max(|U|,|V|)
27:26	R/W	0x0	UV_SAME_SIGN_MODE_SEL UV separate mode in same sign condition 00: Using U always 01: Using V always 10: Using 0 always 11: Using Max/Min mode
25:24	R/W	0x0	UV_DIFF_SIGN_MODE_SEL UV separate mode in different sign condition 00: Using U always 01: Using V always 10: Using 0 always 11: Using Max/Min mode
23:22	/	/	/
21:16	R/W	0x0	DCTI_GAIN
15:12	R/W	0x0	DCTI_PATH_LIMIT Max path limit equal to 12
11:10	R/W	0x0	DCTI_FILTER2_SEL DCTI 2nd filter algorithm selection 00: algorithm0 01: algorithm1 10: algorithm2 11: reserved
9:8	R/W	0x0	DCTI_FILTER1_SEL DCTI 1st filter algorithm selection 00: algorithm0 01: algorithm1 10: algorithm2 11: reserved
7	R/W	0x0	DCTI_SUPHILL_EN

Offset: 0xA04			Register Name: DEFE_VPP_DCTI_REG
Bit	Read/ Write	Default/Hex	Description
			DCTI super hill protection enable 0: Disable 1: Enable
6	R/W	0x0	DCTI_HILL_EN DCTI hill protection enable 0: Disable 1: Enable
5:1	/	/	/
0:	R/W	0x0	DCTI_EN 0: Disable 1: Enable

5.3.4.84. DEFE_VPP_LP1_REG

Offset: 0xA08			Register Name: DEFE_VPP_LP1_REG
Bit	Read/ Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	BETA LP high-pass filter gain(BETA)
23:21	/	/	/
20:16	R/W	0x0	ALPHA LP band-pass filter2 gain(ALPHA)
15:13	/	/	/
12:8	R/W	0x0	TAU LP band-pass filter1 gain(TAU)
7:1	/	/	/
0	R/W	0x0	LP_EN 0: Disable 1: Enable

5.3.4.85. DEFE_VPP_LP2_REG

Offset: 0xA0C			Register Name: DEFE_VPP_LP2_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	LIMIT_THR LP limit threshold
23:22	R/W	0x0	DELTA LP LUT selection for overshoot(DELTA) 00: DELTA0 01: DELTA025 10: DELTA05 11: DELTA1
21:18	/	/	/
17:16	R/W	0x0	NEGGAIN LP LUT selection for undershot(NEGGAIN) 00: NEGGAIN0 01: NEGGAIN025 10: NEGGAIN05 11: NEGGAIN1
15:8	R/W	0x0	CORTHR LP coring threshold(CORTHR)
7:5	/	/	/
4:0	R/W	0x0	LPF_GAIN LP low-pass-filter gain

5.3.4.86. DEFE_VPP_WLE_REG

Offset: 0xA10			Register Name: DEFE_VPP_WLE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	WLE_GAIN WLE gain
15:8	R/W	0x0	WLE_THR WLE threshold

Offset: 0xA10			Register Name: DEFE_VPP_WLE_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
			Note: MUST BE set 128~255.
7:1	/	/	/
0	R/W	0x0	WLE_EN WLE enable

5.3.4.87. DEFE_VPP_BLE_REG

Offset: 0xA14			Register Name: DEFE_VPP_BLE_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	BLE_GAIN BLE gain
15:8	R/W	0x0	BLE_THR BLE threshold Note: MUST BE set 0~127.
7:1	/	/	/
0	R/W	0x0	BLE_EN BLE enable

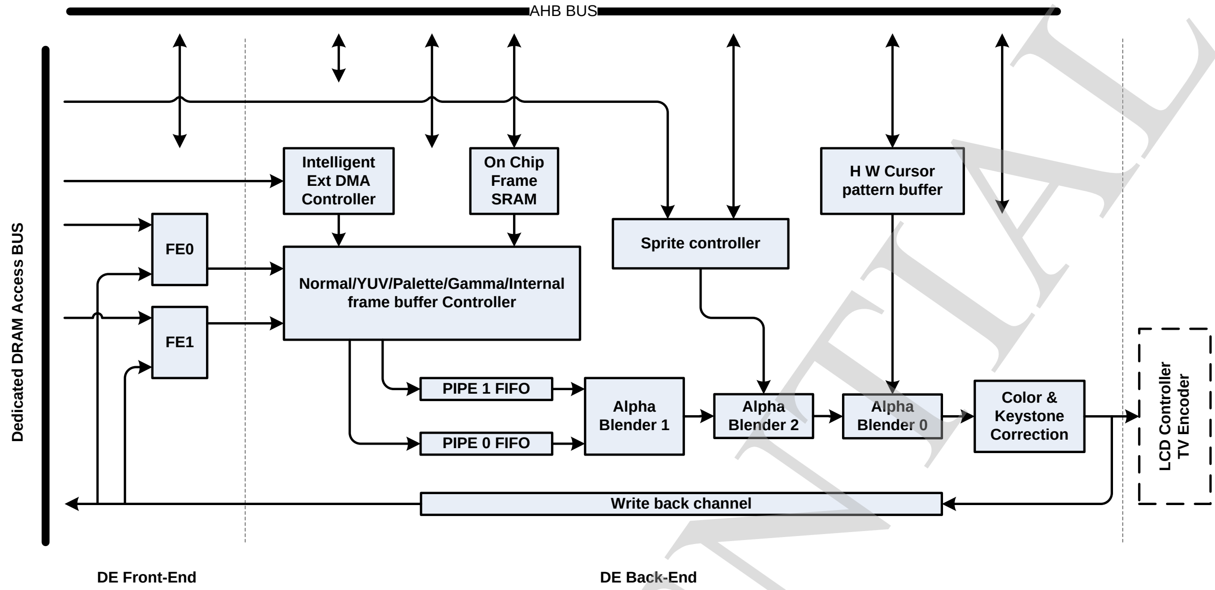
5.4. Display Engine Backend

5.4.1. Overview

The display engine backend features:

- 4 moveable and size-adjustable layers
- Layer size up to 8192x8192 pixels
- Alpha blending support
- Color key support
- Write back function support
- 1/2/4/8 bpp mono / palette support
- 16/24/32 bpp color support (external frame buffer)
    - 5/6/5
    - 1/5/5/5
    - 0/8/8/8
    - 8/8/8
    - 8/8/8/8
    - 4/4/4/4
- On chip SRAM support
    - 256 entry 32-bpp palette
    - 1/2/4/8 bpp internal frame buffer
    - Gamma correction support
- Hardware cursor support
    - 32x32 @8bpp
    - 64x64 @2bpp
    - 64x32 @4bpp
    - 32x64 @4bpp
- Sprite function support
    - 32bpp true color or 8bpp palette mode
    - up to 32 independent sprite blocks
    - each block can be set arbitrary coordinate
    - adjustable block size
- YUV input channel support
- Vertical keystone correction
- Output color correction

5.4.2. Display Engine Block Diagram



5.4.3. DEBE Register list

Module name	Base Address
BE0	0x01e60000
BE1	0x01e40000

Register name	Offset	Description
DEBE_MODCTL_REG	0x800	DE back-end mode control register
DEBE_BACKCOLOR_REG	0x804	DE-back color control register
DEBE_DISSIZE_REG	0x808	DE-back display size setting register
DEBE_LAYSIZE_REG	0x810 – 0x81C	DE-layer size register
DEBE_LAYCOOR_REG	0x820 – 0x82C	DE-layer coordinate control register
DEBE_LAYLINEWIDTH_REG	0x840 – 0x84C	DE-layer frame buffer line width register
DEBE_LAYFB_L32ADD_REG	0x850 – 0x85C	DE-layer frame buffer low 32 bit address register

Register name	Offset	Description
DEBE_LAYFB_H4ADD_REG	0x860	DE-layer frame buffer high 4 bit address register
DEBE_REGBUFFCTL_REG	0x870	DE-Register buffer control register
DEBE_CKMAX_REG	0x880	DE-color key MAX register
DEBE_CKMIN_REG	0x884	DE-color key MIN register
DEBE_CKCFG_REG	0x888	DE-color key configuration register
DEBE_ATTCTL_REG0	0x890 – 0x89C	DE-layer attribute control register0
DEBE_ATTCTL_REG1	0x8A0 – 0x8AC	DE-layer attribute control register1
DEBE_HWCCTL_REG	0x8D8	DE-HWC coordinate control register
DEBE_HWCFBCTL_REG	0x8E0	DE-HWC frame buffer format register
DEBE_WBCTL_REG	0x8F0	DE backend write back control register
DEBE_WBADD_REG	0x8F4	DE backend write back address register
DEBE_WBLINEWIDTH_REG	0x8F8	DE backend write back buffer line width register
DEBE_SPREN_REG	0x900	DE-sprite enable register
DEBE_SPRFMTCTL_REG	0x908	DE-sprite format control register
DEBE_SPRALPHACTL_REG	0x90C	DE-sprite alpha control register
DEBE_IYUVCTL_REG	0x920	DE backend input YUV channel control register
DEBE_IYUVADD_REG	0x930 – 0x938	DE backend YUV channel frame buffer address register
DEBE_IYUVLINEWIDTH_REG	0x940 – 0x948	DE backend YUV channel buffer line width register
DEBE_YGCOEF_REG	0x950 – 0x958	DE backend Y/G coefficient register
DEBE_YGCONS_REG	0x95C	DE backend Y/G constant register
DEBE_URCOEF_REG	0x960 – 0x968	DE backend U/R coefficient register
DEBE_URCONS_REG	0x96C	DE backend U/R constant register
DEBE_VBCOEF_REG	0x970 – 0x978	DE backend V/B coefficient register
DEBE_VBCONS_REG	0x97C	DE backend V/B constant register
DEBE_KSCTL_REG	0x980	DE backend keystone correction control register
DEBE_KSBKCOLOR_REG	0x984	DE backend keystone back color control register
DEBE_KSFSTLINEWIDTH_REG	0x988	DE backend keystone output first line width setting register

Register name	Offset	Description
DEBE_KSVSCAFCT_REG	0x98C	DE backend keystone vertical scaling factor register
DEBE_KSHSCACOEF_RAM	0x9A0 – 0x9BC	DE backend keystone horizontal filtering coefficient RAM block
DEBE_OCCTL_REG	0x9C0	DE backend output color control register
DEBE_OCRCOEF_REG	0x9D0-0x9D8	DE backend output color R coefficient register
DEBE_OCRCONS_REG	0x9DC	DE backend output color R constant register
DEBE_OCGCOEF_REG	0x9E0-0x9E8	DE backend output color G coefficient register
DEBE_OCGCONS_REG	0x9EC	DE backend output color G constant register
DEBE_OCBCOEF_REG	0x9F0-0x9F8	DE backend output color B coefficient register
DEBE_OCBCONS_REG	0x9FC	DE backend output color B constant register
DEBE_SPRCOORCTL_REG	0xA00-0xAFC	DE-sprite single block coordinate control register
DEBE_SPRATTCTL_REG	0xB00-0xBFC	DE-sprite single block attribute control register
DEBE_SPRADD_SRAM	0xC00-0xCFC	DE-sprite single block address setting SRAM array
DEBE_SPRLINEWIDTH_SRAM	0xD00-0xDFC	DE-sprite single block line width setting SRAM array
	Memories	
	0x4000-0x43FF	DE-sprite palette table
	0x4400-0x47FF	Gamma table
	0x4800-0x4BFF	DE-HWC pattern memory block
	0x4C00-0x4FFF	DE-HWC color palette table
	0x5000-0x53FF	Pipe0 palette table
	0x5400-0x57FF	Pipe1 palette table

5.4.4. DEBE Register Description

5.4.4.1. DE BACK-END MODE CONTROL REGISTER

Offset: 0x800			Register Name: DEBE_MODCTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
31:30	/	/	/
29	R/W	0	**LINE_SEL** Start top/bottom line selection in interlace mode
28	R/W	0	**ITLMOD_EN** Interlace mode enable 0:disable 1:enable
27	/	/	/
22:20	R/W	0	**OUT_SEL** Output selection 000:LCD 110:FE0 only 111:FE1 only Other: reserved
19:17	/	/	/
16	R/W	0	**HWC_EN** Hardware cursor enabled/disabled control 0: Disabled 1: Enabled Hardware cursor has the highest priority, in the alpha blender0, the alpha value of cursor will be selected
15:12	/	/	/
11	R/W	0	**LAY3_EN** Layer3 Enable/Disable 0: Disabled 1: Enabled
10	R/W	0	**LAY2_EN** Layer2 Enable/Disable 0: Disabled 1: Enabled

Offset: 0x800			Register Name: DEBE_MODCTL_REG
Bit	**Read/ Write**	**Default/ Hex**	**Description**
9	R/W	0	**LAY1_EN** Layer1 Enable/Disable 0: Disabled 1: Enabled
8	R/W	0	**LAY0_EN** Layer0 Enable/Disable 0: Disabled 1: Enabled
7:6	/	/	/
5	R/W	0	**OCSC_EN** Output CSC enable 0: disable 1: enable
4	R/W	0	**DEFLK_EN** De-flicker enable 0: disable 1: enable
3	/	/	/
2	R/W	0	**DLP_START_CTL** Direct LCD channel Start & Reset control 0: reset 1: start
1	R/W	0	**START_CTL** Normal output channel Start & Reset control 0: reset 1: start
0	R/W	0	**DEBE_EN** DE back-end enable/disable 0: disable 1: enable

5.4.4.2. DE-BACK COLOR CONTROL REGISTER

Offset: 0x804			Register Name: DEBE_BACKCOLOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	UDF	**BK_RED** Red Red screen background color value
15:8	R/W	UDF	**BK_GREEN** Green Green screen background color value
7:0	R/W	UDF	**BK_BLUE** Blue Blue screen background color value

5.4.4.3. DE-BACK DISPLAY SIZE SETTING REGISTER

Offset: 0x808			Register Name: DEBE_DISSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**DIS_HEIGHT** Display height The real display height = The value of these bits add 1
15:0	R/W	UDF	**DIS_WIDTH** Display width The real display width = The value of these bits add 1

5.4.4.4. DE-LAYER SIZE REGISTER

Offset: Layer 0: 0x810 Layer 1: 0x814 Layer 2: 0x818 Layer 3: 0x81C	Register Name: DEBE_LAYSIZE_REG

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	**LAY_HEIGHT** Layer Height The Layer Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	UDF	**LAY_WIDTH** Layer Width The Layer Width = The value of these bits add 1

5.4.4.5. DE-LAYER COORDINATE CONTROL REGISTER

Offset: **Layer 0: 0x820** **Layer 1: 0x824** **Layer 2: 0x828** **Layer 3: 0x82C**			**Register Name: DEBE_LAYCOOR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**LAY_YCOOR** Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	UDF	**LAY_XCOOR** X coordinate X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

Setting the layer0-layer3 the coordinate (left-top) on screen control information

5.4.4.6. DE-LAYER FRAME BUFFER LINE WIDTH REGISTER

Offset: Layer 0: 0x840 Layer 1: 0x844 Layer 2: 0x848 Layer 3: 0x84C			Register Name: DEBE_LAYLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**LAY_LINEWIDTH** Layer frame buffer line width in bits

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.4.4.7. DE-LAYER FRAME BUFFER LOW 32 BIT ADDRESS REGISTER

Offset: Layer 0: 0x850 Layer 1: 0x854 Layer 2: 0x858 Layer 3: 0x85C			Register Name: DEBE_LAYFB_L32ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**LAYFB_L32ADD** Buffer start Address Layer Frame start Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.4.4.8. DE-LAYER FRAME BUFFER HIGH 4 BIT ADDRESS REGISTER

Offset: 0x860			Register Name: DEBE_LAYFB_H4ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

Offset: 0x860			Register Name: DEBE_LAYFB_H4ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	UDF	**LAY3FB_H4ADD** Layer3 Layer Frame Buffer Address in bit
23:20	/	/	/
19:16	R/W	UDF	**LAY2FB_H4ADD** Layer2 Layer Frame Buffer Address in bit
15:12	/	/	/
11:8	R/W	UDF	**LAY1FB_H4ADD** Layer1 Layer Frame Buffer Address in bit
7:4	/	/	/
3:0	R/W	UDF	**LAY0FB_H4ADD** Layer0 Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.4.4.9. DE-REGISTER BUFFER CONTROL REGISTER

Offset: 0x870			Register Name: DEBE_REGBUFFCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0X00	**REGAUTOLOAD_DIS** Module registers loading auto mode disable control 0: registers auto loading mode 1: disable registers auto loading mode, the registers will be loaded by write 1 to bit0 of this register
0	R/W	0X00	**REGLOADCTL** Register load control When the Module registers loading auto mode disable control bit is set, the registers will be loaded by write 1 to the bit, and the bit

Offset: 0x870			Register Name: DEBE_REGBUFFCTL_REG
Bit	Read/Write	Default/Hex	Description
			will self clean when the registers is loading done.

5.4.4.10. DE-COLOR KEY MAX REGISTER

Offset: 0x880			Register Name: DEBE_CKMAX_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	UDF	**CKMAX_R** Red Red color key max
15:8	R/W	UDF	**CKMAX_G** Green Green color key max
7:0	R/W	UDF	**CKMAX_B** Blue Blue color key max

5.4.4.11. DE-COLOR KEY MIN REGISTER

Offset: 0x884			Register Name: DEBE_CKMIN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	UDF	**CKMIN_R** Red Red color key min
15:8	R/W	UDF	**CKMIN_G** Green Green color key min
7:0	R/W	UDF	**CKMIN_B**

Offset: 0x884			Register Name: DEBE_CKMIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Blue Blue color key min

5.4.4.12. DE-COLOR KEY CONFIGURATION REGISTER

Offset: 0x888			Register Name: DEBE_CKCFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	UDF	**CKR_MATCH** Red Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
3:2	R/W	UDF	**CKG_MATCH** Green Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
1:0	R/W	UDF	**CKB_MATCH** Blue Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)

DE-LAYER ATTRIBUTE CONTROL REGISTER0

Offset: **Layer0: 0x890** **Layer1: 0x894** **Layer2: 0x898** **Layer3: 0x89C**			**Register Name: DEBE_ATTCTL_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	**LAY_GLBALPHA** Alpha value Alpha value is used for this layer
23:22	R/W	UDF	**LAY_WORKMOD** Layer working mode selection 00: normal mode (Non-Index mode) 01: palette mode (Index mode) 10: internal frame buffer mode 11: gamma correction Except the normal mode, if the other working mode is selected, the on chip SRAM will be enabled.
21:20	/	/	/
19:18	R/W	UDF	**CKEN** Color key Mode 00: disabled color key 01: The layer color key match another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	UDF	**LAY_PIPESEL** Pipe Select 0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	UDF	**LAY_PRISEL** Priority

Offset: Layer0: 0x890 Layer1: 0x894 Layer2: 0x898 Layer3: 0x89C			Register Name: DEBE_ATTCTL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			The rule is: 11>10>01>00 When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition. If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:5	/	/	/
4	R/W	UDF	**LAY_VDOSEL** Video channel selection control 0:select video channel 0 (FE0) 1:select video channel 1 (FE1) The selection setting is only valid when Layer video channel selection is enabled.
3	/	/	/
2	R/W	UDF	**LAY_YUVEN** YUV channel selection 0: disable 1: enable Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.
1	R/W	UDF	**LAY_VDOEN** Layer video channel selection enable control 0: disable 1: enable

Offset: Layer0: 0x890 Layer1: 0x894 Layer2: 0x898 Layer3: 0x89C			Register Name: DEBE_ATTCTL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			Normally, one layer can not be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, programmer should confirm it. Setting 2 or more layers video channel mode is illegal, programmer should confirm it.
0	R/W	UDF	**LAY_GLBALPHAEN** Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

5.4.4.13. DE-LAYER ATTRIBUTE CONTROL REGISTER1

Offset: Layer0: 0x8A0 Layer1: 0x8A4 Layer2: 0x8A8 Layer3: 0x8AC			Register Name: DEBE_ATTCTL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	UDF	**LAY_HSCAFCT** Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode SH Height scale factor 00: no scaling 01: *2 10: *4

Offset: Layer0: 0x8A0 Layer1: 0x8A4 Layer2: 0x8A8 Layer3: 0x8AC			Register Name: DEBE_ATTCTL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			11: Reserved
13:12	R/W	UDF	**LAY_WSCAFCT** Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode SW Width scale factor 00: no scaling 01: *2 10: *4 11: Reserved
11:8	R/W	UDF	**LAY_FBFMT** Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp 0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5) 1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 24-bpp (Padding:8/R:8/G:8/B:8) 1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R:8/G:8/B:8) 1100: color 16-bpp (Alpha:4/R:4/G:4/B:4) Other: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp

Offset: Layer0: 0x8A0 Layer1: 0x8A4 Layer2: 0x8A8 Layer3: 0x8AC			Register Name: DEBE_ATTCTL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0011: 8-bpp other: Reserved Internal Frame buffer mode data format 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp Other: Reserved
7:3	/	/	/
2	R/W	UDF	**LAY_BRSWAPEN** B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
1:0	R/W	UDF	**LAY_FBPS** PS Pixels Sequence See the follow table "Pixels Sequence"

5.4.4.14. PIXELS SEQUENCE TABLE

DE-layer attribute control register1 [11:08] = FBF (frame buffer format)
DE-layer attribute control register1 [01:00] = PS (pixels sequence)

Mono or internal frame buffer 1-bpp or palette 1-bpp mode : FBF = 0000
PS=00
Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23
P08	P09	P10	P11	P12	P13	P14	P15	P00	P01	P02	P03	P04	P05	P06	P07

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P07	P06	P05	P04	P03	P02	P01	P00	P15	P14	P13	P12	P11	P10	P09	P08
P23	P22	P21	P20	P19	P18	P17	P16	P31	P30	P29	P28	P27	P26	P25	P24

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15
P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Mono or internal frame buffer 2-bpp or palette 2-bpp mode : FBF = 0001

PS=00

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P15	P14	P13	P12	P11	P10	P09	P08
P07	P06	P05	P04	P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P12	P13	P14	P15	P08	P09	P10	P11
P04	P05	P06	P07	P00	P01	P02	P03

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P03	P02	P01	P00	P07	P06	P05	P04
P11	P10	P09	P08	P15	P14	P13	P12

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P00	P01	P02	P03	P04	P05	P06	P07
P08	P09	P10	P11	P12	P13	P14	P15

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Mono 4-bpp or palette 4-bpp mode : FBF = 0010

PS=00

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P07	P06	P05	P04
P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P06	P07	P04	P05
P02	P03	P00	P01

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P01	P00	P03	P02
P05	P04	P07	P06

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P00	P01	P02	P03
P04	P05	P06	P07

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Mono 8-bpp mode or palette 8-bpp mode : FBF = 0011

PS=00/11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P3	P2
P1	P0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=01/10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P0	P1
P2	P3

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Color 16-bpp mode : FBF = 0100 or 0101 or 0110 or 0111 or 1000

PS=00

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P1
P0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P0
P1

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=10/11

Invalid

Color 24-bpp or 32-bpp mode : FBF = 1001 or 1010

PS=00/01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
The bytes sequence is ARGB
PS=10/11
Bit
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
The bytes sequence is BGRA

5.4.4.15. DE-HWC COORDINATE CONTROL REGISTER

Offset: 0x8D8			**Register Name: DEBE_HWCCTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**HWC_YCOOR** Hardware cursor Y coordinate
15:0	R/W	UDF	**HWC_XCOOR** Hardware cursor X coordinate

5.4.4.16. DE-HWC FRAME BUFFER FORMAT REGISTER

Offset: 0x8E0			**Register Name: DEBE_HWCFBCTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	**HWC_YCOOROFF** Y coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in Y coordinate
23:16	R/W	UDF	**HWC_XCOOROFF** X coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in X coordinate
15:6	/	/	/
5:4	R/W	UDF	**HWC_YSIZE**

Offset: 0x8E0			Register Name: DEBE_HWCFBCTL_REG
Bit	Read/Write	Default/Hex	Description
			Y size control 00: 32pixels per line 01: 64pixels per line Other: reserved
3:2	R/W	UDF	**HWC_XSIZE** X size control 00: 32pixels per row 01: 64pixels per row Other: reserved
1:0	R/W	UDF	**HWC_FBFMT** Pixels format control 00: 1bpp 01: 2bpp 10: 4bpp 11: 8bpp

5.4.4.17. DE BACKEND WRITE BACK CONTROL REGISTER

Offset: 0x8F0			Register Name: DEBE_WBCTL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	UDF	**WB_FMT** Write back data format setting 0: ARGB (little endian system) 1: BGRA (little endian system)
11:10	/	/	/
9	R/W	UDF	**WB_EFLAG** Error flag 0: 1: write back error

Offset: 0x8F0			Register Name: DEBE_WBCTL_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	UDF	**WB_STATUS** Write-back process status 0: write-back end or write-back disable 1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
7:2	/	/	/
1	R/W	UDF	**WB_WOC** Write back only control 0: disable the write back only control, the normal channel data of back end will transfer to LCD/TV controller too. 1: enable the write back only function, the all output data will by pass the LCD/TV controller.
0	R/W	UDF	**WB_EN** Write back enable 0: Disable 1: Enable If normal channel of back-end is selected by LCD/TV controller (write back only function is disabled), the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be cleared when the new writing-back frame start to process.

5.4.4.18. DE BACKEND WRITE BACK ADDRESS REGISTER

Offset: 0x8F4	Register Name: DEBE_WBADD_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	**WB_ADD** The start address of write back data in WORD

5.4.4.19. DE BACKEND WRITE BACK BUFFER LINE WIDTH REGISTER

Offset: 0x8F8			Register Name: DEBE_WBLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**WB_LINEWIDTH** Write back image buffer line width in bits

5.4.4.20. DE-SPRITE ENABLE REGISTER

Offset: 0x900			Register Name: DEBE_SPREN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	UDF	**SPR_EN** 0: disable 1: enable

5.4.4.21. DE-SPRITE FORMAT CONTROL REGISTER

Offset: 0x908			Register Name: DEBE_SPRFMTCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	UDF	**SPR_FBPS** Pixel sequence

Offset: 0x908			Register Name: DEBE_SPRFMTCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: 1: Reference the following illustration
11:9	/	/	/
8	R/W	UDF	**SPR_FBFMT** Frame buffer format 0:32bpp mode 1:8bpp palette mode
7:0	/	/	/

5.4.4.22. PIXELS SEQUENCE DESCRIPTION:

32bpp mode: (bit8 will be set 0)
The setting status of the DE-sprite format control register bit12
0:
ARGB (little endian system)
1:
BGRA (little endian system)

8bpp palette mode: (bit8 will be set 1)
The setting status of the DE-sprite format control register bit12
0:
Bit
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P3	P2
P1	P0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

1:
Bit
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P0	P1
P2	P3

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

DE-SPRITE ALPHA CONTROL REGISTER

Offset: 0x90C			Register Name: DEBE_SPRALPHACTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	**SPR_GLBALPHA** Globe alpha value
23:1	/	/	/
0	R/W	UDF	**SPR_GLBALPHAEN** 0: Disable the globe alpha function 1: Enable the globe alpha function, when the function is set, the sprite will use the globe alpha value to calculate the display pixels.

5.4.4.23. DE-SPRITE SINGLE BLOCK COORDINATE CONTROL REGISTER

Offset: Block 0: 0xA00 Block 1: 0xA04 Block 2: 0xA08 . . . Block 31: 0xA7C			Register Name: DEBE_SPRCOORCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**SPR_YCOOR** Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	UDF	**SPR_XCOOR** X coordinate X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

Note: this register is used to set the single block (block 0----block 31) the coordinate (left-top) on screen control information

5.4.4.24. DE-SPRITE SINGLE BLOCK ATTRIBUTE CONTROL REGISTER

Offset: Block 0: 0xB00 Block 1: 0xB04 Block 2: 0xB08 . . . Block 31: 0xB7C			Register Name: DEBE_SPRATTCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	UDF	**SPR_HEIGHT** Single block height The real block height = The value of these bits add 1
19:8	R/W	UDF	**SPR_WIDTH** Single block width The real block width = The value of these bits add 1
7:6	/	/	/
5:0	R/W	UDF	**SPR_NEXTID** The value determine the next block ID number from 0-31

5.4.4.25. DE-SPRITE SINGLE BLOCK ADDRESS SETTING SRAM ARRAY

Offset: Block 0: 0xC00 Block 1: 0xC04 Block 2: 0xC08 . . . Block 31: 0xC7C			Register Name: DEBE_SPRADD_SRAM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**SPR_ADD** Sprite start address Sprite buffer start address in BYTE

DE-SPRITE LINE WIDTH SETTING SRAM ARRAY

Offset: Block 0: 0xD00 Block 1: 0xD04 Block 2: 0xD08 . . . Block 31: 0xD7C			Register Name: DEBE_SPRLINEWIDTH_SRAM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**SPR_LINEWIDTH** Sprite single block line width Sprite single block line width in bits

5.4.4.26. DE BACKEND INPUT YUV CHANNEL CONTROL REGISTER

Offset: 0x920			Register Name: DEBE_IYUVCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x920			Register Name: DEBE_IYUVCTL_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:12	R/W	UDF	**IYUV_FBFMT** Input data format 000: planar YUV 411 001: planar YUV 422 010: planar YUV 444 011: interleaved YUV 422 100: interleaved YUV 444 Other: illegal
11:10	/	/	/
9:8	R/W	UDF	**IYUV_FBPS** Pixel sequence **In planar data format mode:** 00: Y3Y2Y1Y0 01: Y0Y1Y2Y3 (the other 2 components are same) Other: illegal **In interleaved YUV 422 data format mode:** 00: UYVY 01: YUYV 10: VYUY 11: YVYU **In interleaved YUV 444 data format mode:** 00: AYUV 01: VUYA Other: illegal
7:5	/	/	/
4	R/W	UDF	**IYUV_LINNEREN** 0: linner 1:
3:1	/	/	/
0	R/W	UDF	**IYUV_EN** YUV channel enable control 0: disable

Offset: 0x920			Register Name: DEBE_IYUVCTL_REG
Bit	Read/Write	Default/Hex	Description
			1: enable

5.4.4.27. SOURCE DATA INPUT DATA PORTS

Input buffer channel	Planar YUV	Interleaved YUV
Channel0	Y	YUV
Channel1	U	-
Channel2	V	-

5.4.4.28. DE BACKEND YUV CHANNEL FRAME BUFFER ADDRESS REGISTER

Offset: Channel 0 : 0x930 Channel 1 : 0x934 Channel 2 : 0x938			Register Name: DEBE_IYUVADD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	**IYUV_ADD** Buffer Address Frame buffer address in BYTE

5.4.4.29. DE BACKEND YUV CHANNEL BUFFER LINE WIDTH REGISTER

Offset: Channel 0 : 0x940 Channel 1 : 0x944 Channel 2 : 0x948	Register Name: DEBE_IYUVLINEWIDTH_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	**IYUV_LINEWIDTH** Line width The width is the distance from the start of one line to the start of the next line. Description in bits

YUV to RGB conversion algorithm formula:

R =
(R Y component coefficient * Y) +
(R U component coefficient * U) +
(R V component coefficient * V) +
R constant

G =
(G Y component coefficient * Y) +
(G U component coefficient * U) +
(G V component coefficient * V) +
G constant

B =
(B Y component coefficient * Y) +
(B U component coefficient * U) +
(B V component coefficient * V) +
B constant

5.4.4.30. DE BACKEND Y/G COEFFICIENT REGISTER

Offset: **G/Y component: 0x950** **R/U component: 0x954** **B/V component: 0x958**			**Register Name: DEBE_YGCOEF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	UDF	**DF_YGCOEF** the Y/G coefficient for de-flicker the value equals to coefficient*2^{10}

Offset: G/Y component: 0x950 R/U component: 0x954 B/V component: 0x958			Register Name: DEBE_YGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
12:0	R/W	UDF	**IYUV_YGCOEF** the Y/G coefficient the value equals to coefficient*2^{10}

5.4.4.31. DE BACKEND Y/G CONSTANT REGISTER

Offset: 0x95C			Register Name: DEBE_YGCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	UDF	**DF_YGCONS** the Y/G constant for de-flicker the value equals to coefficient*2^4
15:14	/	/	/
13:0	R/W	UDF	**IYUV_YGCONS** the Y/G constant the value equals to coefficient*2^4

5.4.4.32. DE BACKEND U/R COEFFICIENT REGISTER

Offset: G/Y component: 0x960 R/U component: 0x964 B/V component: 0x968			Register Name: DEBE_URCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

Offset: G/Y component: 0x960 R/U component: 0x964 B/V component: 0x968			Register Name: DEBE_URCOEF_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
28:16	R/W	UDF	**DF_URCOEF** the U/R coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	**IYUV_URCOEF** the U/R coefficient the value equals to coefficient*2^{10}

5.4.4.33. DE BACKEND U/R CONSTANT REGISTER

Offset: 0x96C			Register Name: DEBE_URCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	UDF	**DF_URCONS** the U/R constant for de-flicker the value equals to coefficient*2^{4}
15:14	/	/	/
13:0	R/W	UDF	**IYUV_URCONS** the U/R constant the value equals to coefficient*2^{4}

5.4.4.34. DE BACKEND V/B COEFFICIENT REGISTER

Offset: G/Y component: 0x970 R/U component: 0x974 B/V component: 0x978	Register Name: DEBE_VBCOEF_REG

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	**DF_VBCOEF** the V/B coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	**IYUV_VBCOEF** the V/B coefficient the value equals to coefficient*2^{10}

5.4.4.35. DE BACKEND V/B CONSTANT REGISTER

Offset: 0x97C			Register Name: DEBE_VBCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	UDF	**DF_VBCONS** the V/B constant for de-flicker the value equals to coefficient*2^4
15:14	/	/	/
13:0	R/W	UDF	**IYUV_VBCONS** the V/B constant the value equals to coefficient*2^4

5.4.4.36. DE BACKEND KEYSTONE CORRECTION CONTROL REGISTER

Offset: 0x980			Register Name: DEBE_KSCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	UDF	**KS_EN** 0: disable 1: enable

5.4.4.37. DE BACKEND KEYSTONE BACK COLOR CONTROL REGISTER

Offset: 0x984			Register Name: DEBE_KSBKCOLOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	UDF	**KS_BKRED** Red Red screen background color value
15:8	R/W	UDF	**KS_BKGREEN** Green Green screen background color value
7:0	R/W	UDF	**KS_BKBLUE** Blue Blue screen background color value

5.4.4.38. DE BACKEND KEYSTONE OUTPUT FIRST LINE WIDTH SETTING REGISTER

Offset: 0x988			Register Name: DEBE_KSFSTLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	UDF	**KS_FSTLINEWIDTH** Output first line width in pixels The width = The value of these bits add 1

5.4.4.39. DE BACKEND KEYSTONE VERTICAL SCALING FACTOR REGISTER

Offset: 0x98C			Register Name: DEBE_KSVSCAFCT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x98C			Register Name: DEBE_KSVSCAFCT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	UDF	**KS_VSCASIGN** Sign bit 0:increasing 1:decreasing
30:24	/	/	/
23:16	R/W	UDF	**KS_VSCAIRATIO** The integer part of the vertical scaling ratio
15:12	/	/	/
11:0	R/W	UDF	**KS_VSCAFRATIO** The fractional part of the vertical scaling ratio

5.4.4.40. DE BACKEND KEYSTONE HORIZONTAL FILTERING COEFFICIENT RAM BLOCK

Offset: 0x9A0 – 0x9BC			Register Name: DEBE_KSHSCACOEF_RAM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	**KS_HSCATAP3COEF** Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	UDF	**KS_HSCATAP2COEF** Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	UDF	**KS_HSCATAP1COEF** Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	UDF	**KS_HSCATAP0COEF** Horizontal tap0 coefficient The value equals to coefficient*2^6

5.4.4.41. DE BACKEND OUTPUT COLOR CONTROL REGISTER

Offset: 0x9C0			Register Name: DEBE_OCCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	UDF	**OC_EN** Color control module enable control 0: disable 1: enable

5.4.4.42. COLOR CORRECTION CONVERSION ALGORITHM FORMULA:

R =
(R R component coefficient * R) +
(R G component coefficient * G) +
(R B component coefficient * B) +
R constant

G =
(G R component coefficient * R) +
(G G component coefficient * G) +
(G B component coefficient * B) +
G constant

B =
(B R component coefficient * R) +
(B G component coefficient * G) +
(B B component coefficient * B) +
B constant

5.4.4.43. DE BACKEND OUTPUT COLOR R COEFFICIENT REGISTER

Offset: R component: 0x9D0 G component: 0x9D4 B component: 0x9D8	Register Name: DEBE_OCRCOEF_REG

Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	**OC_RCOEF** the R coefficient the value equals to coefficient*2^{10}

5.4.4.44. DE BACKEND OUTPUT COLOR R CONSTANT REGISTER

Offset: 0x9DC			Register Name: DEBE_OCRCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	UDF	**OC_RCONS** the R constant the value equals to coefficient*2^{4}

5.4.4.45. DE BACKEND OUTPUT COLOR G COEFFICIENT REGISTER

Offset: R component: 0x9E0 G component: 0x9E4 B component: 0x9E8			Register Name: DEBE_OCGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	UDF	**OC_GCOEF** the G coefficient the value equals to coefficient*2^{10}

5.4.4.46. DE BACKEND OUTPUT COLOR G CONSTANT REGISTER

Offset: 0x9EC			Register Name: DEBE_OCGCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	UDF	**OC_GCONS** the G constant the value equals to coefficient*2^4

5.4.4.47. DE BACKEND OUTPUT COLOR B COEFFICIENT REGISTER

Offset: G/Y component: 0x9F0 R/U component: 0x9F4 B/V component: 0x9F8			Register Name: DEBE_OCBCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	UDF	**OC_BCOEF** the B coefficient the value equals to coefficient*2^{10}

5.4.4.48. DE BACKEND OUTPUT COLOR B CONSTANT REGISTER

Offset: 0x9FC			Register Name: DEBE_OCBCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	UDF	**OC_BCONS** the B constant the value equals to coefficient*2^4

5.4.4.49. DE-HWC PATTERN MEMORY BLOCK

Function:

1bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P15		P14		P13		P12		P11		P10		P09		P08	
P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

4bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07				P06				P05				P04			
P03				P02				P01				P00			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

8bpp:

Bit

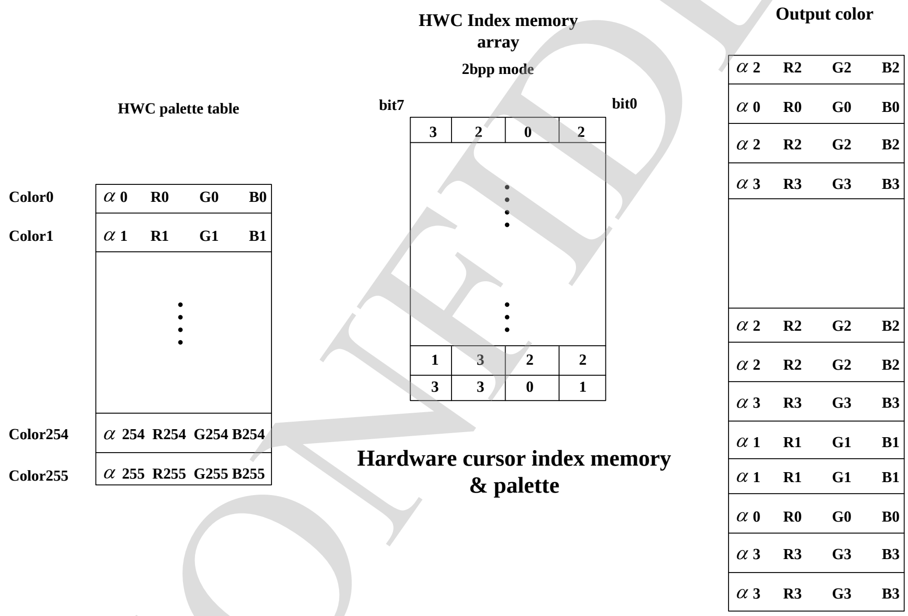
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Offset: 0x4800-0x4BFF			**DE-HW cursor pattern memory block**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	Hardware cursor pixel pattern Specify the color displayed for each of the hardware cursor pixels.

5.4.4.50. DE-HWC PALETTE TABLE

Offset: 0x4C00-0x4FFF			DE-HW palette table
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

The following figure (only with 2bpp mode) shows the RAM array used for hardware cursor palette lookup and the corresponding colors output.



Hardware cursor index memory & palette

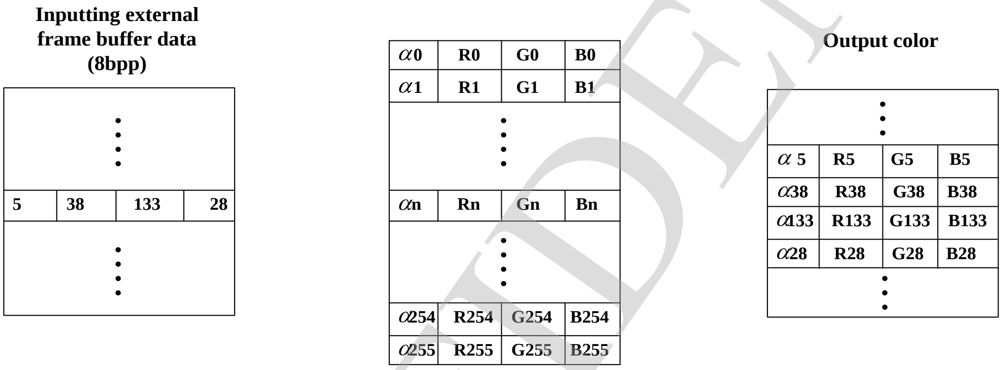
5.4.4.51. SPRITE PALETTE TABLE

Offset: 0x4000-0x43FF	DE-sprite palette SRAM block

Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

In this mode, the sprite RAM array is used for palette lookup table, each pixel in the sprite frame buffer is treated as an index into the RAM array to select the actual color.

The following figure shows the RAM array used for palette lookup and the corresponding colors output.



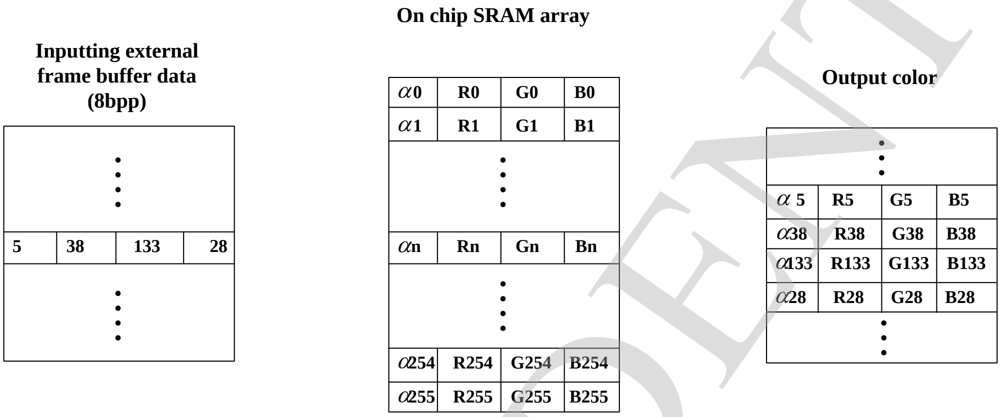
5.4.4.52. PALETTE MODE

Offset: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			Pipe palette color table SRAM block
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	

Offset: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			**Pipe palette color table SRAM block**
			Green value
7:0	R/W	UDF	Blue value

In this mode, RAM array is used for palette lookup table, each pixel in the layer frame buffer is treated as an index into the RAM array to select the actual color.

The following figure shows the RAM array used for palette lookup and the corresponding colors output.



On chip SRAM for palette lookup

5.4.4.53. INTERNAL FRAME BUFFER MODE

In internal frame buffer mode, the RAM array is used as an on-chip frame buffer, each pixel in the RAM array is used to select one of the palette 32-bit colors.

1bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P15	P14	P13	P12	P11	P10	P09	P08

P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

4bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07				P06				P05				P04			
P03				P02				P01				P00			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

8bpp:

Bit

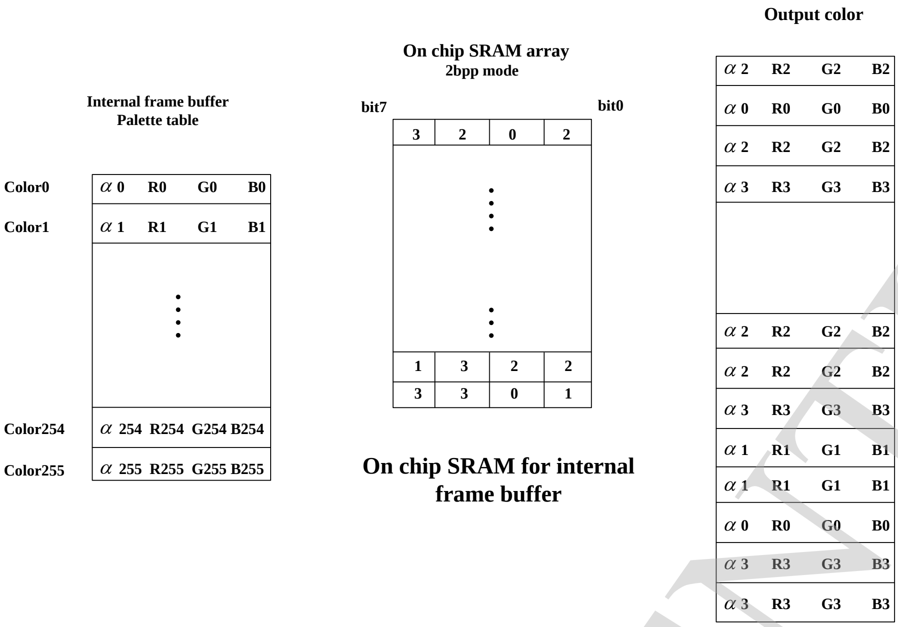
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Offset: 0x4000-0x57FF			**DE-on chip SRAM block**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	Internal frame buffer pixel pattern Specify the color displayed for each of the internal frame buffer pixels.

5.4.4.54. INTERNAL FRAME BUFFER MODE PALETTE TABLE

Address: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			**Pipe palette table**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

The following figure shows the RAM array used for internal frame buffer mode and the corresponding colors output.

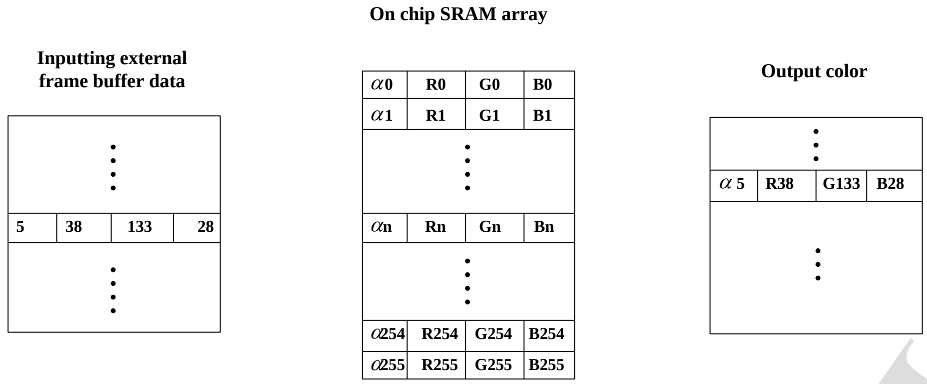


5.4.4.55. GAMMA CORRECTION MODE

Offset: 0x4400-0x47FF			**DE-on chip SRAM block**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha channel intensity
23:16	R/W	UDF	Red channel intensity
15:8	R/W	UDF	Green channel intensity
7:0	R/W	UDF	Blue channel intensity

In gamma correction mode, the RAM array is used for gamma correction, each pixel’s alpha, red, green, and blue color component is treated as an index into the SRAM array. The corresponding alpha, red, green, or blue channel intensity value at that index is used in the actual color.

The following figure shows the RAM array used for gamma correction and the corresponding colors output.



On chip SRAM for gamma correction

5.4.4.56. DISPLAY ENGINE MEMORY MAPPING

Base Address:
BE0: 0x01e60000
BE1: 0x01e40000

Offset:

0x0000	0x07FF	Reserved
0x0800	0x0DFF	Registers
0x0E00	0x3FFF	Reserved
0x4000	0x43FF	Reserved
0x4400	0x47FF	Gamma Table
0x4800	0x4BFF	HWC Memory Block
0x4C00	0x4FFF	HWC Palette Table
0x5000	0x53FF	PIPE0 Palette Table
0x5400	0x57FF	PIPE1 Palette Table
0x5800	0xFFFF	Reserved

5.5. TV Encoder

5.5.1. Overview

- Support CVBS NTSC,PAL, 4-channel CVBS output
- Support YPbPr 1080p60,1080p50,720p60,720p50,576p,480p,576i,480i
- Support VGA up to 1920x1200@60Hz
- Plug auto detection in CVBS and YpbPr

Chapter 6 Interface

This section details the interfaces that provided in A20, mainly includes:

- SD3.0
- TWI
- SPI
- UART
- PS2
- IR
- USB OTG
- USB HOST
- DIGITAL AUDIO INTERFACE
- AC97
- EMAC
- GMAC
- TRANSPORT STREAM
- SMART CARD READER
- SATA HOST
- CAN
- KEYPAD

6.1. SD3.0

6.1.1. Overview

The SD3.0 controller can be configured as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

It features:

- Support industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endean bus.
- Support AMBA AHB Slave mode
- Support Secure Digital memory protocol commands (up to SD3.0)
- Support Secure Digital I/O protocol commands
- Support Multimedia Card protocol commands (up to MMC4.3)
- Support CE-ATA digital protocol commands
- Support eMMC boot operation and alternative boot operation
- Support Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Support one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.3) or CE-ATA device
- Support hardware CRC generation and error detection
- Support programmable baud rate
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 32x32-bit (128 bytes total) FIFO for data transfer
- Support 3.3 V IO pad

6.1.2. SD3.0 Timing Diagram

Please refer to related specifications:

- Physical Layer Specification Ver3.00 Final, 2009.04.16
- SDIO Specification Ver2.00
- Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard

6.2. TWI

6.2.1. Overview

The TWI is designed to be used as an interface between CPU host and the serial 2-Wire bus. It can support all standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This TWI can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

The TWI features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Software-programmable for Slave or Master
- Support Repeated START signal
- Support multi-master systems
- Allow 10-bit addressing with 2-Wire bus
- Perform arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Support speed up to 400Kbits/s (‘fast mode’)
- Allow operation from a wide range of input clock frequencies

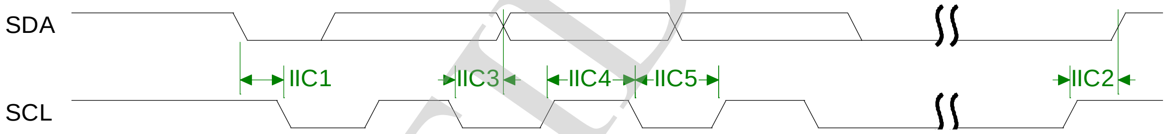
6.2.2. TWI Controller Timing Diagram

Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each bytes. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a “not acknowledge”) to the transmitter.

When a slave receiver doesn’t acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can then generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Following diagram provides an illustration the relation of SDA signal line and SCL signal line on the 2-Wire serial bus.



6.2.3. TWI Controller Register List

Module Name	Base Address
TWI0	0x01C2AC00
TWI1	0x01C2B000
TWI2	0x01C2B400
TWI3	0x01C2B800
TWI4	0x01C2C000

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address
TWI_XADDR	0x0004	TWI Extended slave address
TWI_DATA	0x0008	TWI Data byte
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock control register
TWI_SRST	0x0018	TWI Software reset
TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register

6.2.4. TWI Register Description

6.2.4.1. TWI SLAVE ADDRESS REGISTER

Offset: 0x00			**Register Name: TWI_ADDR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:1	R/W	0	SLA Slave address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0	GCE General call address enable 0: Disable 1: Enable

Note:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the 2-Wire bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

6.2.4.2. TWI EXTEND ADDRESS REGISTER

Offset: 0x04			Register Name: TWI_XADDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	SLAX Extend Slave Address SLAX[7:0]

6.2.4.3. TWI DATA REGISTER

Offset: 0x08			Register Name: TWI_DATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	TWI_DATA Data byte for transmitting or received

6.2.4.4. TWI CONTROL REGISTER

Offset: 0x0C			Register Name: TWI_CNTR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	INT_EN Interrupt Enable 1'b0: The interrupt line always low 1'b1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0	BUS_EN 2-Wire Bus Enable 1'b0: The 2-Wire bus inputs ISDA/ISCL are ignored and the 2-Wire Controller will not respond to any address on the bus 1'b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to '1'
5	R/W	0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the 2-Wire Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect.
4	R/W	0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the 2-Wire bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the 2-Wire bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this

Offset: 0x0C			Register Name: TWI_CNTR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			bit has no effect.
3	R/W	0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the 2-wire bus clock line (SCL) is stretched until '0' is written to INT_FLAG. The 2-wire clock line is then released and the interrupt line goes low.
2	R/W	0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the 2-Wire bus if: a. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. b. The general call address has been received and the GCE bit in the ADDR register is set to '1'. c. A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	R/W	0	/

6.2.4.5. TWI STATUS REGISTER

Offset: 0x10			Register Name: TWI_STAT Default Value: 0x0000_00F8
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received

Offset: 0x10			Register Name: TWI_STAT Default Value: 0x0000_00F8
Bit	**Read/Write**	**Default**	**Description**
			0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

6.2.4.6. TWI CLOCK REGISTER

Offset: 0x14			Register Name: TWI_CCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:3	R/W	0	CLK_M
2:0	R/W	0	CLK_N The 2-Wire bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example: Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48M/2^2=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48M/2^2=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

TWI SOFT RESET REGISTER

Offset: 0x18			Register Name: TWI_SRST Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

Offset: 0x18			Register Name: TWI_SRST Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:1	/	/	/
0	R/W	0	SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation.

6.2.4.7. TWI ENHANCE FEATURE REGISTER

Offset: 0x1C			Register Name: TWI_EFR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/
0:1	R/W	0	DBN Data Byte number follow Read Command Control No Data Byte to be wrote after read command Only 1 byte data to be wrote after read command 2 bytes data can be wrote after read command 3 bytes data can be wrote after read command

6.2.4.8. TWI LINE CONTROL REGISTER

Offset: 0x20			Register Name: TWI_LCR Default Value: 0x0000_003a
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5	R	1	SCL_STATE Current state of TWI_SCL 0 – low 1 - high
4	R	1	SDA_STATE Current state of TWI_SDA

Offset: 0x20			Register Name: TWI_LCR Default Value: 0x0000_003a
Bit	**Read/Write**	**Default**	**Description**
			0 – low 1 - high
3	R/W	1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level
2	R/W	0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode
1	R/W	1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 – output low level 1 – output high level
0	R/W	0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode

6.2.4.9. TWI DVFS CONTROL REGISTER

Offset: 0x24			Register Name: TWI_DVFSCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/

Offset: 0x24			Register Name: TWI_DVFSCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
2	R/W	0	MS_PRIORITY CPU and DVFS BUSY set priority select 0: CPU has higher priority 1: DVFS has higher priority
1	R/W	0	CPU_BUSY_SET CPU Busy set
0	R/W	0	DVFC_BUSY_SET DVFS Busy set

Note: This register is only implemented in TWI0.

6.2.5. TWI Controller Special Requirement

6.2.5.1. TWI PIN LIST

Port Name	Width	Direction	Description
TWI_SCL	1	IN/OUT	TWI Clock line
TWI_SDA	1	IN/OUT	TWI Serial Data line

6.2.5.2. TWI CONTROLLER OPERATION

There are four operation modes on the 2-Wire bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to it's registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

6.3. SPI

6.3.1. Overview

The SPI allows rapid data communication with fewer software interrupts. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode.

It features:

- Support industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus.
- Support AMBA AHB Slave mode
- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals for SPI0 and SPI1 has one chip select
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Support dedicated DMA

6.3.2. SPI Timing Diagram

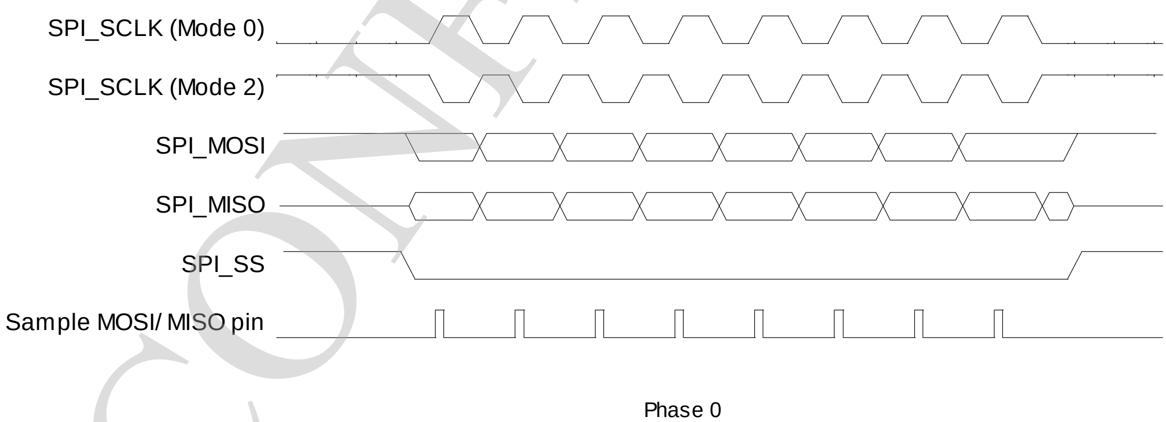
The serial peripheral interface master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

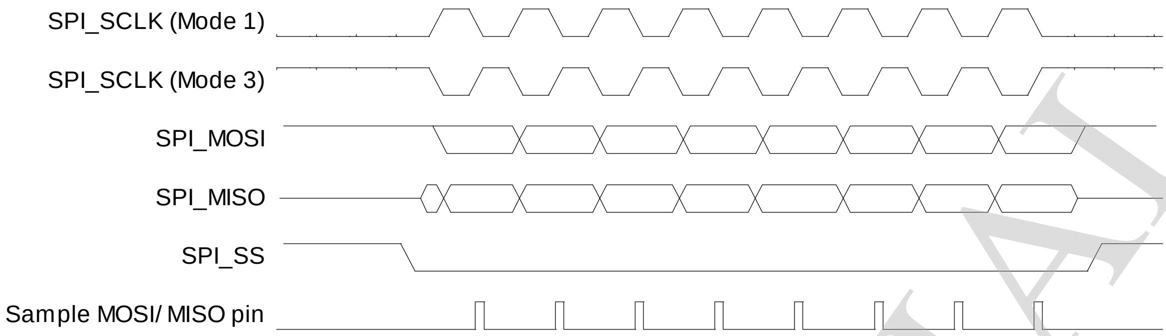
During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is ‘1’ and it is low level when POL is ‘0’. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is ‘1’ and for sample data when PHA is ‘0’. The four kind of modes are listed below:

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample



SPI Phase 0 Timing Diagram



Phase 1

SPI Phase 1 Timing Diagram

6.3.3. SPI Register List

Module Name	Base Address
SPI0	0x01C05000
SPI1	0x01C06000
SPI2	0x01C17000
SPI3	0x01C1F000

Register Name	Offset	Description
SPI_RXDATA	0x00	SPI RX Data register
SPI_TXDATA	0x04	SPI TX Data register
SPI_CTL	0x08	SPI Control register
SPI_INTCTL	0x0C	SPI Interrupt Control register
SPI_ST	0x10	SPI Status register
SPI_DMACTL	0x14	SPI DMA Control register
SPI_WAIT	0x18	SPI Wait Clock Counter register
SPI_CCTL	0x1C	SPI Clock Rate Control register
SPI_BC	0x20	SPI Burst Counter register

Register Name	Offset	Description
SPI_TC	0x24	SPI Transmit Counter Register
SPI_FIFO_STA	0x28	SPI FIFO Status register

6.3.4. SPI Register Description

6.3.4.1. SPI RX DATA REGISTER

Offset: 0x00			Register Name: SPI_RXDATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	RDATA Receive Data In 8-bits SPI bus width, this register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are words in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, the two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4.

6.3.4.2. SPI TX DATA REGISTER

Offset: 0x04			Register Name: SPI_TXDATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0	TDATA Transmit Data

6.3.4.3. SPI CONTROL REGISTER

Offset: 0x08			Register Name: SPI_CTL Default Value: 0x0012_001C
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20	R/W	1	SDM Master Sample Data Mode 1 - Normal Sample Mode 0 - Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
19	R/W	0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 1 – delay internal read sample point 0 – normal operation, do not delay internal read sample point
18	R/W	0	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1 – stop transmit data when RXFIFO full 0 – normal operation, ignore RXFIFO status
17	R/W	1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 1 – set SS to high 0 – set SS to low
16	R/W	0	SS_CTRL SS Output Mode Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTRL_REG.SS_LEVEL (bit [17]) to 1 or 0 to control the level of SS signal.

Offset: 0x08			Register Name: SPI_CTL Default Value: 0x0012_001C
Bit	**Read/Write**	**Default**	**Description**
			1 – manual output SS 0 – automatic output SS
15	R/W	0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by WTC.
14	R/W	0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one
13:12	R/W	0	SS SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Notes: This two bits can't be configured for SPI1 Engine.
11	R/W	0	RPSM Rapids mode select Select rapids operation for high speed read. 0: normal read mode 1: rapids read mode
10	R/W	0	XCH Exchange Burst In master mode it is used to start to SPI burst 0: Idle 1: Initiates exchange. After finishing the SPI bursts transfer specified by BC, this bit is cleared to zero by SPI Controller.
9	R/W	0	RF_RST RXFIFO Reset Write '1' to reset the control portion of the receiver FIFO and

Offset: 0x08			Register Name: SPI_CTL Default Value: 0x0012_001C
Bit	**Read/Write**	**Default**	**Description**
			treats the FIFO as empty. It is 'self-clearing'. It is not necessary to clear this bit.
8	R/W	0	TF_RST TXFIFO Reset Write '1' to reset the control portion of the transmit FIFO and treats the FIFO as empty. It is 'self-clearing'. It is not necessary to clear this bit.
7	R/W	0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts
6	R/W	0	LMTF LSB/ MSB Transfer First select 0: MSB first 1: LSB first
5	R/W	0	DMAMC SPI DMA Mode Control 0: Normal DMA mode 1: Dedicate DMA mode
4	R/W	1	SSPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
3	R/W	1	POL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
2	R/W	1	PHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data)
1	R/W	0	MODE SPI Function Mode Select

Offset: 0x08			Register Name: SPI_CTL Default Value: 0x0012_001C
Bit	**Read/Write**	**Default**	**Description**
			0: Slave Mode 1: Master Mode
0	R/W	0	EN SPI Module Enable Control 0: Disable 1: Enable

6.3.4.4. SPI INTERRUPT CONTROL REGISTER

Offset: 0x0C			Register Name: SPI_INTCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
17	R/W	0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
16	R/W	0	TX_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0	TF_UR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
13	R/W	0	TF_OF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
12	R/W	0	TF_E34_INT_EN

Offset: 0x0C			Register Name: SPI_INTCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			TX FIFO 3/4 Empty Interrrupt Enable 0: Disable 1: Enable
11	R/W	0	TF_E14_INT_EN TX FIFO 1/4 Empty Interrrupt Enable 0: Disable 1: Enable
10	R/W	0	TF_FL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
9	R/W	0	TF_HALF_EMP_INT_EN TX FIFO Half Empty Interrupt Enable 0: Disable 1: Enable
8	R/W	0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0	RF_UR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	RF_OF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
4	R/W	0	RF_F34_INT_EN RXFIFO 3/4 Full Interrupt Enable 0: Disable 1: Enable
3	R/W	0	RF_F14_INT_EN RX FIFO 1/4 Full Interrupt Enable

Offset: 0x0C			Register Name: SPI_INTCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			0: Disable 1: Enable
2	R/W	0	RF_FU_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RF_HALF_FU_INT_EN RX FIFO Half Full Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RF_RDY_INT_EN RX FIFO Ready Interrupt Enable 0: Disable 1: Enable

6.3.4.5. SPI INTERRUPT STATUS REGISTER

Offset: 0x10			Register Name: SPI_INT_STA Default Value: 0x0000_1B00
Bit	**Read/Write**	**Default**	**Description**
31	R	0	INT_CBF Interrupt Clear Busy Flag 0: clear interrupt flag done 1; clear interrupt flag busy
30:18	/	/	/
17	R/W	0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
16	R/W	0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit

Offset: 0x10			Register Name: SPI_INT_STA Default Value: 0x0000_1B00
Bit	**Read/Write**	**Default**	**Description**
			indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
15	/	/	/
14	R/W	0	TU TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
13	R/W	0	TO TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
12	R/W	1	TE34 TXFIFO 3/4 empty This bit is set if the TXFIFO is more than 3/4 empty. Writing 1 to this bit clears it.
11	R/W	1	TE14 TXFIFO 1/4 empty This bit is set if the TXFIFO is more than 1/4 empty. Writing 1 to this bit clears it.
10	R/W	0	TF TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
9	R/W	1	THE TXFIFO Half empty This bit is set if the TXFIFO is more than half empty. Writing 1 to this bit clears it.

Offset: 0x10			Register Name: SPI_INT_STA Default Value: 0x0000_1B00
Bit	**Read/Write**	**Default**	**Description**
			0: TXFIFO holds more than half words 1: TXFIFO holds half or fewer words
8	R/W	1	TE TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
7	/	/	/
6	R/W	0	RU RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
5	R/W	0	RO RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
4	R/W	0	RF34 RXFIFO 3/4 Full This bit is set when the RXFIFO is 3/4 full . Writing 1 to this bit clears it. 0: Not 3/4 Full 1: 3/4 Full
3	R/W	0	RF14 RXFIFO 1/4 Full This bit is set when the RXFIFO is 1/4 full . Writing 1 to this bit clears it. 0: Not 1/4 Full 1: 1/4 Full
2	R/W	0	RF RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full

Offset: 0x10			Register Name: SPI_INT_STA Default Value: 0x0000_1B00
Bit	**Read/Write**	**Default**	**Description**
			1: Full
1	R/W	0	RHF RXFIFO Half Full. This bit is set if the RXFIFO is half full (≥ 4 words in RXFIFO) . Writing 1 to this bit clears it. 0: Less than 4 words are stored in RXFIFO. 1: Four or more words are available in RXFIFO.
0	R/W	0	RR RXFIFO Ready This bit is set any time there is one or more words stored in RXFIFO (≥ 1 words) . Writing 1 to this bit clears it. 0: No valid data in RXFIFO 1: More than 1 word in RXFIFO

6.3.4.6. SPI DMA CONTROL REGISTER

Offset: 0x14			Register Name: SPI_DMACTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:13	/	/	/
12	R/W	0	TF_EMP34_DMA TXFIFO3/4 Empty DMA Request Enable 0: Disable 1: Enable
11	R/W	0	TF_EMP14_DMA TXFIFO 1/4 Empty DMA Request Enable 0: Disable 1: Enable
10	R/W	0	TF_NF_DMA TXFIFO Not Full DMA Request Enable When enable, if more than one free room for burst, DMA request is asserted, else de-asserted. 0: Disable 1: Enable

Offset: 0x14			Register Name: SPI_DMACTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
9	R/W	0	TF_HE_DMA TXFIFO Half Empty DMA Request Enable 0: Disable 1: Enable
8	R/W	0	TF_EMP_DMA TXFIFO Empty DMA Request Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0	RF_FU34_DMA RXFIFO 3/4 Full DMA Request Enable This bit enables/disables the RXFIFO 3/4 Full DMA Request. 0: Disable 1: Enable
3	R/W	0	RF_FU14_DMA RXFIFO 1/4 Full DMA Request Enable This bit enables/disables the RXFIFO 1/4 Full DMA Request. 0: Disable 1: Enable
2	R/W	0	RF_FU_DMA RXFIFO Full DMA Request Enable This bit enables/disables the RXFIFO Half Full DMA Request. 0: Disable 1: Enable
1	R/W	0	RF_HF_DMA RXFIFO Half Full DMA Request Enable This bit enables/disables the RXFIFO Half Full DMA Request. 0: Disable 1: Enable
0	R/W	0	RF_RDY_DMA RXFIFO Ready Request Enable This bit enables/disables the RXFIFO Ready DMA Request when one or more than one words in RXFIFO 0: Disable

Offset: 0x14			Register Name: SPI_DMACTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			1: Enable

6.3.4.7. SPI WAIT CLOCK REGISTER

Offset: 0x18			Register Name: SPI_WAIT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
15:0	R/W	0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

6.3.4.8. SPI CLOCK CONTROL REGISTER

Offset: 0x1C			Register Name: SPI_CCTL Default Value: 0x0000_0002
Bit	**Read/Write**	**Default**	**Description**
31:13	/	/	/
12	R/W	0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0	CDR1 Clock Divide Rate 1 (Master Mode Only) This field selects the baud rate of the SPI_SCLK based on a division of the AHB_CLK. These bits allow SPI to synchronize with different external SPI devices. The max frequency is one quarter of AHB_CLK. The divide ratio is determined according to the following table using the equation: 2^(n+1). The

Offset: 0x1C			Register Name: SPI_CCTL Default Value: 0x0000_0002
Bit	**Read/Write**	**Default**	**Description**
			SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / 2^(n+1).
7:0	R/W	0x2	CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / (2*(n + 1)).

6.3.4.9. SPI BURST COUNTER REGISTER

Offset: 0x20			Register Name: SPI_BC Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	BC Burst Counter In master mode, this field specifies the total burst number when SMC is 1. 0: 0 burst 1: 1 burst … N: N bursts

6.3.4.10. SPI TRANSMIT COUNTER REGISTER

Offset: 0x24			Register Name: SPI_TC Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	WTC Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending

Offset: 0x24			Register Name: SPI_TC Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			dummy burst when SMC is 1. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

6.3.4.11. SPI FIFO STATUS REGISTER

Offset: 0x28			Register Name: SPI_FIFO_STA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:25	/	/	/
22:16	R	0x0	TF_CNT TXFIFO Counter These bits indicate the number of words in TXFIFO 0: 0 byte in TXFIFO 1: 1 byte in TXFIFO … … 63: 63 bytes in TXFIFO 64: 64 bytes in TXFIFO
15:7	/	/	/
6:0	R	0x0	RF_CNT RXFIFO Counter These bits indicate the number of words in RXFIFO 0: 0 byte in RXFIFO 1: 1 byte in RXFIFO … … 63: 63 bytes in RXFIFO 64: 64 bytes in RXFIFO

6.3.5. SPI Special Requirement

6.3.5.1. SPI PIN LIST

The direction of SPI pin is different in two work modes: Master Mode and Slave Mode.

Port Name	Width	Direction(M)	Direction(S)	Description
SPI_SCLK	1	OUT	IN	SPI Clock
SPI_MOSI	1	OUT	IN	SPI Master Output Slave Input Data Signal
SPI_MISO	1	IN	OUT	SPI Master Input Slave Output Data Signal
SPI_SS[3:0]	4	OUT	IN	SPI Chip Select Signal

Notes: SPI0 module has four chip select signals and SPI1 module has only one chip select signal for pin saving.

6.3.5.2. SPI MODULE CLOCK SOURCE AND FREQUENCY

The SPI module uses two clock source: AHB_CLK and SPI_CLK. The SPI_SCLK can in the range from 3Khz to 100 MHZ and AHB_CLK >= 2xSPI_SCLK.

Clock Name	Description	Requirement
AHB_CLK	AHB bus clock, as the clock source of SPI module	AHB_CLK >= 2xSPI_SCLK
SPI_CLK	SPI serial input clock	

6.4. UART

6.4.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

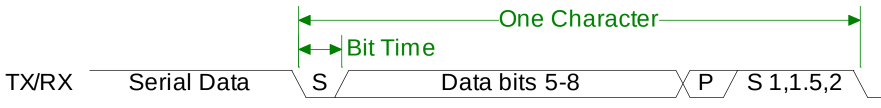
Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

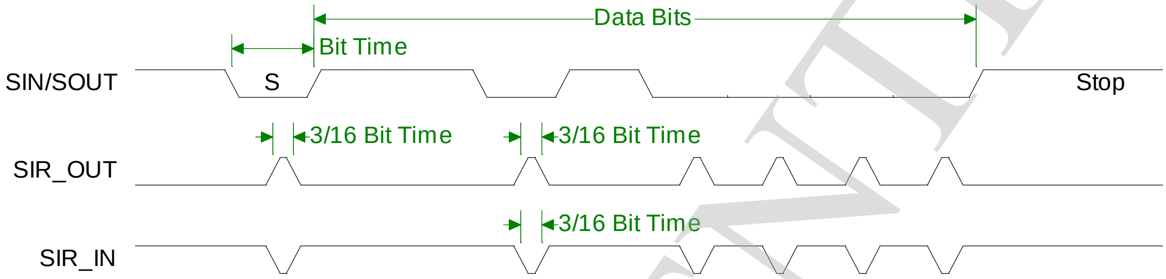
It features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports APB 16-bit bus width
- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Support IrDa 1.0 SIR
- Interrupt support for FIFOs, Status Change

6.4.2. UART Timing Diagram



UART Serial Data Format



Serial IrDA Data Format

6.4.3. UART Register List

There are 8 UART controllers. UART1 has full modem control signals, including RTS, CTS, DTR, DSR, DCD and RING signal. UART2/3 has two data flow control singals, including RTS and CTS. Other UART controller has only two data signals, including DIN and DOUT. All UART controllers can be configured as Serial IrDA.

Module Name	**Base Address**
UART0	0x01C28000
UART1	0x01C28400
UART2	0x01C28800
UART3	0x01C28C00
UART4	0x01C29000
UART5	0x01C29400
UART6	0x01C29800

Module Name	Base Address
UART7	0x01C29C00

Register Name	Offset	Description
UART_RBR	0x00	UART Receive Buffer Register
UART_THR	0x00	UART Transmit Holding Register
UART_DLL	0x00	UART Divisor Latch Low Register
UART_DLH	0x04	UART Divisor Latch High Register
UART_IER	0x04	UART Interrupt Enable Register
UART_IIR	0x08	UART Interrupt Identity Register
UART_FCR	0x08	UART FIFO Control Register
UART_LCR	0x0C	UART Line Control Register
UART_MCR	0x10	UART Modem Control Register
UART_LSR	0x14	UART Line Status Register
UART_MSR	0x18	UART Modem Status Register
UART_SCH	0x1C	UART Scratch Register
UART_USR	0x7C	UART Status Register
UART_TFL	0x80	UART Transmit FIFO Level
UART_RFL	0x84	UART_RFL
UART_HALT	0xA4	UART Halt TX Register

6.4.4. UART Register Description

6.4.4.1. UART RECEIVER BUFFER REGISTER

Offset: 0x00			Register Name: UART_RBR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/

Offset: 0x00			Register Name: UART_RBR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
7:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

6.4.4.2. UART TRANSMIT HOLDING REGISTER

Offset: 0x00			Register Name: UART_THR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

6.4.4.3. UART DIVISOR LATCH LOW REGISTER

Offset: 0x00			Register Name: UART_DLL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

6.4.4.4. UART DIVISOR LATCH HIGH REGISTER

Offset: 0x04			Register Name: UART_DLH Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8

Offset: 0x04			Register Name: UART_DLH Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

6.4.4.5. UART INTERRUPT ENABLE REGISTER

Offset: 0x04			Register Name: UART_IER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W		PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:4	/	/	/
3	R/W	0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable

Offset: 0x04			Register Name: UART_IER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

6.4.4.6. UART INTERRUPT IDENTITY REGISTER

Offset: 0x08			Register Name: UART_IIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types:

Offset: 0x08			Register Name: UART_IIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Second	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Third	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note	Reading the Modem status Register

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
			that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	
0111	Fifth	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

6.4.4.7. UART FIFO CONTROL REGISTER

Offset: 0x08			Register Name: UART_FCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO

Offset: 0x08			Register Name: UART_FCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			10: FIFO ¼ full 11: FIFO ½ full
3	W	0	DMAM DMA Mode 0: Mode 0 1: Mode 1
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

6.4.4.8. UART LINE CONTROL REGISTER

Offset: 0x0C			Register Name: UART_LCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial

Offset: 0x0C			Register Name: UART_LCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	/	/	/
4	R/W	0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). 0: Odd Parity 1: Even Parity
3	R/W	0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are

Offset: 0x0C			Register Name: UART_LCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

6.4.4.9. UART MODEM CONTROL REGISTER

Offset: 0x10			Register Name: UART_MCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6	R/W	0	SIRE SIR Mode Enable 0: IrDA SIR Mode disabled 1: IrDA SIR Mode enabled
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	/
3:2	/	/	/
1	R/W	0	RTS

Offset: 0x10			Register Name: UART_MCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n。」 0:dtr_n de-asserted (logic 1) 1:dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

6.4.4.10. UART LINE STATUS REGISTER

Offset: 0x14			Register Name: UART_LSR Default Value: 0x0000_0060
Bit	**Read/Write**	**Default**	**Description**

Offset: 0x14			Register Name: UART_LSR Default Value: 0x0000_0060
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to “1” whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to “1” whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic ‘0’ state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic ‘0’ for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs

Offset: 0x14			Register Name: UART_LSR Default Value: 0x0000_0060
Bit	**Read/Write**	**Default**	**Description**
			immediately and persists until the LSR is read.
3	R	0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	R	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.

Offset: 0x14			Register Name: UART_LSR Default Value: 0x0000_0060
Bit	**Read/Write**	**Default**	**Description**
1	R	0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

6.4.4.11. UART MODEM STATUS REGISTER

Offset: 0x18			Register Name: UART_MSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)

Offset: 0x18			Register Name: UART_MSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
6	R	0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	R	0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then

Offset: 0x18			Register Name: UART_MSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	R	0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset isremoved if the cts_n signal remains asserted.

6.4.4.12. UART SCRATCH REGISTER

Offset: 0x1C			Register Name: UART_SCH Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

6.4.4.13. UART STATUS REGISTER

Offset: 0x7C			Register Name: UART_USR Default Value: 0x0000_0006
Bit	**Read/Write**	**Default**	**Description**
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.

Offset: 0x7C			Register Name: UART_USR Default Value: 0x0000_0006
Bit	**Read/Write**	**Default**	**Description**
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

6.4.4.14. UART TRANSMIT FIFO LEVEL REGISTER

Offset: 0x80			Register Name: UART_TFL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:0	R	0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

6.4.4.15. UART RECEIVE FIFO LEVEL REGISTER

Offset: 0x84			Register Name: UART_RFL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:0	R	0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

6.4.4.16. UART HALT TX REGISTER

Offset: 0xA4			Register Name: UART_HALT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5	R/W	0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/W	0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0	/

6.4.5. UART Special Requirement

6.4.5.1. UART PIN LIST

Port Name	Width	Direction	Description

Port Name	Width	Direction	Description
UART0_TX	1	OUT	UART Serial Bit output
UART0_RX	1	IN	UART Serial Bit input
UART1_TX	1	OUT	UART Serial Bit output
UART1_RX	1	IN	UART Serial Bit input
UART1_RTS		OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART1_CTS		IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART1_DTR		OUT	UART Data Terminal Ready This active low output signal informs Modem that the UART is ready to establish a communication link
UART1_DSR		IN	UART Data Set Ready This active low signal is an input indicating when Modem is ready to set up a link with the UART0
UART1_DCD		IN	UART Data Carrier Detect This active low signal is an input indicating when Modem has detected a carrier
UART1_RING		IN	UART Ring Indicator This active low signal is an input showing when Modem has sensed a ring signal on the telephone line
UART2_TX	1	OUT	UART Serial Bit output
UART2_RX	1	IN	UART Serial Bit input
UART2_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART2_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART3_TX	1	OUT	UART Serial Bit output
UART3_RX	1	IN	UART Serial Bit input
UART3_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART3_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data

Port Name	Width	Direction	Description
UART4_TX	1	OUT	UART Serial Bit output
UART4_RX	1	IN	UART Serial Bit input
UART5_TX	1	OUT	UART Serial Bit output
UART5_RX	1	IN	UART Serial Bit input
UART6_TX	1	OUT	UART Serial Bit output
UART6_RX	1	IN	UART Serial Bit input
UART7_TX	1	OUT	UART Serial Bit output
UART7_RX	1	IN	UART Serial Bit input

IRDA INVERTED SIGNALS

When the UART is working in IrDA mode (MCR[6]='1'), if HALT[4] is set to '1', the signal is inverted before transferring to pin SOUT and if HALT[5] is set to '1', the signal is inverted after receiving from pin SIN

6.5. PS2

6.5.1. Overview

The PS2 is a Dual-Role controller that supports both device and host functions.

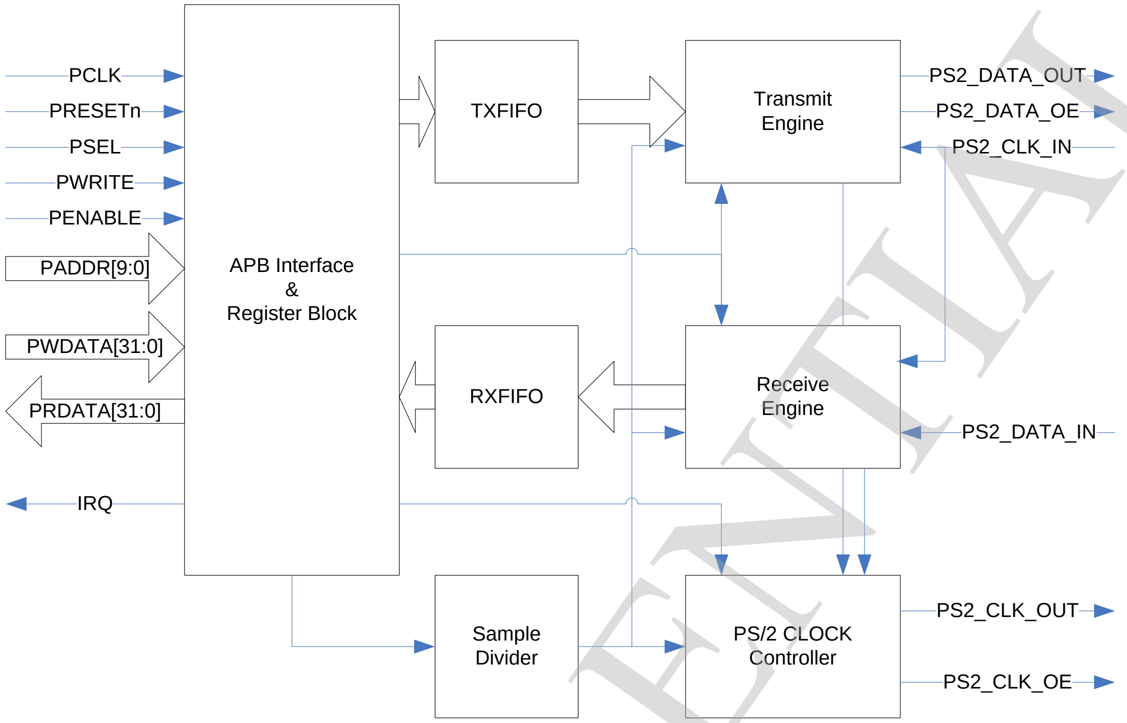
It is fully compliant with IBM PS2 in Personal Computer. It can be configured as a Host to connect PS2 Keyboard or PS2 Mouse, or as a Device to connect computers.

The PS2 module can be integrated with industry-standard AMBA Peripheral Bus (APB) for communication with other system modules, such as ARM CPU, and System Memory.

It features:

- Comply with the AMBA Specification (Rev 2.0) for easy integration into SOC implementation
- Compliant with IBM PS2 and AT-Compatible Keyboard and Mouse Interface
- Dual Role controller, either a PS2 Host or a PS2 Device
- 4-byte TXFIFO and 4-byte RXFIFO for data buffering
- Odd parity generation and checking
- Register bits for override of keyboard clock and data lines
- Internal clock divider for simple clock interface

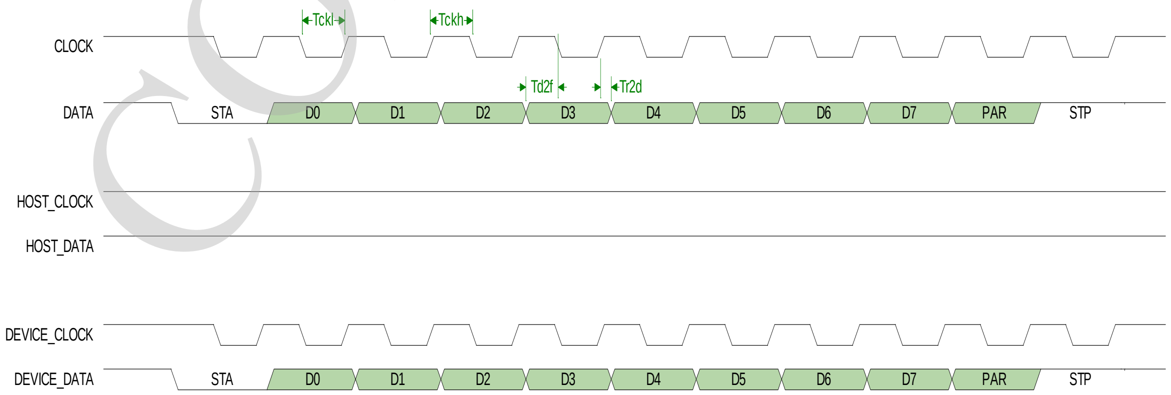
6.5.2. PS2 Block Diagram



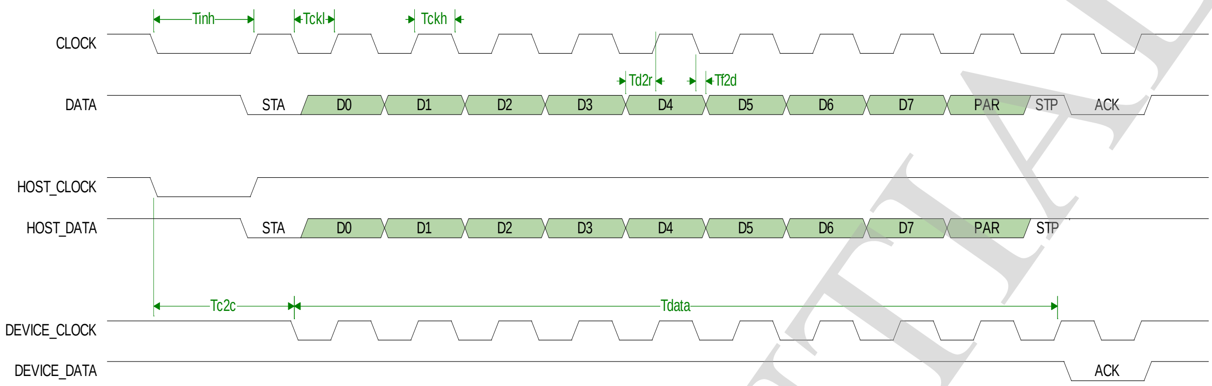
6.5.3. PS2 Timing Diagram

The Data and Clock lines of PS2 Bus are both open-collector with pull-up resistors to power, and so, Data and Clock signals on PS2 Bus are both wire-and by corresponding signal of Host and Device. Data is transferred after start bit, starting with the least significant bit(LSB). These are followed by the parity bit, followed by one stop bit. If data is transferred from master to device, there is an additional acknowledge bit(ACK) sent by device, following the stop bit.

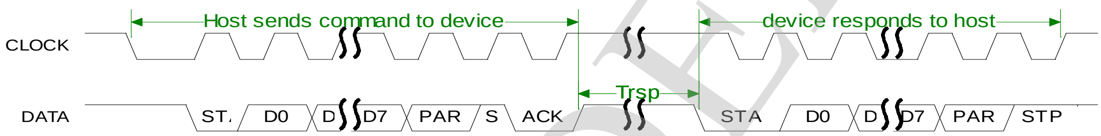
Timing for Device Transmit Data and Master Receive Data:



Timing for Master Transmit Data and Device Receive Data:



Timing for Master sending command then Device sending response



Device drive and sample data at rising edge of CLOCK. Master drive and sample data at falling edge of CLOCK.

Name	Comment	Min.	Typical	Max.
Tckl	Clock LOW time	30us	40us	50us
Tckh	Clock HIGH time	30us	40us	50us
Tinh	Time for Host inhibit clock for send data request	100us	-	-
Td2f	Data change to clock falling edge time during device to host transfer	5us	-	Tckh-5us
Tr2d	Clock rising edge to data change time during device to host transfer	5us	-	Tckh-5us
Td2r	Data change to clock rising edge time during host to device transfer	5us	-	Tckl-5us
Tf2d	Clock falling edge to data change time during host to device transfer	5us	-	Tckl-5us
Tc2c	Host pull low Clock to Device drive Clock	-	-	15ms
Tdata	Time for packet to send	-	-	2ms

Name	Comment	Min.	Typical	Max.
Trsp	Time for device responding to the host command	-	-	20ms

6.5.4. PS2 Register List

Module Name	Base Address
PS2-0	0x01C2A000
PS2-1	0x01C2A400

Register Name	Offset	Description
PS2_GCTL	0x00	PS2 Module Global Control Register
PS2_DATA	0x04	PS2 Module Data Register
PS2_LCTL	0x08	PS2 Module Line Control Register
PS2_LSTS	0x0C	PS2 Module Line Status Register
PS2_FCTL	0x10	PS2 Module FIFO Control Register
PS2_FSTS	0x14	PS2 Module FIFO Status Register
PS2_CKDR	0x18	PS2 Module Clock Divider Register

6.5.5. PS2 Register Description

6.5.5.1. PS2 GLOBAL CONTROL REGISTER

Offset: 0x0000			Register Name: PS2_GCTL Default Value: 0x0000_0002
Bit	**Read/Write**	**Default**	**Description**
31:5	/	/	/
4	R	0	INT_FLAG Interrupt Flag The interrupt flag is set when any bit in FIFO Status and the corresponding enable bit in FIFO Control are set at the same time. This interrupt flag is also set when error flag bit in line status register **(**PS2_LSTS**)**is set at the same time.

Offset: 0x0000			Register Name: PS2_GCTL Default Value: 0x0000_0002
Bit	**Read/Write**	**Default**	**Description**
			Note: This bit is just a status flag, it can not be cleared directly, it can be cleared by clearing the status bits in FIFO Status Register.
3	R/W	0	INT_EN Interrupt Enable 0 – the interrupt signal is always low 1 – the interrupt signal will be high when INT_FLAG is set
2	R/W	0	SOFT_RST Soft Reset Setting this bit will reset transmitter and receiver of PS2 Module, and the status of transmitter and receiver will revert to the default state, but not affect any control bits in register, and data in TXFIFO/RXFIFO. This bit will be cleared by hardware after reset is completed.
1	R/W	1	FUNC_SEL Master/Device Function Select 1 – Master Function, connect to PS2 Keyboard or Mouse 0 – Device Function, connect to Computer
0	R/W	0	BUS_EN PS2 Bus Enable 0 – Ignore PS2 Bus Input 1 – Response to PS2 Bus Input

6.5.5.2. PS2 DATA REGISTER

Offset: 0x0004			Register Name: PS2_DATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	PS2_DATA When write, data will be write into TXFIFO, and will be transmit on to the PS2 Bus. When read, data is read out from RXFIFO, and it is received from PS2 Bus.

Offset: 0x0004			Register Name: PS2_DATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			Note: (1) After TXFIFO is full, writing does not affect anything except the overflow flag of TXFIFO in FIFO Status Register. (2) After RXFIFO is empty, reading has no effect on anything except the underflow flag of RXFIFO in FIFO Status Register.

6.5.5.3. PS2 LINE CONTROL REGISTER

Offset: 0x0008			Register Name: PS2_LCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:19	/	/	/
18	R/W	0	NO_ACK ACK Control 0 – In Host function mode, must check ACK after transmitted data; In Device function mode, must send ACK after received data from Host. 1 – In Host function mode, don't check ACK after transmitted data; In Device function mode, don't send ACK after received data from Host.
17	R/W	0	FORCE_DATA Force Data to LOW 0 – Data Line works in Normal Mode 1 – Data Line is forced to LOW
16	R/W	0	FORCE_CLK Force Clock to LOW 0 – Clock Line works in Normal Mode 1 – Clock Line is forced to LOW
15:9	/	/	/
8	R/W	0	TXDTO_IEN TX Data Timeout Interrupt Enable
7:4	/	/	/
3	R/W	0	STOP_IEN Stop Error Interrupt Enable
2	R/W	0	ACKERR_IEN

Offset: 0x0008			Register Name: PS2_LCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			Acknowledge Error Interrupt Enable
1	R/W	0	PARERR_IEN Parity Error Interrupt Enable
0	R/W	0	RXDTO_IEN RX Data Timeout Interrupt Enable

6.5.5.4. PS2 LINE STATUS REGISTER

Offset: 0x000C			Register Name: PS2_LSTS Default Value: 0x0003_0000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19	R	0	TX_BUSY Transmit Busy 0 – PS2 Module Transmit Engine is Idle. 1 – PS2 Module is currently sending data. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
18	R	0	RX_BUSY Receive Busy 0 –PS2 Module Receive Engine is Idle. 1 –PS2 Module is currently receiving data. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
17	R	1	LS_DATA Line State of DATA. Invalid before BUS_EN set.
16	R	1	LS_CLK Line State of CLOCK. Invalid before BUS_EN set.
15:9	/	/	/
8	R/W	0	TX_DTO Transmit Data Timeout Timers include:

Offset: 0x000C			Register Name: PS2_LSTS Default Value: 0x0003_0000
Bit	**Read/Write**	**Default**	**Description**
			Tc2c<15ms (Host pull low Clock to Device drive Clock) Tdata<2ms (Time for packet to send) Tckl+Tckh<100us(one cycle time, as host) *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
7:4	/	/	/
3	R/W	0	STOP_ERR Stop Bit Error 0 –No Error 1 –Stop Error *This bit can be cleared by writing '1', writing '0' has no effect.*
2	R/W	0	ACK_ERR Acknowledge Error 0 – ACK is received after data transmitted. 1 – ACK is not received after data transmitted. *Note: 1) Only for Master Function; 2) This bit can be cleared by writing '1', writing '0' has no effect.*
1	R/W	0	PAR_ERR Parity Error 0 – No Error 1 – Parity Error *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
0	R/W	0	RX_DTO Receive Data Timeout Timers include: Trsp<20ms(time from the host releases the Clock line to device sends corresponding response) Tckl+Tckh<100us(one cycle time, as host) Note: This bit can be cleared by writing '1', writing '0' has no effect.

6.5.5.5. PS2 FIFO CONTROL REGISTER

Offset: 0x0010			Register Name: PS2_FCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
17	R/W	0	TXFIFO_RST TXFIFO Reset After this bit is set, data in TXFIFO is flushed, and the pointer of TXFIFO is reset. *Note: This bit is cleared automatically after TXFIFO is reset, and writing '0' has no effect.*
16	R/W	0	RXFIFO_RST RXFIFO Reset After this bit is set, data in RXFIFO is flushed, and the pointer of RXFIFO is reset. *Note: This bit is cleared automatically after RXFIFO is reset, and writing '0' has no effect.*
15:11	/	/	/
10	R/W	0	TXUF_IEN TXFIFO Underflow Interrupt Enable
9	R/W	0	TXOF_IEN TXFIFO Overflow Interrupt Enable
8	R/W	0	TXRDY_IEN TXFIFO Ready Interrupt Enable
7:3	/	/	/
2	R/W	0	RXUF_IEN RXFIFO Underflow Interrupt Enable
1	R/W	0	RXOF_IEN RXFIFO Overflow Interrupt Enable
0	R/W	0	RXRDY_IEN RXFIFO Ready Interrupt Enable

6.5.5.6. PS2 FIFO STATUS REGISTER

Offset: 0x0014			Register Name: PS2_FSTS Default Value: 0x0000_0100
Bit	**Read/Write**	**Default**	**Description**

Offset: 0x0014			Register Name: PS2_FSTS Default Value: 0x0000_0100
Bit	**Read/Write**	**Default**	**Description**
31:23	/	/	/
22:20	R	0	TX_LEVEL TXFIFO Level The number of 8-bit data, which will be transmitted on to PS2 Bus, in the TXFIFO. The value must be in the range 0-4.
19	/	/	/
18:16	R	0	RX_LEVEL RXFIFO Level The number of 8-bit data, which is received from PS2 bus, in the RXFIFO. The value must be in the range 0-4.
15:11	/	/	/
10	R/W	0	TX_UF TXFIFO Underflow When this bit is set, TXFIFO is underflow, and it means that the TXFIFO is read by transmit engine after empty. This bit is just a flag of illegal operation, which should not affect any state of TXFIFO. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
9	R/W	0	TX_OF TXFIFO Overflow When this bit is set, TXFIFO is overflow, and it means that the TXFIFO is wrote by CPU after TXFIFO is full. This bit is just a flag of illegal operation, which should not affect any state of TXFIFO. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
8	R/W	1	TX_RDY Transmit Ready 0 – TXFIFO is full 1 – TXFIFO is not full. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
7:3	/	/	/
2	R/W	0	RX_UF RXFIFO Underflow When this bit is set, RXFIFO is underflow, and it means that

Offset: 0x0014			Register Name: PS2_FSTS Default Value: 0x0000_0100
Bit	**Read/Write**	**Default**	**Description**
			the RXFIFO is read by CPU after empty. This bit is just a flag of illegal operation, which should not affect any state of RXFIFO. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
1	R/W	0	RX_OF RXFIFO Overflow When this bit is set, RXFIFO is overflow, and it means that the RXFIFO is wrote by receive engine after RXFIFO is full. This bit is just a flag of illegal operation, which should not affect any state of RXFIFO. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*
0	R/W	0	RX_RDY Receive Ready 0 – RXFIFO is empty 1 – RXFIFO is not empty, there are at least one byte data, which is received from PS2 bus, in the RXFIFO. *Note: This bit can be cleared by writing '1', writing '0' has no effect.*

6.5.5.7. PS2 CLOCK DIVIDER REGISTER

Offset: 0x0018			Register Name: PS2_CKDR Default Value: 0x0000_2F4F
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
15:8	R/W	0x2F	SCLK_DIV Sample Clock Divider Factor (SCDF) Sample Clock is a 1MHz clock for internal timing control. SCDF = APB_CLK/SAMPLE_CLK – 1 Frequency of sample clock is constant, and so, frequency of APB_CLK must be in the range 1-256MHz.
7	/	/	/
6:0	R/W	0x4F	CLK_DIV

Offset: 0x0018			Register Name: PS2_CKDR Default Value: 0x0000_2F4F
Bit	**Read/Write**	**Default**	**Description**
			PS2 Clock Divider Factor (PCDF) PCDF = SAMPLE_CLK /PS2_CLK – 1 = 1MHz/PS2_CLK - 1 The frequency of PS2_CLK must be in the range 10-16.7KHz. *Note: This factor is used in device mode only.*

6.5.6. PS2 Special Requirements

6.5.6.1. PS2 INTERFACE PIN LIST

Port Name	Width	Direction	Description
PS2_CLK	1	IN/OUT	PS2 clock signal
PS2_DATA	1	IN/OUT	PS2 data signal

6.5.6.2. PS2 CLOCK REQUIREMENT

Clock Name	Description	Requirement
apb_clk	APB bus clock	>=1MHz

6.6. IR

6.6.1. Overview

The CIR (Consumer IR) interface is used for remote control through infra-red light.

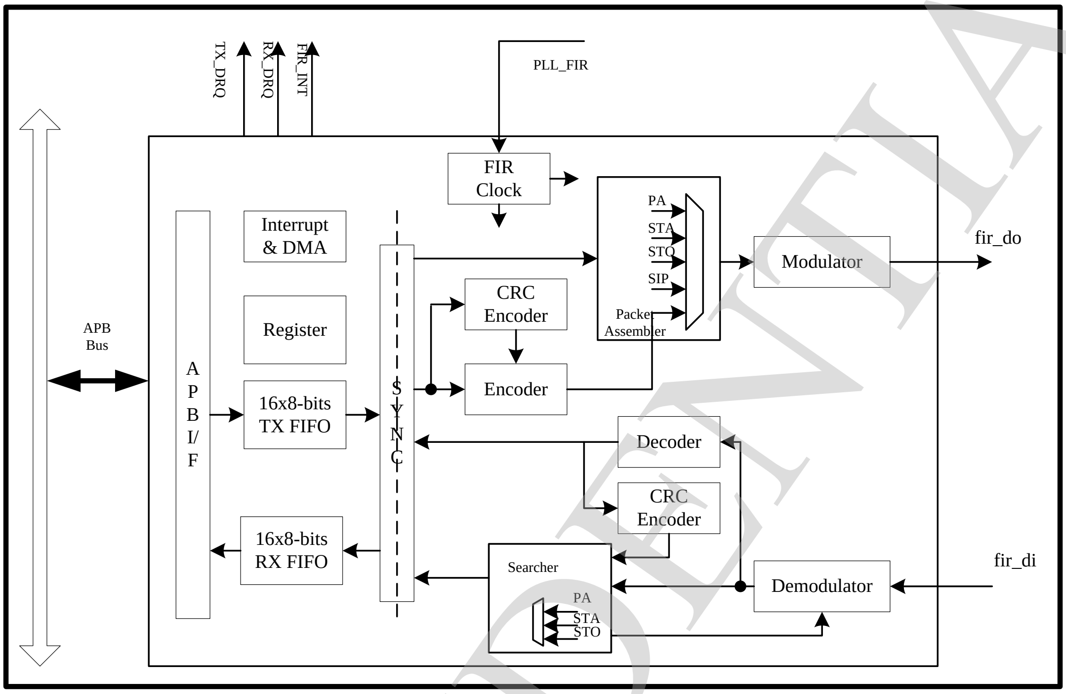
The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as ‘1’ while the low level is represented as ‘0’. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

Since there is always some noise in the air, a threshold can be set to filter the noise to reduce system loading and improve system stability.

The CIR interface features:
- Full physical layer implementation
- Support CIR for remote control or wireless keyboard
- Support dual 64x8bits FIFO for data buffer
- Programmable FIFO thresholds
- Support Interrupt and DMA

6.6.2. IR Block Diagram

The IR block diagram is shown below:



6.6.3. IR Register List

Module Name	Base Address
IR0	0x01C21800
IR1	0x01C21C00

Register Name	Offset	Description
IR_CTL	0x00	IR Control Register
IR_TXCTL	0x04	IR Transmitter Configure Register

Register Name	Offset	Description
IR_TXADR	0x08	IR Transmitter Address Register
IR_TXCNT	0x0C	IR Transmitter Counter Register
IR_RXCTL	0x10	IR Receiver Configure Register
IR_RXADR	0x14	IR Receiver Address Register
IR_RXCNT	0x18	IR Receiver Counter Register
IR_TXFIFO	0x1C	IR Transmitter FIFO Register
IR_RXFIFO	0x20	IR Receiver FIFO Register
IR_TXINT	0x24	IR Transmitter Interrupt Control Register
IR_TXSTA	0x28	IR Transmitter Status Register
IR_RXINT	0x2C	IR Receiver Interrupt Control Register
IR_RXSTA	0x30	IR Receiver Status Register
IR_CIR	0x34	CIR Configure Register

6.6.4. IR Register Description

6.6.4.1. IR CONTROL REGISTER

Offset: 0x00			Register Name: IR_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/
8	R/W	0	CGPO General Program Output (GPO) Control in CIR mode for TX Pin 0: Low level 1: High level
7:6	/	/	/
5:4	R/W	0	MD Irda Mode 00: 0.576 Mbit/s MIR mode 01: 1.152 Mbit/s MIR mode 10: 4.0 Mbit/s FIR mode

Offset: 0x00			Register Name: IR_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			11: CIR mode for Remote control or wireless keyboard
3	R/W	0	/
2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

6.6.4.2. IR TRANSMITTER CONFIGURE REGISTER

Offset: 0x04			Register Name: IR_TXCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5	R/W	0	PCF Packet Complete by FIFO This bit determines how a packet is completed if a TX FIFO underrun event occurs. Do not write software intentionally to cause underrun events. However, if due to erroneous conditions, the value of this bit selects between two recovery modes. Set the PCF based on system and upper layer IrDA protocol requirements. 0: Send CRC and STO fields Send CRC16 and STO for MIR or CRC32 and STO for FIR 1: Send packet abort symbol Send 7’b111,1111 for MIR or 8’b0000,0000 for FIR

Offset: 0x04			Register Name: IR_TXCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
4	/	/	/
3	R/W	0	SIP Transmit SIP Writing '1' to this bit produces a "Serial Infrared Interaction Pulse" transmission. Writing a '0' to this bit is ignored. This bit is always read as "0". If this bit is set while in the middle of the transfer, the packet will be ignored by IRDA controller. Don't Set SIP bit in the middle of transfer. A SIP is defined as a 1.6us optical pulse of the transmitter followed by a 7.1us off time of the transmitter. It simulates a start pulse, causing the potentially interfering system to listen for at least 500 ms.
2	R/W	1	TPPI Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
1:0	/	/	/

6.6.4.3. IR TRANSMITTER ADDRESS REGISTER

Offset: 0x08			Register Name: IR_TXADR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/
8	R/W	0	HAG Hardware Address Generator. When this bit is set, the content of the TPA bits is transmitted as a packet address. When the bit is cleared, the packet address is read from TX FIFO. 0: Read packet address from TX FIFO 1: Use TPA bits as packet address
7:0	R/W	0	TPA Transmit Packet Address This field contains the 8-bit Transmit Packet Address. If the HAG bit is cleared, the TPA bits have no effect.

6.6.4.4. IR TRANSMITTER COUNTER REGISTER

Offset: 0x0C			Register Name: IR_TXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:11	/	/	/
10:0	R/W	0	TPL Transmit Packet Length This field contains the length of the address, control and data. The length are (N+1) bytes. 11’d0: 1 bytes 11’d1: 2 bytes 11’d2: 3 bytes … 11’d2046: 2047 bytes 11’d2047: 2048 bytes

6.6.4.5. IR RECEIVER CONFIGURE REGISTER

Offset: 0x10			Register Name: IR_RXCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
3	R/W	0	RPA Receiver Packet Abort bit. Determines behavior of the RX FIFO upon detection of an illegal symbol. When an illegal symbol is detected, the DDE or CRCE bit in the receiver status register is set. If the RPA bit is set, the RX FIFO pointers are cleared and the receiver starts to search for the PA or STA fields for FIR and MIR mode, respectively. If RPA is cleared, the receiver continues to write to the RX FIFO. 0: Does not clear the RX FIFO upon detection of an illegal symbol 1: Clears the RX FIFO upon detection of illegal symbol

Offset: 0x10			Register Name: IR_RXCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
2	R/W	1	RPPI Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

6.6.4.6. IR RECEIVER ADDRESS REGISTER

Offset: 0x14			Register Name: IR_RXADR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/
8	R/W	0	RAM Receiver Address Match 0: Does not need match address (RA). When an new packet is received, the address, control and data fields are filled into RX FIFO. 1: Should match packet address to RA bits when an new packet is received. If address matched, the control and data fields are filled into RX FIFO excluding the address field. The value of this bit can be changed when the RXEN bit is cleared.
7:0	R/W	0	RA Receiver Address The value of this bit can be changed when the RXEN bit is cleared.

6.6.4.7. IR RECEIVER COUNTER REGISTER

Offset: 0x18			Register Name: IR_RXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

Offset: 0x18			Register Name: IR_RXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:0	R	0	RPL Receiver Packet Length This field contains the length of the address, control and data. The length are (N+1) bytes. 0: no bytes received N: N bytes received It can automatically clear by Irda Controller when new packet is found.

6.6.4.8. IR TRANSMITTER FIFO REGISTER

Offset: 0x1C			Register Name: IR_TXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	W	0	TX_DATA Transmitter Byte FIFO

6.6.4.9. IR RECEIVER FIFO REGISTER

Offset: 0x20			Register Name: IR_RXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R	0	RX_DATA Receiver Byte FIFO

6.6.4.10. IR TRANSMITTER INTERRUPT CONTROL REGISTER

Offset: 0x24			Register Name: IR_TXINT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:8	R/W	0	TEL TX FIFO Empty Level for interrupt and DMA request TRIGGER_LEVEL = TEL + 1
7:6	/	/	/
5	R/W	0	DRQ_EN TX FIFO Empty DMA Enable 0: Disable 1: Enable When set to '1', the Transmitter FIFO DRQ is asserted if reaching TEL. The DRQ is de-asserted when condition fails or specified number data has been sent from host CPU.
4	R/W	0	TEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable When set to '1', the Transmitter FIFO interrupt is asserted if reaching TEL. The interrupt is de-asserted when condition fails or specified number data has been sent from host CPU.
3	R/W	0	TCI_EN Transmit (including the CRC and STO fields) Complete Interrupt Enable 0: Disable 1: Enable
2	R/W	0	SIPEI_EN Transmitter SIP End Interrupt Enable 0: Disable 1: Enable
1	R/W	0	TPEI_EN Transmitter Packet (the address, control and data fields) End Interrupt Enable 0: Disable 1: Enable
0	R/W	0	TUI_EN

Offset: 0x24			Register Name: IR_TXINT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			Transmitter FIFO Under run Interrupt Enable 0: Disable 1: Enable

6.6.4.11. IR TRANSMITTER STATUS REGISTER

Offset: 0x28			Register Name: IR_TXSTA Default Value: 0x0000_1000
Bit	**Read/Write**	**Default**	**Description**
31:13	/	/	/
12:8	R	0x10	TA TX FIFO Available Room Counter 0: TX FIFO full 1: TX FIFO 1 byte room for new data 2: TX FIFO 2 byte room for new data … 15: TX FIFO 15 byte room for new data 16: TX FIFO 16 byte room for new data (full empty) Others: Reserved
7:5	/	/	/
4	R/W	1	TE TX FIFO Empty 0: TX FIFO not empty 1: TX FIFO empty by its level This bit is cleared by writing a ‘1’.
3	R/W	0	TC Transmit (including the CRC and STO fields) Complete 0: Transmission not completed 1: Transmission completed This bit is cleared by writing a ‘1’.
2	R/W	0	SIPE Transmitter SIP End

Offset: 0x28			Register Name: IR_TXSTA Default Value: 0x0000_1000
Bit	**Read/Write**	**Default**	**Description**
			0: Transmission of SIP not completed 1: Transmission of SIP completed This bit is cleared by writing a '1'.
1	R/W	0	TPE Transmitter Packet End 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed This bit is cleared by writing a '1'.
0	R/W	0	TU Transmitter FIFO Under Run 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a '1'.

6.6.4.12. IR RECEIVER INTERRUPT CONTROL REGISTER

Offset: 0x2C			Register Name: IR_RXINT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:8	R/W	0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
7:6	/	/	/
5	R/W	0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0	RAI_EN

Offset: 0x2C			Register Name: IR_RXINT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to ‘1’, the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3	R/W	0	CRCI_EN Receiver CRC Error Interrupt Enable 0: Disable 1: Enable
2	R/W	0	RISI_EN Receiver Illegal Symbol Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

6.6.4.13. IR RECEIVER STATUS REGISTER

Offset: 0x30			Register Name: IR_RXSTA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:13	/	/	/
12:8	R	0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO

Offset: 0x30			Register Name: IR_RXSTA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			… 16: 16 byte available data in RX FIFO
7:5	/	/	/
4	R/W	0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a '1'.
3	R/W	0	CRC Receiver CRC Error Flag 0: No CRC failure 1: CRC failure This bit is cleared by writing a '1'.
2	R/W	0	RIS Receiver Illegal Symbol Flag 0: No illegal symbols in address, control, data or CRC field 1: Illegal symbol in address, control, data or CRC field This bit is cleared by writing a '1'.
1	R/W	0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7'b0000,000 and 8'b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a '1'.
0	R/W	0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a '1'.

6.6.4.14. CIR CONFIGURE REGISTER

<table>
<tr><td colspan="3">Offset: 0x34</td><td>Register Name: IR_CIR
Default Value: 0x0000_1828</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td>31:25</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>24</td><td>R/W</td><td>0x0</td><td>SCS2
Bit2 of Sample Clock Select for CIR
This bit is defined by SCS bits below.</td></tr>
<tr><td>15:8</td><td>R/W</td><td>0x18</td><td>ITHR
Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enable, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xa</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0: all samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0</td><td>SCS
Sample Clock Select for CIR<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ir_clk/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ir_clk/128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ir_clk/256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ir_clk/512</td></tr>
</table></td></tr>
</table>

Offset: 0x34			Register Name: IR_CIR Default Value: 0x0000_1828
Bit	**Read/Write**	**Default**	**Description**
			<table><tr><td>1</td><td>0</td><td>0</td><td>ir_clk</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr></table>

6.7. USB OTG

6.7.1. Overview

The USB OTG is a Dual-Role Device (DRD) controller, which supports both device and host functions and is full compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a. It can also be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification.

It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode.

It features:

- Comply with USB 2.0 Specification
- Support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) in host mode and support high-Speed (HS, 480-Mbps), full-Speed (FS, 12-Mbps) in Device mode
- 64-Byte endpoint 0 for control transfer (Endpoint0)
- Support up to 5 user-configurable Endpoints for Bulk , Isochronous, Control and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)

6.7.2. USB OTG Timing Diagram

Please refer USB2.0 Specification and its On-The-Go Supplement to the USB 2.0 Specification.

6.8. USB Host

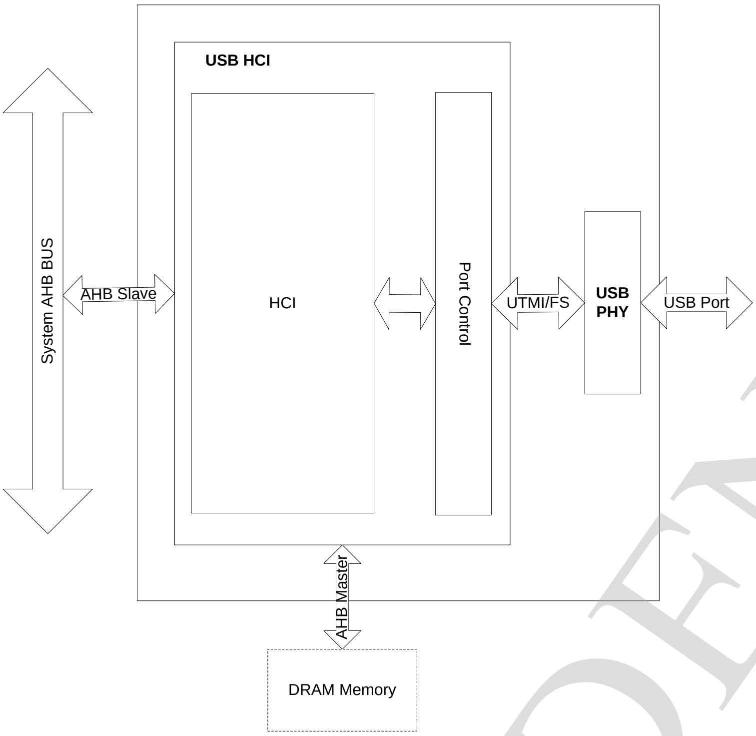
6.8.1. Overview

USB Host controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host controller, as well as full and low speed through one or more integrated OHCI host controllers.

The USB host controller features:

- Support industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports bus.
- Support 32-bit Little Endian AMBA AHB Slave bus for register access
- Support 32-bit Little Endian AMBA AHB Master bus for memory access.
- Include an internal DMA Controller for data transfer with memory.
- Comply with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) device
- Support the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- Support only 1 USB Root Port shared between EHCI and OHCI
- The USB HOST system contains two HCI controllers. The HCI controllers are composed of an EHCI controller and an OHCI companinon controller.

6.8.2. USB Host Block Diagram



6.8.3. USB Host Timing Diagram

Please refer USB2.0 Specification and EHCI Specification V1.0.

6.8.4. USB Host Register List

Module Name	Base Address
USB_HCI0	0x01C14000
USB_HCI1	0x01C1C000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x000	EHCI Capability register Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x00c	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01c	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register

6.8.5. EHCI Register Description

6.8.5.1. EHCI IDENTIFICATION REGISTER

Offset:0x00			**Register Name: CAPLENGTH** **Default Value: Implementation Dependent**
Bit	**Read/Write**	**Default**	**Description**
7:0	R	0x10	**CAPLENGTH** The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

6.8.5.2. EHCI HOST INTERFACE VERSION NUMBER REGISTER

Offset: 0x02			Register Name: HCIVERSION Default Value:0x0100
Bit	**Read/Write**	**Default**	**Description**
15:0	R	0x0100	**HCIVERSION** This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

6.8.5.3. EHCI HOST CONTROL STRUCTURAL PARAMETER REGISTER

Offset: 0x04			Register Name: HCSPARAMS Default Value: Implementation Dependent
Bit	**Read/Write**	**Default**	**Description**
31:24	/	0	**Reserved** These bits are reserved and should be set to zero.
23:20	R	0	**/**
19:16	/	0	**Reserved.** These bits are reserved and should be set to zero.
15:12	R	0	**N_CC** **Number of Companion Controller (N_CC)** This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be ‘0’.
11:8	R	0	**N_PCC** **Number of Port per Companion Controller(N_PCC)** This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with ‘0’.
7	R	0	**PRR** **Port Routing Rules** This field indicates the method used by this implementation for

<table>
<tr><td colspan="3">Offset: 0x04</td><td>Register Name: HCSPARAMS
Default Value: Implementation Dependent</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>how all ports are mapped to companion controllers. The value of this field has the following interpretation:
<table>
<tr><td>Value</td><td>Meaning</td></tr>
<tr><td>0</td><td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td></tr>
<tr><td>1</td><td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td></tr>
</table></td></tr>
<tr><td>6:4</td><td>/</td><td>0</td><td>Reserved.
These bits are reserved and should be set to zero.</td></tr>
<tr><td>3:0</td><td>R</td><td>1</td><td>N_PORTS
This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f.
This field is always 1.</td></tr>
</table>

6.8.5.4. EHCI HOST CONTROL CAPABILITY PARAMETER REGISTER

<table>
<tr><td colspan="3">Offset: 0x08</td><td>Register Name: HCCPARAMS
Default Value: Implementation Dependent</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td>31:16</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>15:18</td><td>R</td><td>0</td><td>EECP
EHCI Extended Capabilities Pointer (EECP)
This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device.
The value of this field is always ‘00b’.</td></tr>
</table>

Offset: 0x08			Register Name: HCCPARAMS Default Value: Implementation Dependent
Bit	**Read/Write**	**Default**	**Description**
7:4	R		**IST** **Isochronous Scheduling Threshold** This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	R	0	**Reserved** These bits are reserved and should be set to zero.
2	R		**ASPC** **Asynchronous Schedule Park Capability** If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R		**PFLF** **Programmable Frame List Flag** If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.
0	R	0	**Reserved** These bits are reserved for future use and should return a value of zero when read.

6.8.5.5. EHCI COMPANION PORT ROUTE DESCRIPTION

Offset: 0x0C			Register Name: HCSP-PORTROUTE Default Value: UNDEFINED
Bit	**Read/Write**	**Default**	**Description**
31:0	R		**HCSP-PORTROUTE** This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

6.8.5.6. EHCI USB COMMAND REGISTER

Offset: 0x10			Register Name: USBCMD Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)
Bit	**Read/Write**	**Default**	**Description**
31:24	/	0	**Reserved** These bits are reserved and should be set to zero.
23:16	R/W	0x08	**ITC** **Interrupt Threshold Control** The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below: Value / Minimum Interrupt Interval 0x00 / Reserved 0x01 / 1 micro-frame 0x02 / 2 micro-frame

<table>
<tr><td colspan="3">Offset: 0x10</td><td>Register Name: USBCMD
Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td><table>
<tr><td>0x04</td><td>4 micro-frame</td></tr>
<tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr>
<tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr>
<tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr>
<tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr>
</table>
Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>11</td><td>R/W or R</td><td>0</td><td>ASPME
Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>9:8</td><td>R/W or R</td><td>0</td><td>ASPMC
Asynchronous Schedule Park Mode Count(OPTIONAL)
Asynchronous Park Capability bit in the HCCPARAMS register is a one,
Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.
Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>LHCR
Light Host Controller Reset(OPTIONAL)</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x10</td><td>Register Name: USBCMD
Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>This control bit is not required.
If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships).
A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0</td><td>IAAD
Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0</td><td>ASE
Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>
The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0</td><td>PSE
Periodic Schedule Enable</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x10</td><td>Register Name: USBCMD
Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:
<table>
<tr><td>Bit Value</td><td>Meaning</td></tr>
<tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr>
<tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr>
</table>
The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W or R</td><td>0</td><td>FLS
Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index
Register should be used for the Frame List Current index. Values mean:
<table>
<tr><td>Bits</td><td>Meaning</td></tr>
<tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr>
<tr><td>01b</td><td>512 elements(2048byts)</td></tr>
<tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr>
<tr><td>11b</td><td>reserved</td></tr>
</table>
The default value is ‘00b’.</td></tr>
<tr><td>1</td><td>R/W</td><td>0</td><td>HCR
Host Controller Reset
This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.
When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of</td></tr>
</table>

Offset: 0x10			Register Name: USBCMD Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)
Bit	**Read/Write**	**Default**	**Description**
			the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0	**RS** **Run/Stop** When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

6.8.5.7. EHCI USB STATUS REGISTER

Offset: 0x14			Register Name: USBSTS Default Value: 0x00001000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	0	**Reserved** These bits are reserved and should be set to zero.
15	R	0	**ASS** **Asynchronous Schedule Status** The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the

Offset: 0x14			Register Name: USBSTS Default Value: 0x00001000
Bit	**Read/Write**	**Default**	**Description**
			Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0	**PSS** **Periodic Schedule Status** The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0	**RECL** **Reclamation** This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	1	**HCH** **HC Halted** This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is ‘1’.
11:6	/	0	**Reserved** These bits are reserved and should be set to zero.
5	R/WC	0	**IAA** **Interrupt on Async Advance** System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0	**HSE** **Host System Error** The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host

Offset: 0x14			Register Name: USBSTS Default Value: 0x00001000
Bit	**Read/Write**	**Default**	**Description**
			Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0	**FLR** **Frame List Rollover** The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0	**PCD** **Port Change Detect** The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0	**ERRINT** **USB Error Interrupt(USBERRINT)** The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0	**USBINT** **USB Interrupt(USBINT)** The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

6.8.5.8. EHCI USB INTERRUPT ENABLE REGISTER

Offset: 0x18			Register Name: USBINTR Default Value:0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	0	**Reserved** These bits are reserved and should be zero.
5	R/W	0	**IAAE** **Interrupt on Async Advance Enable** When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0	**HSEE** **Host System Error Enable** When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0	**FLRE** **Frame List Rollover Enable** When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0	**PCIE** **Port Change Interrupt Enable** When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0	**EIE** **USB Error Interrupt Enable** When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0	**UIE** **USB Interrupt Enable** When this bit is 1, and the USBINT bit in the USBSTS register

Offset: 0x18			Register Name: USBINTR Default Value:0x00000000
Bit	**Read/Write**	**Default**	**Description**
			is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

6.8.5.9. EHCI FRAME INDEX REGISTER

Offset: 0x1c			Register Name: FRINDEX Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:14	/	0	**Reserved** These bits are reserved and should be zero.
13:0	R/W	0	**FRIND** **Frame Index** The value in this register increment at the end of each time frame(e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

Note: This register must be written as a DWord. Byte writes produce undefined results.

6.8.5.10. EHCI PERIODIC FRAME LIST BASE ADDRESS REGISTER

Offset: 0x24			Register Name: PERIODICLISTBASE Default Value: Undefined
Bit	**Read/Write**	**Default**	**Description**
31:12	R/W		**BADDR** **Base Address** These bits correspond to memory address signals [31:12],

Offset: 0x24			Register Name: PERIODICLISTBASE Default Value: Undefined
Bit	**Read/Write**	**Default**	**Description**
			respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/		**Reserved** Must be written as 0x0 during runtime, the values of these bits are undefined.

Note: Writes must be Dword Writes.

6.8.5.11. EHCI CURRENT ASYNCHRONOUS LIST ADDRESS REGISTER

Offset: 0x28			Register Name: ASYNCLISTADDR Default Value: Undefined
Bit	**Read/Write**	**Default**	**Description**
31:5	R/W		**LP** **Link Pointer (LP)** This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	**Reserved** These bits are reserved and their value has no effect on operation. Bits in this field cannot be modified by system software and will always return a zero when read.

Note: Write must be DWord Writes.

6.8.5.12. EHCI CONFIGURE FLAG REGISTER

Offset: 0x50			Register Name: CONFIGFLAG Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:1	/	0	**Reserved** These bits are reserved and should be set to zero.
0	R/W	0	**CF** **Configure Flag(CF)** Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: <table><tr><td>Value</td><td>Meaning</td></tr><tr><td>0</td><td>Port routing control logic default-routs each port to an implementation dependent classic host controller.</td></tr><tr><td>1</td><td>Port routing control logic default-routs all ports to this host controller.</td></tr></table> The default value of this field is ‘0’.

Note: This register is not use in the normal implementation.

6.8.5.13. EHCI PORT STATUS AND CONTROL REGISTER

Offset: 0x54			Register Name: PORTSC Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)
Bit	**Read/Write**	**Default**	**Description**
31:22	/	0	**Reserved** These bits are reserved for future use and should return a value of zero when read.
21	R/W	0	**WDE** **Wake on Disconnect Enable(WKDSCNNT_E)** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is ‘0’.
20	R/W	0	**WCE** **Wake on Connect Enable(WKCNNT_E)** Writing this bit to a one enable the port to be sensitive to

<table>
<tr><td colspan="3">Offset: 0x54</td><td>Register Name: PORTSC
Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>device connects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0</td><td>/</td></tr>
<tr><td>15:14</td><td>R/W</td><td>0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>13</td><td>R/W</td><td>1</td><td>PO
Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>11:10</td><td>R</td><td>0</td><td>LS
Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x54</td><td>Register Name: PORTSC
Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td><table><tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr></table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>0</td><td>Reserved
This bit is reserved for future use, and should return a value of zero when read.</td></tr>
<tr><td>8</td><td>R/W</td><td>0</td><td>PR
Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit.
Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>SUSPEND
Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table><tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr></table></td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x54</td><td>Register Name: PORTSC
Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>0x</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
<tr><td>11</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
1) Software sets the Force Port Resume bit to a zero(from a one).
2) Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.
</td></tr>
<tr><td>6</td><td>R/W</td><td>0</td><td>
FPR
Force Port Resume
1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0.
This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined.
Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit.
Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed ‘K’) is driven on the port as long as this remains a
</td></tr>
</table>

Offset: 0x54			Register Name: PORTSC Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)
Bit	**Read/Write**	**Default**	**Description**
			one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0	**OCC** **Over-current Change** Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0	**OCA** **Over-current Active** 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is ‘0’.
3	R/WC	0	**PEDC** **Port Enable/Disable Change** Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0	**PED** **Port Enabled/Disabled** 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that

Offset: 0x54			Register Name: PORTSC Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)
Bit	**Read/Write**	**Default**	**Description**
			the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0	**CSC** **Connect Status Change** 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0	**CCS** **Current Connect Status** Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

Note: This register is only reset by hardware or in response to a host controller reset.

6.8.6. OHCI Register List

Register Name	Offset	Description
	The Control and Status Partition Register	
HcRevision	0x400	HcRevision Register
HcCtl	0x404	HcControl Register
HcCommandStatus	0x408	HcCommandStatus Register
HcInterruptStatus	0x40c	HcInterruptStatus Register
HcInterruptEnable	0x410	HcInterruptEnable Register

HcInterruptDisable	0x414	HcInterruptDisable Register
Memory Pointer Partition Register		
HcHCCA	0x418	HcHCCA Register
PCED	0x41c	HcPeriodCurrentED Register
CHED	0x420	HcControlHeadED Register
CCED	0x424	HcControlCurrentED Register
BHED	0x428	HcBulkHeadED Register
BCED	0x42c	HcBulkCurrentED Register
HcDoneHead	0x430	HcDoneHead Register
Frame Counter Partition Register		
HcFmInterval	0x434	HcFmInterval Register
HcFmRemaining	0x438	HcFmRemaining Register
HcFmNumber	0x43c	HcFmNumber Register
HcPeriodicStatus	0x440	HcPerioddicStart Register
HcLSThreshold	0x444	HcLSThreshold Register
Root Hub Partition Register		
HcRhDescriptorA	0x448	HcRhDescriptorA Register
HcRhDescriptorB	0x44c	HcRhDesriptorB Register
HcRhStatus	0x450	HcRhStatus Register
HcRhPortStatus	0x454	HcRhPortStatus Register

6.8.7. OHCI Register Description

6.8.7.1. HCREVISION REGISTER

Offset: 0x400				**Register Name: HcRevision** **Default Value:0x10**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:8				**Reserved**
7:0	R	R	0x10	**Revision** This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

6.8.7.2. HCCONTROL REGISTER

Offset: 0x404				Register Name: HcRevision Default Value:0x0
	Read/Write			
Bit	**HCD**	**HC**	**Default**	**Description**
31:11				**Reserved**
10	R/W	R	0x0	**RemoteWakeupEnable** This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the **ResumeDetected** bit in ***HcInterruptStatus*** is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	**RemoteWakeupConnected** This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
8	R/W	R	0x0	**InterruptRouting** This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	R/W	0x0	**HostControllerFunctionalState for USB** 00b: USBReset 01b: USBResume 10b: USBOperational 11b: USBSuspend A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
				BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcBulkCurrentED* is pointing to an ED to be removed,

<table>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>4</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlListEnable
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>3</td><td>R/W</td><td>R</td><td>0x0</td><td>IsochronousEnable
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.
Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).</td></tr>
<tr><td>2</td><td>R/W</td><td>R</td><td>0x0</td><td>PeriodicListEnable
This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlBulkServiceRatio
This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
<table>
<tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr>
<tr><td>0</td><td>1:1</td></tr>
<tr><td>1</td><td>2:1</td></tr>
<tr><td>2</td><td>3:1</td></tr>
<tr><td>3</td><td>4:1</td></tr>
</table>
The default value is 0x0.</td></tr>
</table>

6.8.7.3. HCCOMMANDSTATUS REGISTER

<table>
<tr><td colspan="4">Offset: 0x408</td><td>Register Name: HcCommandStatus
Default Value:0x0</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td>31:18</td><td></td><td></td><td></td><td>Reserved</td></tr>
<tr><td></td><td></td><td></td><td></td><td>SchedulingOverrunCount
These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if</td></tr>
</table>

17:16	R	R/W	0x0	**SchedulingOverrun** in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4				**Reserved**
3	R/W	R/W	0x0	**OwershipChangeRequest** This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the **OwnershipChange** field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	**BulklListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as **BulkListFilled** is 0, HC will not start processing the Bulk list. If **BulkListFilled** is 1, HC will start processing the Bulk list and will set **BFL** to 0. If HC finds a TD on the list, then HC will set **BulkListFilled** to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set **BulkListFilled**, then **BulkListFilled** will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks **CLF**. As long as **ControlListFilled** is 0, HC will not start processing the Control list. If **CLF** is 1, HC will start processing the Control list and will set **ControlListFilled** to 0. If HC finds a TD on the list, then HC will set **ControlListFilled** to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set **ControlListFilled**, then **ControlListFilled** will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	**HostControllerReset** This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

6.8.7.4. HCINTERRUPTSTATUS REGISTER

Offset: 0x40c				Register Name: HcInterruptStatus Default Value:0x0
	Read/Write			
Bit	**HCD**	**HC**	**Default**	**Description**
31:7				**Reserved**

6	R/W	R/W	0x0	**RootHubStatusChange** This bit is set when the content of ***HcRhStatus*** or the content of any of ***HcRhPortStatus***[**NumberofDownstreamPort**] has changed.
5	R/W	R/W	0x0	**FrameNumberOverflow** This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	**UnrecoverableError** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	**ResumeDetected** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	**StartofFrame** This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	**WritebackDoneHead** This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	**SchedulingOverrun** This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the **SchedulingOverrunCount** of *HcCommandStatus* to be Incremented.

6.8.7.5. HCINTERRUPTENABLE REGISTER

Offset: 0x410				**Register Name: HcInterruptEnable Register** **Default Value: 0x0**
	Read/Write			
Bit	**HCD**	**HC**	**Default**	**Description**
31:7				**Reserved**
6	R/W	R	0x0	**RootHubStatusChange Interrupt Enable** 0: Ignore; 1: Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	**FrameNumberOverflow Interrupt Enable** 0: Ignore; 1: Enable interrupt generation due to Frame Number Over Flow;
				UnrecoverableError Interrupt Enable

4	R/W	R	0x0	0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	**ResumeDetected Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	**StartofFrame Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	**WritebackDoneHead Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	**SchedulingOverrun Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

6.8.7.6. HCINTERRUPTDISABLE REGISTER

Offset: 0x414				**Register Name: HcInterruptDisable Register** **Default Value: 0x0**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	**MasterInterruptEnable** A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7				**Reserved**
6	R/W	R	0x0	**RootHubStatusChange Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	**FrameNumberOverflow Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	**UnrecoverableError Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	**ResumeDetected Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	**StartofFrame Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Start of Flame;

1	R/W	R	0x0	**WritebackDoneHead Interrupt Disable** 0: Ignore; 1: Disable interrupt generation due to Write back Done Head;
0	R/w	R	0x0	**SchedulingOverrun Interrupt Disable** 0: Ignore; 1: Disable interrupt generation due to Scheduling Overrun;

6.8.7.7. HCHCCA REGISTER

Offset: 0x418				Register Name: HcHCCA Default Value:0x0
Bit	Read/Write HCD	Read/Write HC	Default	Description
31:8	R/W	R	0x0	**HCCA[31:8]** This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R/W	R	0x0	**HCCA[7:0]** The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

6.8.7.8. HCPERIODCURRENTED REGISTER

Offset: 0x41c				Register Name: HcPeriodCurrentED(PCED) Default Value: 0x0
Bit	Read/Write HCD	Read/Write HC	Default	Description
31:4	R	R/W	0x0	**PCED[31:4]** This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R/W	0x0	**PCED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

6.8.7.9. HCCONTROLHEADED REGISTER

Offset: 0x420	Register Name: HcControlHeadED[CHED] Default Value: 0x0

Bit	Read/Write HCD	HC	Default	Description
31:4	R/W	R	0x0	**CHED[31:4]** The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R/W	R	0x0	**CHED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

6.8.7.10. HCCONTROLCURRENTED REGISTER

Offset: 0x424				Register Name: HcControlCurrentED[CCED] Default Value: 0x0
Bit	**Read/Write HCD**	**HC**	**Default**	**Description**
31:4	R/W	R/W	0x0	**CCED[31:4]** The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially , this is set to zero to indicate the end of the Control list.
3:0	R/W	R/W	0x0	**CCED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

6.8.7.11. HCBULKHEADED REGISTER

Offset: 0x428				Register Name: HcBulkHeadED[BHED] Default Value: 0x0
Bit	**Read/Write HCD**	**HC**	**Default**	**Description**
31:4	R/W	R	0x0	**BHED[31:4]** The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
				BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits

3:0	R/W	R	0x0	in the PCED, through bit 0 to bit 3 must be zero in this field.

6.8.7.12. HCBULKCURRENTED REGISTER

Offset: 0x42c				Register Name: HcBulkCurrentED [BCED] Default Value: 0x0
Bit	Read/Write HCD	HC	Default	Description
31:4	R/W	R/W	0x0	**BulkCurrentED[31:4]** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the **ControlListFilled** of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the **BulkListEnable** of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R/W	R/W	0x0	**BulkCurrentED [3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

6.8.7.13. HCDONEHEAD REGISTER

Offset: 0x430				Register Name: HcDoneHead Default Value:0x0
Bit	Read/Write HCD	HC	Default	Description
31:4	R	R/W	0x0	**HcDoneHead[31:4]** When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the **WritebackDoneHead** of *HcInterruptStatus*.
3:0	R	R/W	0x0	**HcDoneHead[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

6.8.7.14. HCFMINTERVAL REGISTER

Offset: 0x434				Register Name: HcFmInterval Register Default Value:0x2edf
Bit	Read/Write HCD	HC	Default	Description

31	R/W	R	0x0	**FrameIntervalToggler** HCD toggles this bit whenever it loads a new value to **FrameInterval**.
30:16	R/W	R	0x0	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14				**Reserved**
13:0	R/W	R	0x2edf	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the **HostControllerReset** field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

6.8.7.15. HCFMREMAINING REGISTER

Offset: 0x438				Register Name: HcFmRemaining Default Value: 0x0
Bit	Read/Write HCD	Read/Write HC	Default	Description
31	R	R/W	0x0	**FrameRemaining Toggle** This bit is loaded from the **FrameIntervalToggle** field of *HcFmInterval* whenever **FrameRemaining** reaches 0. This bit is used by HCD for the synchronization between **FrameInterval** and **FrameRemaining**.
30:14	/	/	/	**Reserved**
13:0	R	RW	0x0	**FramRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

6.8.7.16. HCFMNUMBER REGISTER

Offset: 0x43c				Register Name: HcFmNumber Default Value:0x0
Bit	Read/Write HCD	Read/Write HC	Default	Description
31:16	/	/	/	**Reserved**

15:0	R	R/W	0x0	**FrameNumber** This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the **FrameNumber** at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the **StartofFrame** in *HcInterruptStatus.*

6.8.7.17. HCPERIODICSTART REGISTER

Offset: 0x440				**Register Name: HcPeriodicStatus** **Default Value: 0x0**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:14	/	/	/	**Reserved**
13:0	R/W	R	0x0	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*.. A typical value will be 0x3e67. When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

6.8.7.18. HCLSTHRESHOLD REGISTER

Offset: 0x444				**Register Name: HcLSThreshold** **Default Value: 0x0628**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:12				**Reserved**
11:0	R/W	R	0x0628	**LSThreshold** This field contains a value which is compared to the **FrameRemaining** field prior to initiating a Low Speed transaction. The transaction is started only if **FrameRemaining** >= this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

6.8.7.19. HCRHDESCRIPTORA REGISTER

Offset: 0x448				**Register Name: HcRhDescriptorA** **Default Value:0x02001201**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:24	R/W	R	0x02	**PowerOnToPowerGoodTime[POTPGT]** This byte specifies the duration HCD has to wait before accessing

<table>
<tr><td></td><td></td><td></td><td></td><td>a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.</td></tr>
<tr><td>23:13</td><td></td><td></td><td></td><td>Reserved</td></tr>
<tr><td>12</td><td>R/W</td><td>R</td><td>0x01</td><td>NoOverCurrentProtection
This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting.<table><tr><td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr><tr><td>1</td><td>No overcurrent protection supported.</td></tr></table></td></tr>
<tr><td>11</td><td>R/W</td><td>R</td><td>0x0</td><td>OverCurrentProtectionMode
This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared.<table><tr><td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr><tr><td>1</td><td>Over-current status is reported on per-port basis.</td></tr></table></td></tr>
<tr><td>10</td><td>R</td><td>R</td><td>0x0</td><td>Device Type
This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.</td></tr>
<tr><td>9</td><td>R/W</td><td>R</td><td>0x01</td><td>PowerSwitchingMode
This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared.<table><tr><td>0</td><td>All ports are powered at the same time.</td></tr><tr><td>1</td><td>Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port
switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).</td></tr></table></td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>NoPowerSwithcing
These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.<table><tr><td>0</td><td>Ports are power switched.</td></tr><tr><td>1</td><td>Ports are always powered on when the HC is powered on.</td></tr></table></td></tr>
<tr><td>7:0</td><td>R</td><td>R</td><td>0x01</td><td>NumberDownstreamPorts
These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.</td></tr>
</table>

6.8.7.20. HCRHDESCRIPTORB REGISTER

Offset: 0x44c				Register Name: HcRhDescriptorB Register **Default Value:**0x0
	Read/Write			
Bit	**HCD**	**HC**	**Default**	**Description**
31:16	R/W	R	0x0	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when **PowerSwitchingMode** is set. When set, the port's power state is only affected by per-port power control (**Set/Counterpower**). When cleared, the port is controlled by the global power switch (**Set/ClearGlobalPower**). If the device is configured to global switching mode (**PowerSwitchingMode** = 0), this field is not valid. Bit0 | Reserved Bit1 | Ganged-power mask on Port #1. Bit2 | Ganged-power mask on Port #2. … Bit15 | Ganged-power mask on Port #15.
15:0	R/W	R	0x0	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 | Reserved Bit1 | Device attached to Port #1. Bit2 | Device attached to Port #2. … Bit15 | Device attached to Port #15.

6.8.7.21. HCRHSTATUS REGISTER

Offset: 0x450				Register Name: HcRhStatus Register **Default Value:**0x0
	Read/Write			
Bit	**HCD**	**HC**	**Default**	**Description**
31	W	R	0x0	**(write)ClearRemoteWakeupEnable** Write a '1' clears **DeviceRemoteWakeupEnable.** Write a '0' has no effect.
30:18	/	/	/	**Reserved**
17	R/W	R	0x0	**OverCurrentIndicatorChang** This bit is set by hardware when a change has occurred to the **OverCurrentIndicator** field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
				(read)LocalPowerStartusChange

16	R/W	R	0x0	The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’. **(write)SetGlobalPower** In global power mode (**PowerSwitchingMode**=0), This bit is written to ‘1’ to turn on power to all ports (clear **PortPowerStatus**). In per-port power mode, it sets **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a ‘0’ has no effect.
15	R/W	R	0x0	**(read)DeviceRemoteWakeupEnable** This bit enables a **ConnectStatusChange** bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the **ResumeDetected** interrupt. 0 | **ConnectStatusChange** is not a remote wakeup event. 1 | **ConnectStatusChange** is a remote wakeup event. **(write)SetRemoteWakeupEnable** Writing a ‘1’ sets DeviceRemoveWakeupEnable. Writing a ‘0’ has no effect.
14:2	/	/	/	**Reserved**
1	R	R/W	0x0	**OverCurrentIndicator** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always ‘0’
0	R/W	R	0x0	**(Read)LocalPowerStatus** When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as ‘0’. **(Write)ClearGlobalPower** When write, this bit is operated as the ClearGlobalPower. In global power mode (**PowerSwitchingMode**=0), This bit is written to ‘1’ to turn off power to all ports (clear **PortPowerStatus**). In per-port power mode, it clears **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a ‘0’ has no effect.

6.8.7.22. HCRHPORTSTATUS REGISTER

Offset: 0x454				Register Name: HcRhPortStatus Default Value:0x100
Bit	Read/Write HCD	 HC	Default	Description
31:21			-	**Reserved**
20	R/W	R/W	0x0	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. 0 | port reset is not complete 1 | port reset is complete
				PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a

19	R/W	R/W	0x0	per-port basis. This bit is set when Root Hub changes the **PortOverCurrentIndicator** bit. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. 0 | no change in **PortOverCurrentIndicator** 1 | **PortOverCurrentIndicator** has changed
18	R/W	R/W	0x0	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. This bit is also cleared when **ResetStatusChange** is set. 0 | resume is not completed 1 | resume completed
17	R/W	R/W	0x0	**PortEnableStatusChange** This bit is set when hardware events cause the **PortEnableStatus** bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. 0 | no change in **PortEnableStatus** 1 | change in **PortEnableStatus**
16	R/W	R/W	0x0	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If **CurrentConnectStatus** is cleared when a **SetPortReset,SetPortEnable**, or **SetPortSuspend** write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 | no change in **PortEnableStatus** 1 | change in **PortEnableStatus** Note: If the **DeviceRemovable[NDP]** bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10				**Reserved**
9	R/W	R/W	-	(read)**LowSpeedDeviceAttached** This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the **CurrentConnectStatus** is set. 0 | full speed device attached 1 | low speed device attached (write)**ClearPortPower** The HCD clears the **PortPowerStatus** bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.
				(read)**PortPowerStatus** This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing **SetPortPower** or **SetGlobalPower**. HCD clears this bit by writing **ClearPortPower** or **ClearGlobalPower**. Which power control switches are enabled

<table>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x0</td><td>is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls
this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>

(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.

Note: This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td></td><td></td><td></td><td>Reserved</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>

(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>

(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td></td><td></td><td></td><td></td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is</td></tr>
</table>

<table>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.<table><tr><td>0</td><td>port is disabled</td></tr><tr><td>1</td><td>port is enabled</td></tr></table>
(write)SetPortEnable
The HCD sets PortEnableStatus by writing a ‘1’. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.</td></tr>
<tr><td>0</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)CurrentConnectStatus
This bit reflects the current state of the downstream port.<table><tr><td>0</td><td>No device connected</td></tr><tr><td>1</td><td>Device connected</td></tr></table>(write)ClearPortEnable
The HCD writes a ‘1’ to clear the PortEnableStatus bit. Writing ‘0’ has no effect. The CurrentConnectStatus is not affected by any write.

Note: This bit is always read ‘1’ when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).</td></tr>
</table>

6.8.8. USB Host Special Requirement

6.8.8.1. USB HOST CLOCK REQUIRMENT

Name	Description
HCLK	System clock (provided by AHB bus clock). This clock needs to be >30MHz.
CLK60M	Clock from PHY for HS SIE, is constant to be 60MHz.

6.9. Digital Audio Interface

6.9.1. Overview

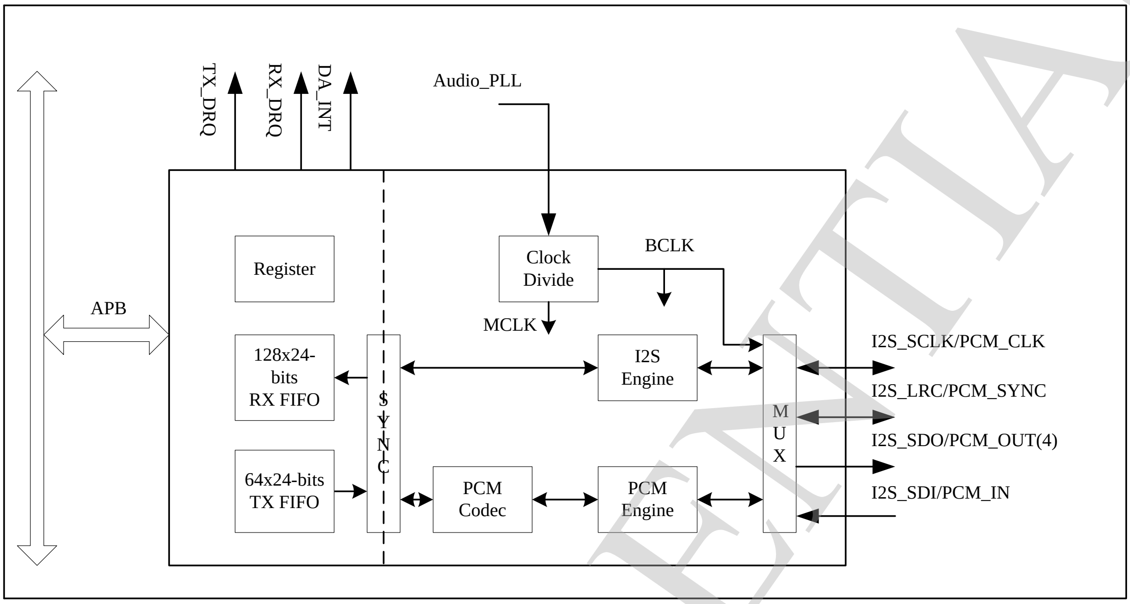
The Digital Audio Interface can be configured as I2S interface or PCM interface by software. When configured as I2S interface ,it can support the industry standard format for I2S, left-justified, or right-justified. PCM is a standard method used to digital audio for transmission over digital communication channels. It supports linear 13 or 16-bits linear, or 8-bit u-law or A-law companded sample formats at 8K samples/s and can receive and transmit on any selection of four of the first four slots following PCM_SYNC.

It features:

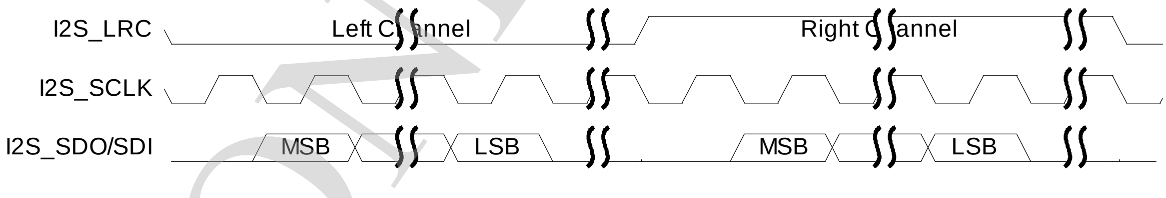
- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Support APB 32-bit bus width
- I2S or PCM configured by software
- Full-duplex synchronous serial interface
- Master / Slave mode operation configured by software
- Audio data resolution of 16, 20, 24
- I2S Audio data sample rate from 8KHz to 192KHz
- I2S data format for standard I2S, Left Justified and Right Justified
- I2S support 8-channel output and 2-channel input
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law companded sample
- One 128x24-bit FIFO for data transmit, one 64x24-bit FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA support
- Two 32-bit counters for AV sync application
- Loopback mode for test

6.9.2. Digital Audio Interface Block Diagram

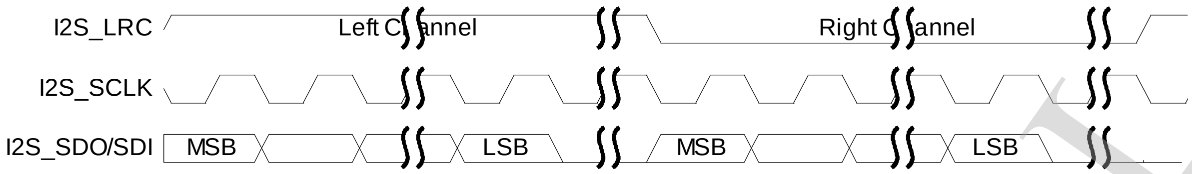
The Digital Audio Interface block diagram is shown below:



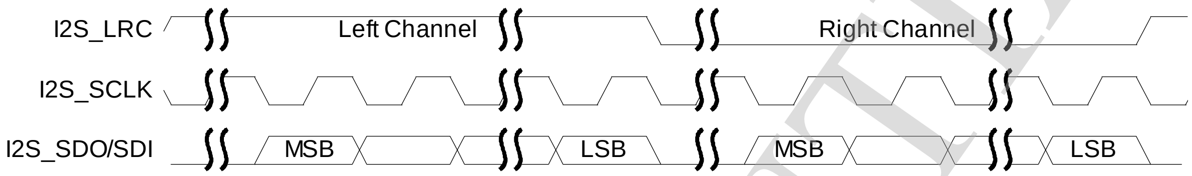
6.9.3. Digital Audio Interface Timing Diagram



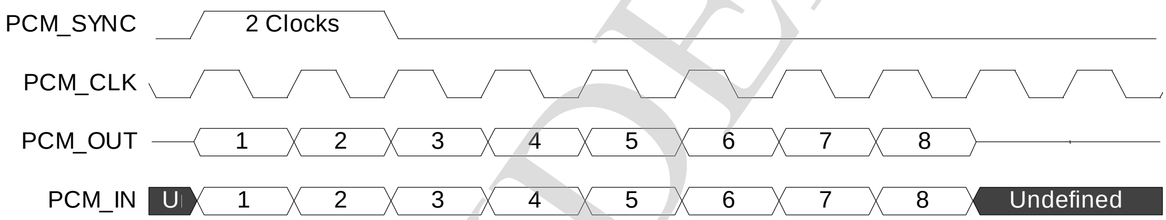
Standard I2S Timing Diagram



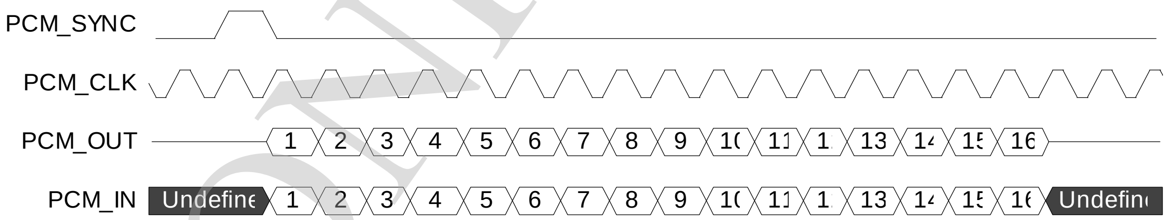
Left-justified I2S Timing Diagram



Right-justified I2S Timing Diagram



PCM Long Frame SYNC Timing Diagram (8-bits Companded Sample Example)



PCM Short Frame SYNC Timing Diagram (16-bits sample example)

6.9.4. Digital Audio Interface Register List

Module Name	Base Address
DA0	0x01C22400
DA1	0x01C22000

Register Name	Offset	Description
DA_CTL	0x00	Digital Audio Control Register
DA_FAT0	0x04	Digital Audio Format Register 0
DA_FAT1	0x08	Digital Audio Format Register 1
DA_TXFIFO	0x0C	Digital Audio TX FIFO Register
DA_RXFIFO	0x10	Digital Audio RX FIFO Register
DA_FCTL	0x14	Digital Audio FIFO Control Register
DA_FSTA	0x18	Digital Audio FIFO Status Register
DA_INT	0x1C	Digital Audio Interrupt Control Register
DA_ISTA	0x20	Digital Audio Interrupt Status Register
DA_CLKD	0x24	Digital Audio Clock Divide Register
DA_TXCNT	0x28	Digital Audio RX Sample Counter Register
DA_RXCNT	0x2C	Digital Audio TX Sample Counter Register
DA_TXCHSEL	0x30	Digital Audio TX Channel Select register
DA_TXCHMAP	0x34	Digital Audio TX Channel Mapping Register

6.9.5. Digital Audio Interface Register Description

6.9.5.1. DIGITAL AUDIO CONTROL REGISTER

Offset: 0x00			**Register Name: DA_CTL** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11	R/W	0	SDO3_EN

Offset: 0x00			Register Name: DA_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			0: Disable 1: Enable
10	R/W	0	SDO2_EN 0: Disable 1: Enable
9	R/W	0	SDO1_EN 0: Disable 1: Enable
8	R/W	0	SDO0_EN 0: Disable 1: Enable
7	/	/	/
6	R/W	0	ASS Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
5	R/W	0	MS Master Slave Select 0: Master 1: Slave
4	R/W	0	PCM 0: I2S Interface 1: PCM Interface
3	R/W	0	/
2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN

Offset: 0x00			Register Name: DA_CTL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
			Globe Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

6.9.5.2. DIGITAL AUDIO FORMAT REGISTER 0

Offset: 0x04			Register Name: DA_FAT0 Default Value: 0x0000_000C
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	LRCP Left/ Right Clock Parity 0: Normal 1: Inverted In DSP/ PCM mode 0: MSB is available on 2nd BCLK rising edge after LRC rising edge 1: MSB is available on 1st BCLK rising edge after LRC rising edge
6	R/W	0	BCP BCLK Parity 0: Normal 1: Inverted
5:4	R/W	0	SR Sample Resolution 00: 16-bit 01: 20-bit 10: 24-bit 11: Reserved
3:2	R/W	0x3	WSS Word Select Size

Offset: 0x04			Register Name: DA_FAT0 Default Value: 0x0000_000C
Bit	**Read/Write**	**Default**	**Description**
			00: 16 BCLK 01: 20 BCLK 10: 24 BCLK 11: 32 BCLK
1:0	R/W	0	FMT Serial Data Format 00: Standard I2S Format 01: Left Justified Format 10: Right Justified Format 11: Reserved

6.9.5.3. DIGITAL AUDIO FORMAT REGISTER 1

Offset: 0x08			Register Name: DA_FAT1 Default Value: 0x0000_4020
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	0x4	PCM_SYNC_PERIOD PCM SYNC Period Clock Number 000: 16 BCLK period 001: 32 BCLK period 010: 64 BCLK period 011: 128 BCLK period 100: 256 BCLK period Others : Reserved
11	R/W	0	PCM_SYNC_OUT PCM Sync Out 0: Enable PCM_SYNC output in Master mode 1: Suppress PCM_SYNC whilst keeping PCM_CLK running. Some Codec utilize this to enter a low power state.
10	R/W	0	PCM Out Mute Write 1 force PCM_OUT to 0
9	R/W	0	MLS

Offset: 0x08			Register Name: DA_FAT1 Default Value: 0x0000_4020
Bit	**Read/Write**	**Default**	**Description**
			MSB / LSB First Select 0: MSB First 1: LSB First
8	R/W	0	SEXT Sign Extend (only for 16 bits slot) 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit companding sample. When writing the bit is 1, the unused bits are both sign extension.
7:6	R/W	0	SI Slot Index 00: the 1st slot 01: the 2nd slot 10: the 3rd slot 11: the 4th slot
5	R/W	1	SW Slot Width 0: 8 clocks width 1: 16 clocks width Note: For A-law or u-law PCM sample, if this bit is set to 1, eight zero bits are following with PCM sample.
4	R/W	0	SSYNC Short Sync Select 0: Long Frame Sync 1: Short Frame Sync It should be set ‘1’ for 8 clocks width slot.
3:2	R/W	0	RX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law

Offset: 0x08			Register Name: DA_FAT1 Default Value: 0x0000_4020
Bit	**Read/Write**	**Default**	**Description**
1:0	R/W	0	TX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law

6.9.5.4. DIGITAL AUDIO TX FIFO REGISTER

Offset: 0x0C			Register Name: DA_TXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

6.9.5.5. DIGITAL AUDIO RX FIFO REGISTER

Offset: 0x10			Register Name: DA_RXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

6.9.5.6. DIGITAL AUDIO FIFO CONTROL REGISTER

Offset: 0x14			Register Name: DA_FCTL Default Value: 0x0004_00F0
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0	FIFOSRC TX FIFO source select 0: APB bus 1: Analog Audio CODEC
30:26	/	/	/
25	R/W	0	FTX Write '1' to flush TX FIFO, self clear to '0'.
24	R/W	0	FRX Write '1' to flush RX FIFO, self clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0	TXIM TX FIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[23:0] = {4'h0, TXFIFO[31:12]} Mode 1: FIFO_I[23:0] = {4'h0, TXFIFO[19:0]}
1:0	R/W	0	RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of DA_RXFIFO register.

Offset: 0x14			Register Name: DA_FCTL Default Value: 0x0004_00F0
Bit	**Read/Write**	**Default**	**Description**
			01: Expanding received sample sign bit at MSB of DA_RXFIFO register. 10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by '0'. 11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: RXFIFO[31:0] = {FIFO_O[19:0], 12'h0} Mode 1: RXFIFO[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0]} Mode 2: RXFIFO[31:0] = {FIFO_O[19:4], 16'h0} Mode 3: RXFIFO[31:0] = {16{FIFO_O[19], FIFO_O[19:4]}

6.9.5.7. DIGITAL AUDIO FIFO STATUS REGISTER

Offset: 0x18			Register Name: DA_FSTA Default Value: 0x1080_0000
Bit	**Read/Write**	**Default**	**Description**
31:29	/	/	/
28	R	1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/

Offset: 0x18			Register Name: DA_FSTA Default Value: 0x1080_0000
Bit	**Read/Write**	**Default**	**Description**
6:0	R	0	RXA_CNT RX FIFO Available Sample Word Counter

6.9.5.8. DIGITAL AUDIO DMA & INTERRUPT CONTROL REGISTER

Offset: 0x1C			Register Name: DA_INT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to ‘1’, an interrupt happens when writing new audio data if TX FIFO is full.
4	R/W	0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0	RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to ‘1’, RXFIFO DMA Request line is asserted if Data is available in RX FIFO.

Offset: 0x1C			Register Name: DA_INT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
2	R/W	0	RXUI_EN RX FIFO Under run Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

6.9.5.9. DIGITAL AUDIO INTERRUPT STATUS REGISTER

Offset: 0x20			Register Name: DA_ISTA Default Value: 0x0000_0010
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt
4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write ‘1’ to clear this interrupt or automatic clear if interrupt

Offset: 0x20			Register Name: DA_ISTA Default Value: 0x0000_0010
Bit	**Read/Write**	**Default**	**Description**
			condition fails.
3:2	/	/	/
2	R/W	0	RXU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt Write 1 to clear this interrupt
1	R/W	0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	R/W	0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

6.9.5.10. DIGITAL AUDIO CLOCK DIVIDE REGISTER

Offset: 0x24			Register Name: DA_CLKD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.
6:4	R/W	0	BCLKDIV BCLK Divide Ratio from MCLK

Offset: 0x24			Register Name: DA_CLKD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			000: Divide by 2 (BCLK = MCLK/2) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 12 101: Divide by 16 110: Divide by 32 111: Divide by 64
3:0	R/W	0	MCLKDIV MCLK Divide Ratio from Audio PLL Output 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0011: Divide by 6 0100: Divide by 8 0101: Divide by 12 0110: Divide by 16 0111: Divide by 24 1000: Divide by 32 1001: Divide by 48 1010: Divide by 64 Others : Reserved

6.9.5.11. DIGITAL AUDIO TX COUNTER REGISTER

Offset: 0x28			Register Name: DA_TXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After

Offset: 0x28			Register Name: DA_TXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			been updated by the initial value, the counter register should count on base of this initial value.

6.9.5.12. DIGITAL AUDIO RX COUNTER REGISTER

Offset: 0x2C			Register Name: DA_RXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

6.9.5.13. DIGITAL AUDIO TX CHANNEL SELECT REGISTER

Offset: 0x30			Register Name: DA_TXCHSEL Default Value: 0x0000_0001
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2:0	R/W	1	TX_CHSEL TX Channel Select 0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch 4: 5-ch 5: 6-ch 6: 7-ch 7: 8-ch

6.9.5.14. DIGITAL AUDIO TX CHANNEL MAPPING REGISTER

Offset: 0x34			Register Name: DA_TXCHMAP Default Value: 0x7654_3210
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	7	TX_CH7_MAP TX Channel7 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
27	/	/	/
26:24	R/W	6	TX_CH6_MAP TX Channel6 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
23	/	/	/
22:20	R/W	5	TX_CH5_MAP TX Channel5 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample

Offset: 0x34			Register Name: DA_TXCHMAP Default Value: 0x7654_3210
Bit	**Read/Write**	**Default**	**Description**
			101: 6th sample 110: 7th sample 111: 8th sample
19	/	/	/
18:16	R/W	4	TX_CH4_MAP TX Channel4 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
15	/	/	/
14:12	R/W	3	TX_CH3_MAP TX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
11	/	/	/
10:8	R/W	2	TX_CH2_MAP TX Channel2 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample

Offset: 0x34			Register Name: DA_TXCHMAP Default Value: 0x7654_3210
Bit	**Read/Write**	**Default**	**Description**
			110: 7th sample 111: 8th sample
7	/	/	/
6:4	R/W	1	TX_CH1_MAP TX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
3	/	/	/
2:0	R/W	0	TX_CH0_MAP TX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample

6.9.5.15. DIGITAL AUDIO RX CHANNEL SELECT REGISTER

Offset: 0x38			Register Name: DA_RXCHSEL Default Value: 0x0000_0001
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2:0	R/W	1	RX_CHSEL

Offset: 0x38			Register Name: DA_RXCHSEL Default Value: 0x0000_0001
Bit	**Read/Write**	**Default**	**Description**
			RX Channel Select 0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch Others: Reserved

6.9.5.16. DIGITAL AUDIO RX CHANNEL MAPPING REGISTER

Offset: 0x3C			Register Name: DA_RXCHMAP Default Value: 0x0000_3210
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	3	RX_CH3_MAP RX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
11	/	/	/
10:8	R/W	2	RX_CH2_MAP RX Channel2 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
7	/	/	/
6:4	R/W	1	RX_CH1_MAP RX Channel1 Mapping 000: 1st sample

Offset: 0x3C			Register Name: DA_RXCHMAP Default Value: 0x0000_3210
Bit	**Read/Write**	**Default**	**Description**
			001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
3	/	/	/
2:0	R/W	0	RX_CH0_MAP RX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved

6.9.6. Digital Audio Interface Special Requirement

6.9.6.1. DIGITAL AUDIO INTERFACE PIN LIST

Port Name	Width	Direction(M)	Description
DA_BCLK	1	IN/OUT	Digital Audio Serial Clock
DA_LRC	1	IN/OUT	Digital Audio Sample Rate Clock/ Sync
DA_SDO	1	OUT	Digital Audio Serial Data Output
DA_SDI	1	IN	Digital Audio Serial Data Input
DA_MCLK	1	OUT	Digital Audio MCLK Output

6.9.6.2. DIGITAL AUDIO INTERFACE MCLK AND BCLK

The Digital Audio Interface can support sampling rates from 128fs to 768fs, where fs is the audio sampling frequency typically 32kHz, 44.1kHz, 48kHz or 96kHz. For different sampling frequencies, the tables list the coefficient value of MCLKDIV and BCLKDIV.

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
8	24	16	12	8	6	4
16	12	8	6	4	X	2
32	6	4	X	2	X	1
64	X	2	X	1	X	X
128	X	1	X	X	X	X
12	16	X	8	X	4	X
24	8	X	4	X	2	X
48	4	X	2	X	1	X
96	2	X	1	X	X	X
192	1	X	X	X	X	X

MCLKDIV value for 24.576MHz Audio Serial Frequency

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
11.025	16	X	8	X	4	X
22.05	8	X	4	X	2	X
44.1	4	X	2	X	1	X
88.2	2	X	1	X	X	X
176.4	1	X	X	X	X	X

MCLKDIV value for 22.5792 MHz Audio Serial Frequency

Word Select Size	128fs	192fs	256fs	384fs	512fs	768fs
16	4	6	8	12	16	X
24	X	4	X	8	X	16
32	2	X	4	6	8	12

BCLKDIV value for Different Word Select Size

DIGITAL AUDIO INTERFACE CLOCK SOURCE AND FREQUENCY

There are two clocks for Digital Audio Interface. One is from APB bus and one is from Audio PLL.

Name	Description
Audio_PLL	24.576Mhz or 22.528Mhz generated by Audio PLL

Name	Description
APB_CLK	APB bus system clock. In I2S mode, it is requested >= 0.25 BCLK. In PCM mode, it is requested >= 0.5 BCLK.

6.10. AC97 Interface

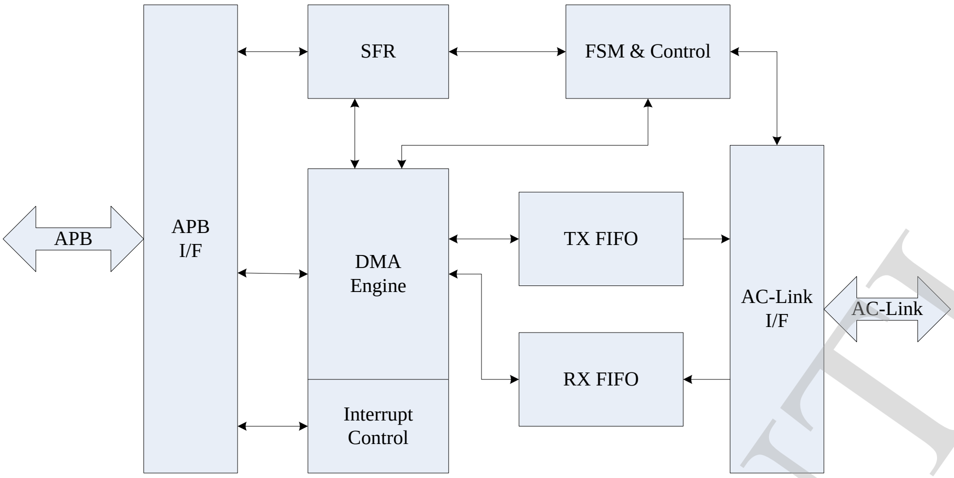
6.10.1. Overview

The AC97 interface supports AC97 revision 2.3 features. AC97 controller communicates with AC97 Codec using an audio controller link (AC-link). Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec converts the audio sample to an analog audio waveform. Controller receives the stereo PCM data and the mono Microphone data from Codec then stores in memories.

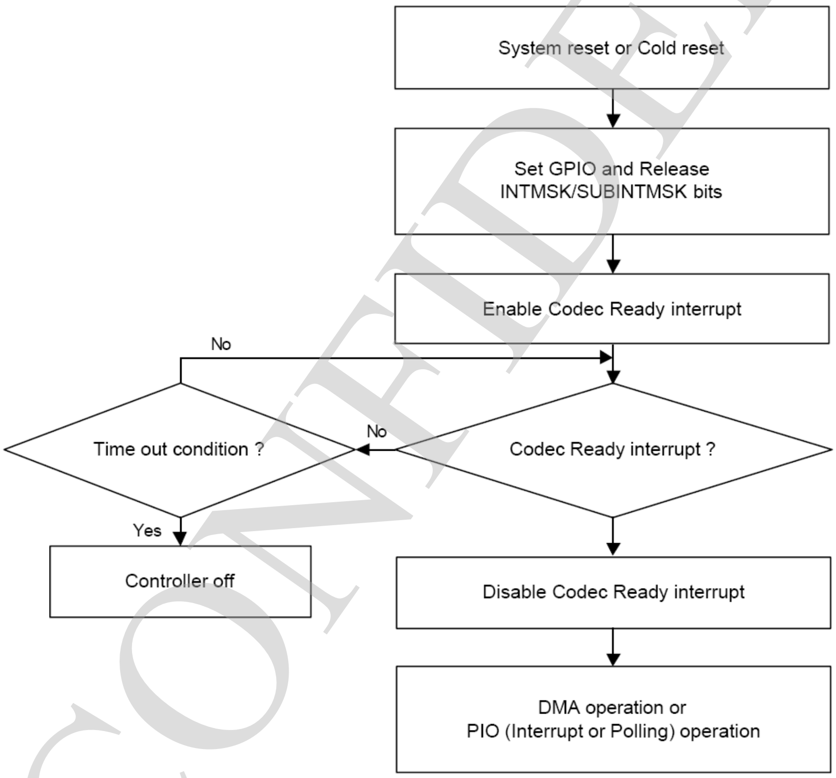
It features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Support APB 32-bits bus width
- Comply with AC97 2.3 component specification
- Full-duplex synchronous serial interface
- Support 2 channels, TX (stereo),RX (PCM stereo, MIC mono optional)
- Variable sampling rate AC97 codec interface support, up to 48KHz
- Support 2-channel and 6-channel audio data output
- DRA mode support
- Only one primary codec support
- Channels support mono or stereo samples of 16(standard), 18(optional) and 20(optional) bit wide
- One 96×20-bit FIFO and one 32×20-bit FIFO for data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

10.2. AC97 Block diagram



AC97 Interface Block Diagram

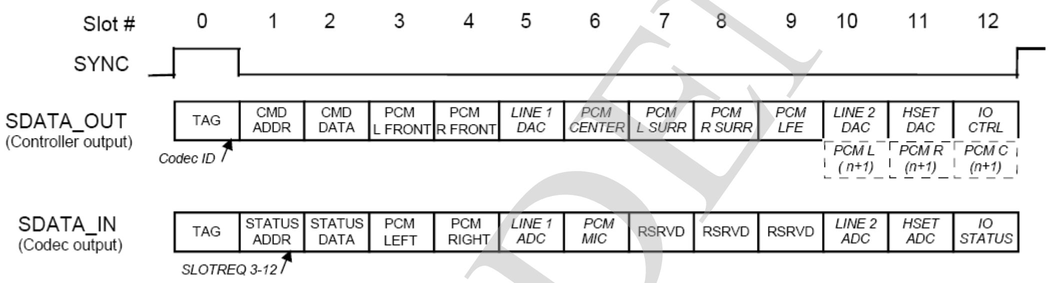


Operation Flow Diagram

6.10.3. AC97 Interface Clock Tree

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the Controller. The Controller generates SYNC by dividing BIT_CLK by 256 and applying some condition to tailor its duty cycle. This yields a 48 KHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving device on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

6.10.4. AC Link Frame Format



Bi-directional AC-link Frame with slot assignments

The AC-link output slots (transmitted from the Controller) are defined as follows:

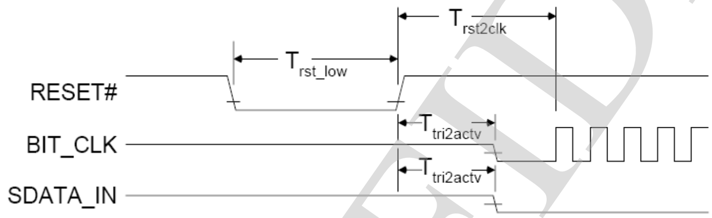
Slot	Name	Description
0	SDATA_OUT TAG	MSBs indicate which slots contain valid data; LSBs convey Codec ID
1	Control CMD ADDR write port	Read/write command bit plus 7-bit Codec register address
2	Control DATA write port	16-bit command register write data
3,4	PCM L&R DAC playback	16, 18, or 20-bit PCM data for Left and Right channels
5	Modem Line 1 DAC	16-bit modem data for modem Line 1 output
6,7,8,9	PCM Center, Surround L&R, LFE	16, 18, or 20-bit PCM data for Center, Surround L&R, LFE channels
10	Modem Line 2 DAC	16-bit modem data for modem Line 2 output
11	Modem handset DAC	16-bit modem data for modem Handset output
12	Modem IO control	GPIO write port for modem Control
10-11	SPDIF Out	Optional AC-link bandwidth for SPDIF output
6-12	Double rate audio	Optional AC-link bandwidth for 88.2 or 96 kHz on L, C, R channels. Actual slots used are controlled by the DRSS bits.

The AC-link input slots (transmitted from the Codec) are defined as follows:

Slot	Name	Description
0	SDATA_IN TAG	MSBs indicate which slots contain valid data
1	STATUS ADDR read port	MSBs echo register address; LSBs indicate which slots request data
2	STATUS DATA read port	16-bit command register read data
3,4	PCM L&R ADC record	16, 18 or 20-bit PCM data from Left and Right inputs
5	Modem Line 1 ADC	16-bit modem data from modem Line1 input
6	Dedicated Microphone ADC	16, 18 or 20-bit PCM data from optional 3rd ADC input
7,8,9	Vendor reserved	Vendor specific (enhanced input for docking, array mic, etc)
10	Modem Line 2 ADC	16-bit modem data from modem Line 2 input
11	Modem handset input ADC	16-bit modem data for modem Handset input
12	Modem IO status	GPIO read port for modem Status

6.10.5. AC97 Interface Timing Diagram

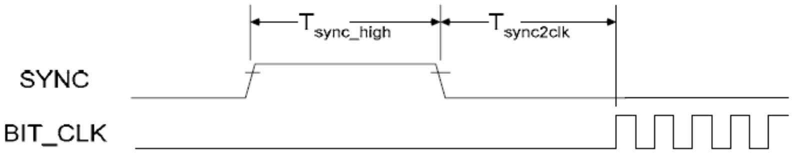
6.10.5.1. COLD RESET TIMING DIAGRAM



Cold Reset timing parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to SDATA_IN or BIT_CLK active delay	$T_{tri2actv}$	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

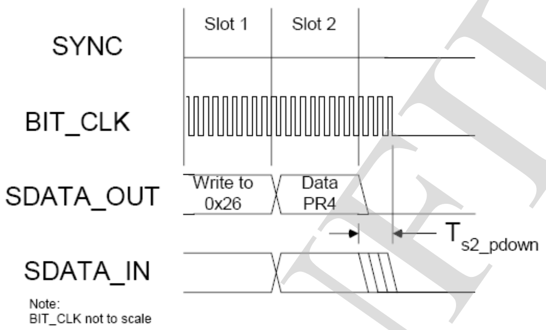
6.10.5.2. WARM RESET TIMING DIAGRAM



Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

Warm Reset timing parameters

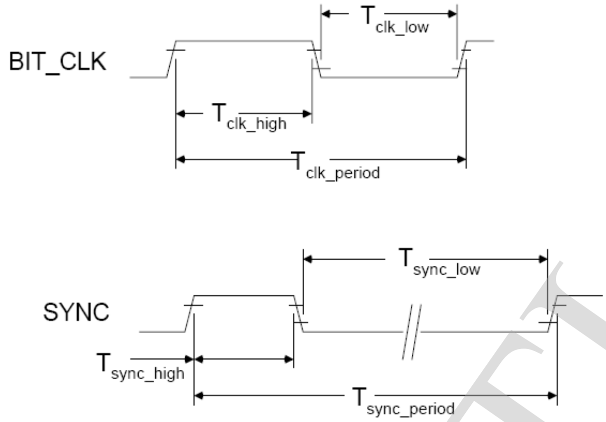
6.10.5.3. POWER DOWN TIMING DIAGRAM



AC-link low power mode timing parameters

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

6.10.5.4. AC-LINK CLOCK

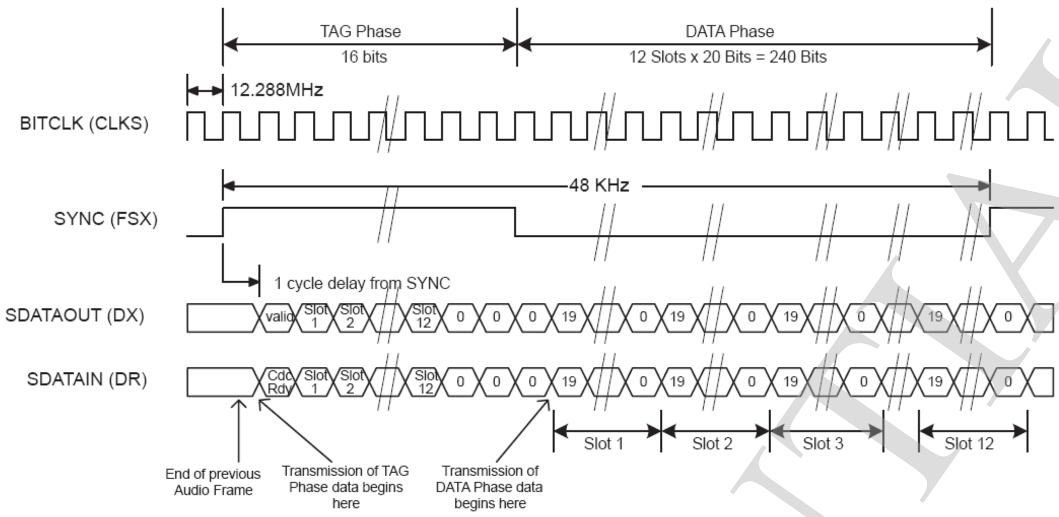


BIT_CLK and SYNC Timing diagram

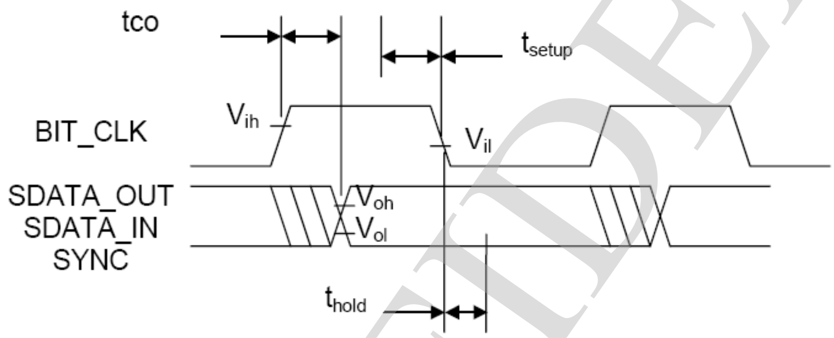
BIT_CLK and SYNC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Note 1: 47.5-75 pF external load as per Table 54 Note 2: Worst case duty cycle restricted to 45/55					

6.10.5.5. DATA TRANSMISSION TIMING DIAGRAM



Data transmission timing diagram



Data Output and Input Timing Diagram

AC-link Output Valid Delay Timing Parameters

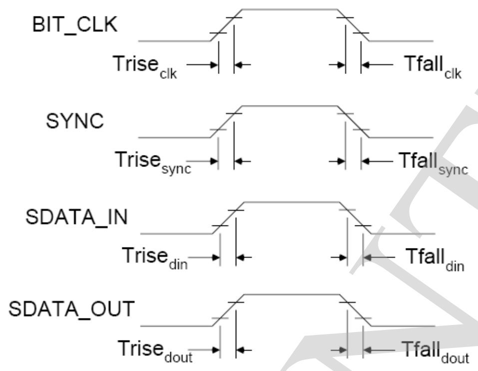
Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	tco	-	-	15	ns
Note: 47.5-75pF external load as per Table 54					

AC-link Input Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns

AC-link Combined Rise or Fall plus Flight Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes					



Signal rise and fall timing diagram

Signal Rise and Fall Time Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time (Note 1)	$Trise_{clk}$	-	-	6	ns
BIT_CLK fall time (Note 1)	$Tfall_{clk}$	-	-	6	ns
SYNC rise time (Note 2)	$Trise_{sync}$	-	-	6	ns
SYNC fall time (Note 2)	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time (Note 3)	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time (Note 3)	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time (Note 2)	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time (Note 2)	$Tfall_{dout}$	-	-	6	ns
Note 1: BIT_CLK rise/fall times with an external load of 75 pF Note 2: SYNC and SDATA_OUT rise/fall times with a external load of 75 pF Note 3: SDATA_IN rise/fall times with an external load of 60 pF Note 4: Rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 5: Fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					

10.6. AC97 Interface Register List

Module Name	Base Address
AC97	0x01C21400

Register Name	Offset	Description
AC_CTL	0x00	AC97 Control Register
AC_FAT	0x04	AC97 Format Register
AC_CMD	0x08	AC97 Command Register
AC_CS	0x0C	AC97 Codec Status Register
AC_TX_FIFO	0x10	AC97 TX FIFO Register
AC_RX_FIFO	0x14	AC97 RX FIFO Register
AC_FCTL	0x18	AC97 FIFO Control Register
AC_FSTA	0x1C	AC97 FIFO Status Register
AC_INT	0x20	AC97 Interrupt Control Register
AC_ISTA	0x24	AC97 Interrupt Status Register
AC_TX_CNT	0x28	AC97 TX Counter register
AC_RX_CNT	0x2C	AC97 RX Counter register

10.7. AC97 Interface Register Description

6.10.7.1. AC97 CONTROL REGISTER

Offset: 0x00			**Register Name: AC_CTL** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:19	/	/	/
18	R	0	CS_RF CODEC Status Register FLAG 0: Empty 1: Full
17	R	0	CMD_RF CMD Register FLAG 0: Empty 1: Full

Offset: 0x00			Register Name: AC_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
16	R	0	RX_STATUS RX Transfer Status 0: PCM IN 1: MIC IN
15:10	/	/	/
9	R/W	0	RX_MODE RX MODE 0: PCM IN 1: MIC IN *Note: this bit indicate which mode will be selected when PCM IN and MIC IN slots are available simultaneity*
8	R/W	0	ASS Audio sample select with TX FIFO under run 0: sending 0 (invalid frame) 1: sending the last audio (valid frame)
7	R/W	0	TXEN 0: Disable 1: Enable
6	R/W	0	RXEN 0: Disable 1: Enable
5	R/W	0	AC-link EN 0: Disable 1: Enable(SYNC signal transfer to Codec)
4	R/W	0	GEN Globe Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
3:2	/	/	/
1	R/W	0	WARM_RST Warm reset

Offset: 0x00			Register Name: AC_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			0: Normal 1: Wake up codec from power down *Note: Self clear to "0"*
0	/	/	/

6.10.7.2. AC97 FORMAT REGISTER

Offset: 0x04			Register Name: AC_FAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/
8:7	R/W	0	TX_AUDIO_MODE TX audio mode 00: 2-channel(PCM l/r main) 01: 6-channel(PCM l/r main, l/r surround, center, AFE) 10: Reserved 11: Reserved
6	R/W	0	DRA_SLOT_SEL DRA additional slots select (available in 2-channel mode) 0: select slot 10, slot 11 1: select slot 7, slot 8
5	R/W	0	DRA_MODE DRA mode 0 : Non-DRA 1 : DRA
4	R/W	0	VRA_MODE VRA Mode 0 : Non-VRA 1 : VRA
3:2	R/W	0	TX_RES TX Audio data resolution 00: 16-bit 01: 18-bit

Offset: 0x04			Register Name: AC_FAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			10: 20-bit 11: Reserved
1:0	R/W	0	RX_RES RX Audio data resolution 00: 16-bit 01: 18-bit 10: 20-bit 11: Reserved

6.10.7.3. AC97 CODEC COMMAND REGISTER

Offset: 0x08			Register Name: AC_CMD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R/W	0	OP Read enable 0: Command write 1: Status read
22:16	R/W	0x00	CC_ADDR Codec command address
15:0	R/W	0x0000	CC Codec command data

6.10.7.4. AC97 CODEC STATUS REGISTER

Offset: 0x0C			Register Name: AC_CS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:23	/	/	/

Offset: 0x0C			Register Name: AC_CS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
22:16	R	0x00	CS_ADDR Codec status address
15:0	R	0x0000	CS Codec status data

6.10.7.5. AC97 TX FIFO REGISTER

Offset: 0x10			Register Name: AC_TXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

6.10.7.6. AC97 RX FIFO REGISTER

Offset: 0x14			Register Name: AC_RXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	RX_DATA Host can get one sample by reading this register. If in the PCM IN mode, the left channel sample data is first and then the right channel sample

6.10.7.7. AC97 FIFO CONTROL REGISTER

Offset: 0x18			Register Name: AC_FCTL Default Value: 0x0000_3078
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
17	R/W	0	FTX

Offset: 0x18			Register Name: AC_FCTL Default Value: 0x0000_3078
Bit	**Read/Write**	**Default**	**Description**
			Write “1” to flush TX FIFO, self clear to “0”
16	R/W	0	FRX Write “1” to flush RX FIFO, self clear to “0”
15:8	R/W	0x30	TXTL TX FIFO empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition Trigger Level = TXTL
7:3	R/W	0x0F	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition Trigger Level =RXTL + 1
2	R/W	0	TXIM TX FIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of AC_TXFIFO register 1: Valid data at the LSB of AC_TXFIFO register Example for 18-bits transmitted audio sample: Mode 0: FIFO_I[19:0] = {TXFIFO[31:14], 2’h0} Mode 1: FIFO_I[19:0] = {TXFIFO[17:0], 2’h0}
1:0	R/W	0	RXOM RX FIFO Output Mode(Mode 0,1,2,3) 00: Expanding “0” at LSB of AC_RXFIFO register 01: Expanding received sample sign bit at MSB of AC_RXFIFO register 10: Truncating received samples at high half-word of AC_RXFIFO register and low half-word of AC_FIFO register is filled by “0” 11: Truncating received samples at low half-word of AC_RXFIFO register and high half-word of AC_FIFO register is expanded by its sigh bit Example for 18-bits received audio sample: Mode0: RXFIFO[31:0] = {FIFO_O[19:2], 14’h0} Mode 1: RXFIFO[31:0] = {14’FIFO_O[19], FIFO_O[19:2]} Mode 2: RXFIFO[31:0] = {FIFO_O[19:4], 16’h0} Mode 3: RXFIFO[31:0] = {16’FIFO_O[19], FIFO_O[19:4]}

6.10.7.8. AC97 FIFO STATUS REGISTER

Offset: 0x1C			Register Name: AC_FSTA Default Value: 0x0000_C000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
15	R	1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>=1 word)
14:7	R	0x80	TXE_CNT TX FIFO Empty Space Word counter
6	R	0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>=1 word)
5:0	R	0	RXA_CNT RX FIFO Available Sample Word counter

6.10.7.9. AC97 INTERRUPT CONTROL REGISTER

Offset: 0x20			Register Name: AC_INT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:10	/	/	/
9	R/W	0	CODEC_GPIO_EN Codec GPIO interrupt enable 0: Disable 1: Enable
8	R/W	0	CREN Codec Ready interrupt enable 0: Disable

Offset: 0x20			Register Name: AC_INT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			1: Enable
7	R/W	0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0	RX_DRQ RX FIFO Data Available DRQ Enable When set to "1", RX FIFO DMA Request is asserted if Data is available in RX FIFO 0: Disable 1: Enable
1	R/W	0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

6.10.7.10. AC97 INTERRUPT STATUS REGISTER

Offset: 0x24			Register Name: AC_ISTA Default Value: 0x0000_0010
Bit	**Read/Write**	**Default**	**Description**
31:10	/	/	/
9	R/W	0	CODEC_GPIO_INT Codec GPIO interrupt 0: No pending IRQ 1: Codec GPIO interrupt
8	R/W	0	CR_INT Codec Ready pending Interrupt 0: No pending IRQ 1: Codec Ready Pending Interrupt Write "1" to clear this interrupt
7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No pending IRQ 1: FIFO Under run Pending Interrupt Write "1" to clear this interrupt
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Write "1" to clear this interrupt
4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write "1" to clear this interrupt or automatically clear if interrupt condition fails.
3:2	/	/	/
1	R/W	0	RXO_INT RX FIFO Overrun Pending Interrupt 0: FIFO Overrun Pending Write "1" to clear this interrupt

Offset: 0x24			Register Name: AC_ISTA Default Value: 0x0000_0010
Bit	**Read/Write**	**Default**	**Description**
0	R/W	0	RXA_INT RX FIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write “1” to clear this interrupt or automatically clear if interrupt condition fails

6.10.7.11. AC97 TX COUNTER REGISTER

Offset: 0x28			Register Name: AC_TX_CNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	TX_CNT TX Sample counter The audio sample number of writing into TX FIFO. When one sample is written by DMA or by host IO, the TX sample counter register increases by one. The TX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

6.10.7.12. AC97 RX COUNTER REGISTER

Offset: 0x2C			Register Name: AC_RX_CNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	RX_CNT RX Sample counter The audio sample number of writing into RX FIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

6.10.8. AC97 Interface Special Requirement

6.10.8.1. PIN LIST

Port Name	Width	Direction	Description
AC_BIT_CLK	1	IN	Digital Audio Serial Clock provided by Codec
AC_SYNC	1	OUT	Digital Audio Sample rate/sync
AC_MCLK	1	OUT	AC97 Codec Input Mclk
AC_SDATA_IN	1	IN	Digital Audio serial Data Input
AC_SDTA_OUT	1	OUT	Digital Audio serial Data Output

Note:BIT_CLK is provided by AC97 Codec.

6.10.8.2. AC97 CLOCK REQUIREMENT

Clock Name	Description	Requirement
apb_clk	APB bus clock	
s_clk	AC97 serial access x1 clock	24.576 MHz or 22.5792 MHz from CCU

6.11. EMAC

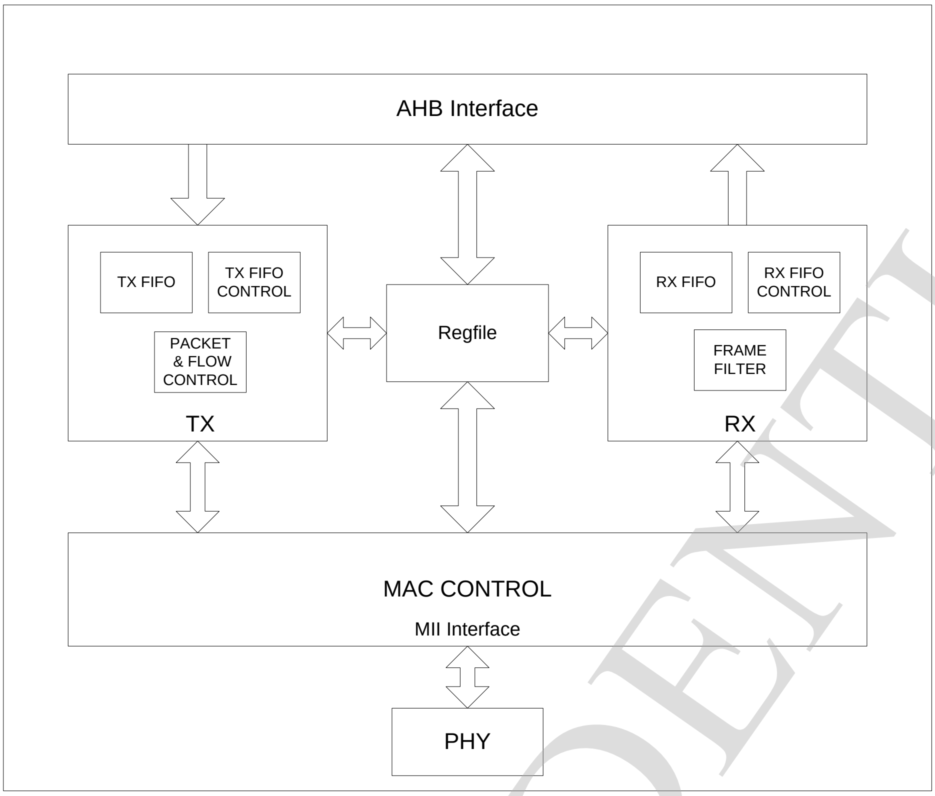
6.11.1. Overview

The Ethernet MAC Controller enables the host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M external PHY with MII interface in both full and half duplex mode. A 16KB SRAM is provided to keep continuous data transmission. Besides, the flow control and DA/SA filter are also supported in EMAC module.

The EMAC features:

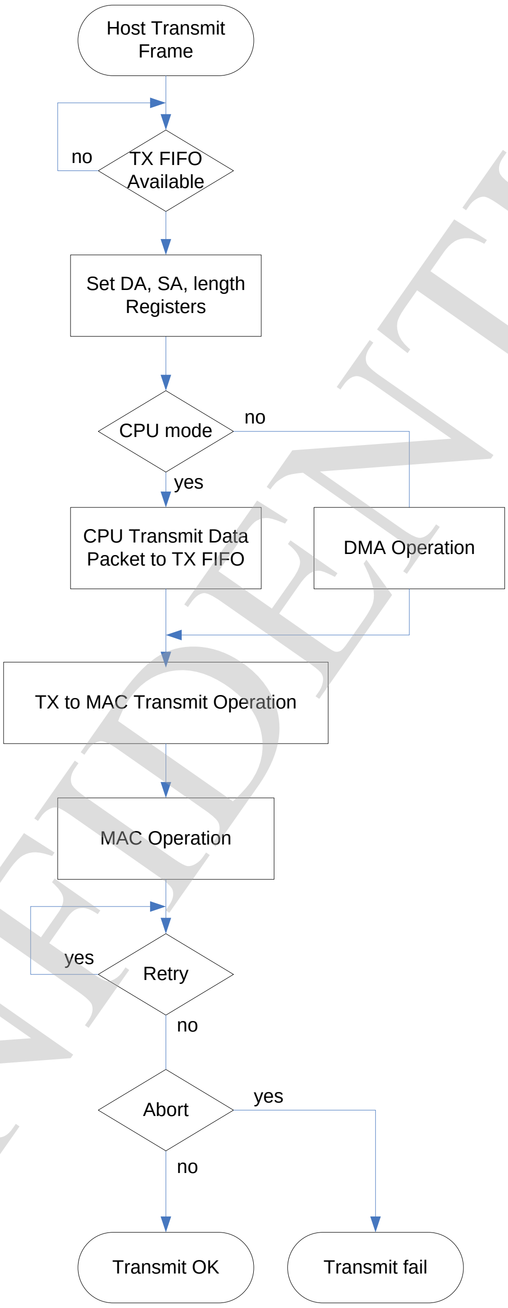
- Support industry-standard AMBA Host Bus (AHB) and fully comply with the AMBA Specification, Revision 2.0, support 32-bit Little Endian bus
- Compatible with IEEE802.3standards
- Support 10/100Mbps data rate
- Support full and half duplex operations
- Support IEEE 802.3x flow control for full-duplex operation
- Support back-pressure flow control for half-duplex operation
- Support DA/SA filter
- Support loop back operation
- Provide MII Interface for external Ethernet PHY
- 3KB FIFO for TX
- 13KB FIFO for RX

6.11.2. EMAC Block Diagram

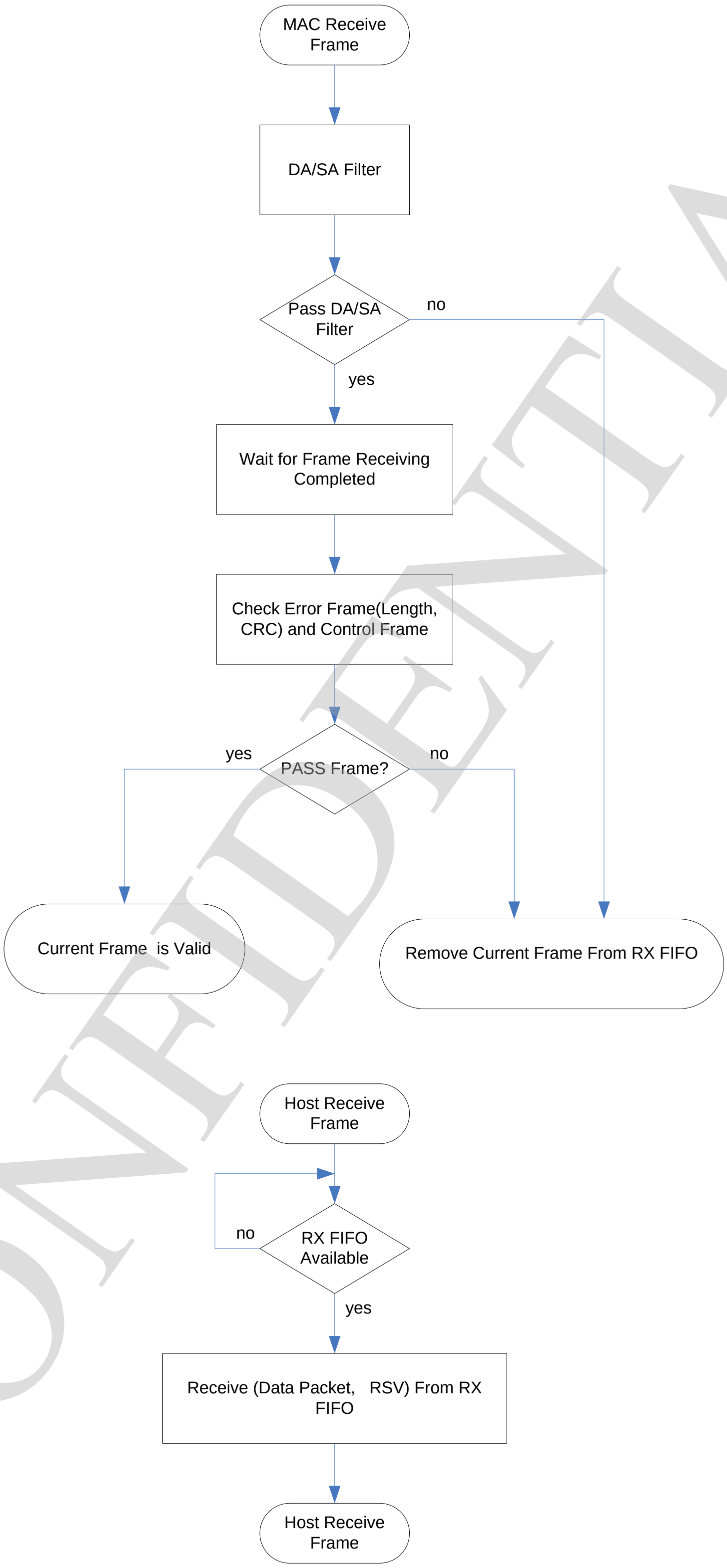


6.11.3. EMAC Operation Diagram

6.11.3.1. TX OPERATION



6.11.3.2. RX OPERATION



Each received packet has 8-byte header followed with data of the reception packet which CRC field isn't included. The format of the 8-byte header is 4Dh, 41h, 43h, 01h, PKT_SIZE low and PKT_SIZE high status low, status high,. The received packet must be WORD(32-bits) align. If there is not enough data for WORD(32-bits) align. The zero bytes are padded at the end of packet. The PKT_SIZE would count the size of useful data, not including padding bytes and 8-bytes packet header.

The 8-bytes packet header is listed below:

Index	Value	Description
BYTE0	PKT_VLD	Packet Valid Flag 0x01: packet valid 0x00: packet not valid
BYTE1	0x43	ASCII code 'C'
BYTE2	0x41	ASCII code 'A'
BYTE3	0x4d	ASCII code 'M'
BYTE4	PKT_STATUS	High byte of received packet's status
BYTE5	PKT_STATUS	Low byte of received packet's status
BYTE6	PKT_SIZE	High byte of packet size
BYTE7	PKT_SIZE	Low byte of packet size

The 2-bytes status is listed below:

Bit	Description
15	Reserved
14	Receive VLAN TYPE detected
13	Receive Unsupported Op-code
12	Receive Pause Control Frame
11	Receive Control Frame
10	Dribble Nibble
9	Broadcast Packet
8	Multicast Packet
7	Receive OK
6	Length Out of Range
5	Length Check Error
4	CRC Error
3	Receive Code Violation
2	Carrier Event Previously Seen
1	RXDV Event Previously Seen
0	Packet Previously Ignored

6.12. GMAC

6.12.1. Overview

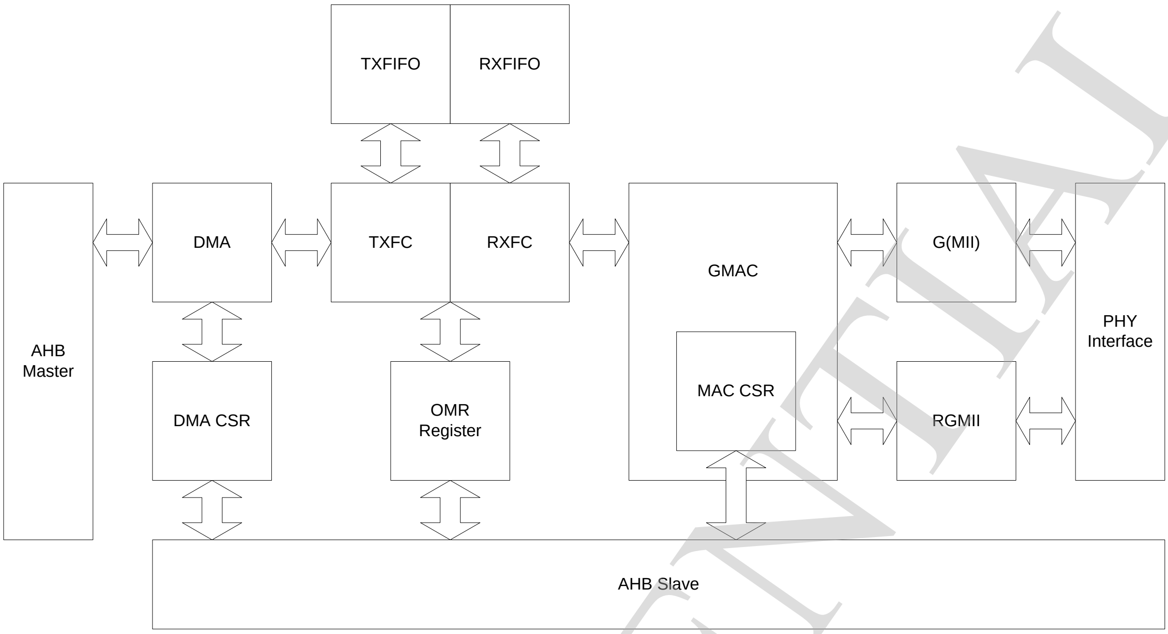
The GMAC controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M/1000M external PHY with RGMII interface in both full and half duplex mode.

The GMAC-DMA is designed for packet-oriented data transfer based on a linked list of descriptors. 4KB TXFIFO and 16KB RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are supported in this module as well.

It features:

- Support 10/100/1000-Mbps data transfer rates
- Support RGMII PHY interface
- Support both full-duplex and half-duplex operation
- Automatic CRC and pad generation controllable on a per-frame basis
- Options for Automatic Pad/CRC Stripping on receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Programmable Inter Frame Gap (40-96 bit times in steps of 8)
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Dual-buffer (ring) or linked-list (chained) descriptor chaining
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB data
- Comprehensive status report for normal operation and transfers with errors
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

6.12.2. GMAC Block Diagram



6.13. Transport Stream

6.13.1. Overview

The transport stream controller is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1.

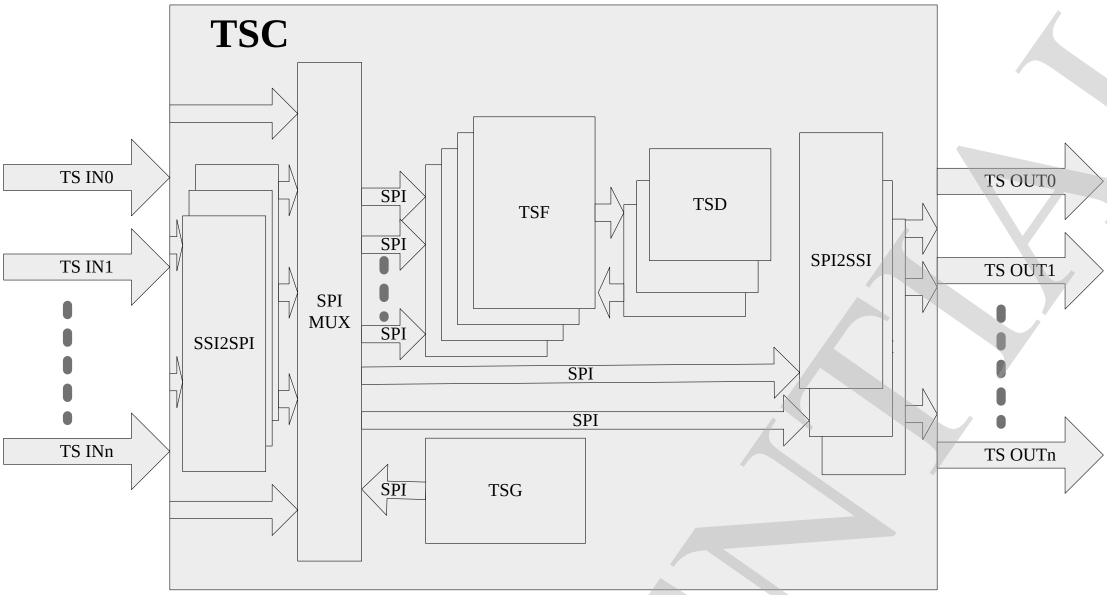
The transport stream controller receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before the Packet is stored to memory by DMA, it can be pre-processed by the Transport Stream Descrambler.

The transport stream controller can be used for almost all multimedia application cases, for example: DVB Set top Box, IPTV, Streaming-media Box, multi-media players and so on.

It features:

- Support industry-standard AMBA Host Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus.
- Support AHB 32-bit bus width
- One external SPI or SSI
- 32 channels PID filter
- Support multiple transport stream packet (188, 192, 204) formats
- Configurable SPI and SSI timing parameters
- Hardware packet synchronous byte error detection
- Hardware PCR packet detection
- Configurable SPI transport stream generator for streams in DRAM memory
- Support DMA for data transfer
- Support interrupt
- Support DVB-CSA V1.1 descrambler

6.13.2. Transport Stream Block Diagram



6.13.3. Transport Stream Controller Register List

Module Name	Base Address
TSC	0x01c04000
TSG OFFSET	0x00000040
TSF0 OFFSET	0x00000080
TSF1 OFFSET	0x00000100
TSD OFFSET	0x00000180

Register Name	Offset	Description
TSC_CTLR	TSC + 0x00	TSC Control Register
TSC_STAR	TSC + 0x04	TSC Status Register
TSC_PCTLR	TSC + 0x10	TSC Port Control Register
TSC_PPARR	TSC + 0x14	TSC Port Parameter Register
TSC_TSFMUXR	TSC + 0x20	TSC TSF Input Multiplex Control Register
TSC_OUTMUXR	TSC + 0x28	TSC Port Output Multiplex Control Register

TSG_CTLR	TSG + 0x00	TSG Control Register
TSG_PPR	TSG + 0x04	TSG Packet Parameter Register
TSG_STAR	TSG + 0x08	TSG Status Register
TSG_CCR	TSG + 0x0c	TSG Clock Control Register
TSG_BBAR	TSG + 0x10	TSG Buffer Base Address Register
TSG_BSZR	TSG + 0x14	TSG Buffer Size Register
TSG_BPR	TSG + 0x18	TSG Buffer Pointer Register
TSF_CTLR	TSF + 0x00	TSF Control Register
TSF_PPR	TSF + 0x04	TSF Packet Parameter Register
TSF_STAR	TSF + 0x08	TSF Status Register
TSF_DIER	TSF + 0x10	TSF DMA Interrupt Enable Register
TSF_OIER	TSF + 0x14	TSF Overlap Interrupt Enable Register
TSF_DISR	TSF + 0x18	TSF DMA Interrupt Status Register
TSF_OISR	TSF + 0x1c	TSF Overlap Interrupt Status Register
TSF_PCRCR	TSF + 0x20	TSF PCR Control Register
TSF_PCRDR	TSF + 0x24	TSF PCR Data Register
TSF_CENR	TSF + 0x30	TSF Channel Enable Register
TSF_CPER	TSF + 0x34	TSF Channel PES Enable Register
TSF_CDER	TSF + 0x38	TSF Channel Descramble Enable Register
TSF_CINDR	TSF + 0x3c	TSF Channel Index Register
TSF_CCTLR	TSF + 0x40	TSF Channel Control Register
TSF_CSTAR	TSF + 0x44	TSF Channel Status Register
TSF_CCWIR	TSF + 0x48	TSF Channel CW Index Register
TSF_CPIDR	TSF + 0x4c	TSF Channel PID Register
TSF_CBBAR	TSF + 0x50	TSF Channel Buffer Base Address Register
TSF_CBSZR	TSF + 0x54	TSF Channel Buffer Size Register
TSF_CBWPR	TSF + 0x58	TSF Channel Buffer Write Pointer Register
TSF_CBRPR	TSF + 0x5c	TSF Channel Buffer Read Pointer Register
TSD_CTLR	TSD + 0x00	TSD Control Register
TSD_STAR	TSD + 0x04	TSD Status Register
TSD_CWIR	TSD + 0x1c	TSD Control Word Index Register
TSD_CWR	TSD + 0x20	TSD Control Word Register

6.13.4. Transport Stream Register Description

6.13.4.1. TSC CONTROL REGISTER

Offset: 0x00			Register Name: TSC_CTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

6.13.4.2. TSC STATUS REGISTER

Offset: 0x04			Register Name: TSC_STAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

6.13.4.3. TSC PORT CONTROL REGISTER

Offset: 0x10			Register Name: TSC_PCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:17	/	/	/
16	R/W	0	TSOutPort0Ctrl TS Output Port0 Control 0 – SPI 1 – SSI
15:2	/	/	/
1	R/W	0	TSInPort1Ctrl TS Input Port1 Control 0 – SPI 1 – SSI
0	R/W	0	TSInPort0Ctrl TS Input Port0 Control

Offset: 0x10			Register Name: TSC_PCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			0 – SPI 1 – SSI

6.13.4.4. TSC PORT PARAMETER REGISTER

Offset: 0x14			Register Name: TSC_PPARR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	R/W	0x00	TSOutPort0Par TS Output Port0 Parameters <table><tr><td>Bit</td><td>Definition</td></tr><tr><td>7:5</td><td>/</td></tr><tr><td>4</td><td>SSI data order 0: MSB first for one byte data 1: LSB first for one byte data</td></tr><tr><td>3</td><td>CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing</td></tr><tr><td>2</td><td>ERROR signal polarity 0: High level active 1: Low level active</td></tr><tr><td>1</td><td>DVALID signal polarity 0: High level active 1: Low level active</td></tr><tr><td>0</td><td>PSYNC signal polarity 0: High level active 1: Low level active</td></tr></table>
23:16	/	/	/
15:8	R/W	0x00	TSInPort1Par TS Input Port1 Parameters <table><tr><td>**Bit**</td><td>**Definition**</td></tr><tr><td>7:5</td><td>Reserved</td></tr><tr><td>4</td><td>SSI data order 0: MSB first for one byte data 1: LSB first for one byte data</td></tr><tr><td>3</td><td>CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing</td></tr><tr><td>2</td><td>ERROR signal polarity 0: High level active 1: Low level active</td></tr></table>

<table>
<tr><td colspan="3">Offset: 0x14</td><td>Register Name: TSC_PPARR
Default Value: 0x0000_0000</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td><table>
<tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr>
<tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr>
</table></td></tr>
<tr><td>7:0</td><td>R/W</td><td>0x00</td><td>TSInPort0Par
TS Input Port0 Parameters<table>
<tr><td>Bit</td><td>Definition</td></tr>
<tr><td>7:5</td><td>Reserved</td></tr>
<tr><td>4</td><td>SSI data order
0: MSB first for one byte data
1: LSB first for one byte data</td></tr>
<tr><td>3</td><td>CLOCK signal polarity
0 : Rise edge capturing
1: Fall edge capturing</td></tr>
<tr><td>2</td><td>ERROR signal polarity
0: High level active
1: Low level active</td></tr>
<tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr>
<tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr>
</table></td></tr>
</table>

6.13.4.5. TSC TSF INPUT MULTIPLEX CONTROL REGISTER

<table>
<tr><td colspan="3">Offset: 0x20</td><td>Register Name: TSC_TSFMUXR
Default Value: 0x0000_0000</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td>31:8</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>7:4</td><td>R/W</td><td>0x0</td><td>TSF1InputMuxCtrl
TSF1 Input Multiplex Control
0x0 –Data from TSG
0x1 –Data from TS IN Port0
0x2 –Data from TS IN Port1
Others – Reserved</td></tr>
<tr><td>3:0</td><td>R/W</td><td>0x0</td><td>TSF0InputMuxCtrl</td></tr>
</table>

Offset: 0x20			Register Name: TSC_TSFMUXR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			TSF0 Input Multiplex Control 0x0 –Data from TSG 0x1 –Data from TS IN Port0 0x2 –Data from TS IN Port1 Others – Reserved

6.13.4.6. TSC PORT OUTPUT MULTIPLEX CONTROL REGISTER

Offset: 0x28			Register Name: TSC_TSFMUXR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
3:0	R/W	0x0	TSPortOutputMuxCtrl TS Port Output Multiplex Control 0x0 – Data from TSG 0x1 –Data from TS IN Port0 0x2 –Data from TS IN Port1 Others – Reserved

6.13.4.7. TSG CONTROL AND STATUS REGISTER

Offset: TSG+0x00			Register Name: TSG_CSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:24	R	0	TSGSts Status for TS Generator 0: IDLE state 1: Running state 2: PAUSE state Others: Reserved

Offset: TSG+0x00			Register Name: TSG_CSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
23:10	/	/	/
9	R/W	0	TSGLBufMode Loop Buffer Mode When set to '1', the TSG external buffer is in loop mode.
8	R/W	0	TSGSyncByteChkEn Sync Byte Check Enable Enable/ Disable check SYNC byte fro receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is receiver, TS Generator would come into PAUSE state. If the correspond interrupt is enable, the interrupt would happen.
7:3	/	/	/
2	R/W	0	TSGPauseBit Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finishing this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0	TSGStopBit Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finishing this operation, this bit will clear to zero by hardware.
0	R/W	0	TSGStartBit Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

6.13.4.8. TSG PACKET PARAMETER REGISTER

Offset: TSG+0x04	Register Name: TSG_PPR Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:24	/	/	/
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position Notes: This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes 1: 192 bytes 2: 204 bytes 3: Reserved

6.13.4.9. TSG INTERRUPT ENABLE AND STATUS REGISTER

Offset: TSG+0x08			Register Name: TSG_IESR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19	R/W	0	TSGEndIE TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0	TSGFFIE TS Generator (TSG) Full Finish Interrupt Enable 0: Disable

Offset: TSG+0x08			Register Name: TSG_IESR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			1: Enable
17	R/W	0	TSGHFIE TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0	TSGErrSyncByteIE TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0	TSGEndSts TS Generator (TSG) End Status Write '1' to clear.
2	R/W	0	TSGFFSts TS Generator (TSG) Full Finish Status Write '1' to clear.
1	R/W	0	TSGHFSts TS Generator (TSG) Half Finish Status Write '1' to clear.
0	R/W	0	TSGErrSyncByteSts TS Generator (TSG) Error Sync Byte Status Write '1' to clear.

6.13.4.10. TSG CLOCK CONTROL REGISTER

Offset: TSG+0x0c			Register Name: TSG_CCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x0	TSGCDF_N TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSGCDF_D

Offset: TSG+0x0c			Register Name: TSG_CCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(16*(D+1)). Fi is the input special clock of TSC, and D must not less than N.

6.13.4.11. TSG BUFFER BASE ADDRESS REGISTER

Offset: TSG+0x10			Register Name: TSG_BBAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	RW	0x0	TSGBufBase Buffer Base Address This value is a start address of TSG buffer. Note: This value should be 4-word (16 Bytes) align, and the lowest 4-bit of this value should be zero.

6.13.4.12. TSG BUFFER SIZE REGISTER

Offset: TSG+0x14			Register Name: TSG_BSZR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	TSGBufSize Data Buffer Size for TS Generator It is in byte unit. The size should be 4-word (16 Bytes) align, and the lowest 4 bits should be zero.

6.13.4.13. TSG BUFFER POINTER REGISTER

Offset: TSG+0x18			Register Name: TSG_BPR Default Value: 0x1fff_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R	0	TSGBufPtr Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

6.13.4.14. TSF CONTROL AND STATUS REGISTER

Offset: TSF+0x00			Register Name: TSF_CSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2	R/W	0	TSF Enable 0: Disable TSF Input 1: Enable TSF Input
1	/	/	/
0			TSFGSR TSF Global Soft Reset A software writing '1' will reset all status and state machine of TSF. And it's cleared by hardware after finish reset. A software writing '0' has no effect.

6.13.4.15. TSF PACKET PARAMETER REGISTER

Offset: TSF+0x04			Register Name: TSF_PPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	R/W	0	LostSyncThd Lost Sync Packet Threshold It is used for packet sync lost by checking the value of sync

Offset: TSF+0x04			Register Name: TSF_PPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			byte.
27:24	R/W	0	SyncThd Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0	SyncMthd Packet Sync Method 0: By PSYNC signal 1: By sync byte 2: By both PSYNC and Sync Byte 3: Reserved
7	R/W	0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position Notes: This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes 1: 192 bytes 2: 204 bytes 3: Reserved

6.13.4.16. TSF INTERRUPT ENABLE AND STATUS REGISTER

Offset: TSF+0x08	Register Name: TSF_IESR Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:20	/	/	/
19	R/W	0	TSFFOIE TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable
18	R/W	0	TSFPPDIE TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable
17	R/W	0	TSFCOIE TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable 1: Enable
16	R/W	0	TSFCDIE TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0	TSFFOIS TS PID Filter (TSF) Internal FIFO Overrun Status Write '1' to clear.
2	R/W	0	TSFPPDIS TS PCR Packet Found Status When it is '1', one TS PCR Packet is found. Write '1' to clear.
1	R	0	TSFCOIS TS PID Filter (TSF) Channel Overlap Status It is global status for 16 channel. It would clear to zero after all channels status bits are clear.
0	R	0	TSFCDIS TS PID Filter (TSF) Channel DMA status It is global status for 16 channel. It would clear to zero after all channels status bits are clear.

6.13.4.17. TSF DMA INTERRUPT ENABLE REGISTER

Offset: TSF+0x10			Register Name: TSF_DIER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DMAIE DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

6.13.4.18. TSF OVERLAP INTERRUPT ENABLE REGISTER

Offset: TSF+0x14			Register Name: TSF_OIER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	OLPIE Overlap Interrupt Enable Overlap interrupt enable bits for channel 0~31.

6.13.4.19. TSF DMA INTERRUPT STATUS REGISTER

Offset: TSF+0x18			Register Name: TSF_DISR Default Value: 0x3FFF_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DMAIS DMA Interrupt Status DMA interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing ‘1’. When both these bits and the corresponding DMA Interrupt Enable bits set, the TSF interrupt will generate.

6.13.4.20. TSF OVERLAP INTERRUPT STATUS REGISTER

Offset: TSF+0x1c			Register Name: TSF_OISR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	OLPIS Overlap Interrupt Status Overlap interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

6.13.4.21. TSF PCR CONTROL REGISTER

Offset: TSF+0x20			Register Name: TSF_PCRCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:17	/	/	/
16	R/W	0	PCRDE PCR Detecting Enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0	PCRCIND Channel Index m for Detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0	PCRLSB PCR Contest LSB 1 bit PCR[0]

6.13.4.22. TSF PCR DATA REGISTER

Offset: TSF+0x24	Register Name: TSF_PCRDR Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:0	R	0	PCRMSB PCR Data High 32 bits PCR[33:1]

6.13.4.23. TSF CHANNEL ENABLE REGISTER

Offset: TSF+0x30			Register Name: TSF_CENR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	FilterEn Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, internal status of the corresponding filter channel will be reset.

6.13.4.24. TSF CHANNEL PES ENABLE REGISTER

Offset: TSF+0x34			Register Name: TSF_CPER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	PESEn PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

6.13.4.25. TSF CHANNEL DESCRAMBLE ENABLE REGISTER

Offset: TSF+0x38			Register Name: TSF_CDER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DescEn Descramble Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

6.13.4.26. TSF CHANNEL INDEX REGISTER

Offset: TSF+0x3c			Register Name: TSF_CINDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:5	/	/	/
4:0	R/W	0x0	CHIND Channel Index This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is 0x40~0x7f.

6.13.4.27. TSF CHANNEL CONTROL REGISTER

Offset: TSF+0x40			Register Name: TSF_CCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

6.13.4.28. TSF CHANNEL STATUS REGISTER

Offset: TSF+0x44			Register Name: TSF_CSTAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

6.13.4.29. TSF CHANNEL CW INDEX REGISTER

Offset: TSF+0x48			Register Name: TSF_CCWIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2:0	R/W	0x0	CWIND Related Control Word Index Index to the control word used by this channel when Descramble Enable of this channel enable. This value is useless when the corresponding Descramble Enable is '0'.

6.13.4.30. TSF CHANNEL PID REGISTER

Offset: TSF+0x4c			Register Name: TSF_CPIDR Default Value: 0x1fff_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x1fff	PIDMSK Filter PID Mask for Channel
15:0	R/W	0x0	PIDVAL Filter PID value for Channel

6.13.4.31. TSF CHANNEL BUFFER BASE ADDRESS REGISTER

Offset: TSF+0x50			Register Name: TSF_CBBAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	TSFBufBAddr Data Buffer Base Address for Channel It is 4-word (16Bytes) align address. The LSB four bits should be zero.

6.13.4.32. TSF CHANNEL BUFFER SIZE REGISTER

Offset: TSF+0x54			Register Name: TSF_CBSZR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:24	R/W	0	CHDMAIntThd DMA Interrupt Threshold for Channel The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 0: 1/2 data buffer packet size 1: 1/4 data buffer packet size 2: 1/8 data buffer packet size 3: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0	CHBufPktSz Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 bytes. The maximum buffer size is 2MB. This size should be 4-word (16 Bytes) aligned. The LSB four bits should be zero.

6.13.4.33. TSF CHANNEL BUFFER WRITE POINTER REGISTER

Offset: TSF+0x58			Register Name: TSF_CBWPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20:0	R/W	0	BufWrPtr Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by software during the corresponding channel is enable.

6.13.4.34. TSF CHANNEL BUFFER READ POINTER REGISTER

Offset: TSF+0x5c			Register Name: TSF_CBRPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20:0	R/W	0	BufRdPtr Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is read.

6.13.4.35. TSD CONTROL REGISTER

Offset: TSD+0x00			Register Name: TSD_CTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	
1:0	R/W	0x0	DescArith Descramble Arithmetic 00: DVB CSA V1.1 Others: Reserved

6.13.4.36. TSD STATUS REGISTER

Offset: TSD+0x04			Register Name: TSD_STAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

6.13.4.37. TSD CONTROL WORD INDEX REGISTER

Offset: TSD+0x1c			Register Name: TSD_CWIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
6:4	R/W	0x0	CWI Control Word Index This value is the Control index for Control word access. Range is from 0x00 to 0x7.
3:2	/	/	/
1:0	R/W	0x0	CWII Control Word Internal Index 0 – Odd Control Word Low 32-bit, OCW[31:0]; 1 – Odd Control Word High 32-bit, OCW[63:32]; 2 – Even Control Word Low 32-bit, ECW[31:0]; 3 – Even Control Word High 32-bit, ECW[63:0];

6.13.4.38. TSD CONTROL WORD REGISTER

Offset: TSD+0x20			Register Name: TSD_CWR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	CWD Content of Control Word corresponding to the TSD_CWIR

Offset: TSD+0x20			Register Name: TSD_CWR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			value

13.5. Transport Stream Clock Requirement

Clock Name	Description	Requirement
HCLK	AHB bus clock	
TS_CLK	Clock of TS Stream in SPI mode	
TSC_CLK	TS serial clock from CCU	TSC_CLK >=16*TS_CLK

6.14. Smart Card Reader

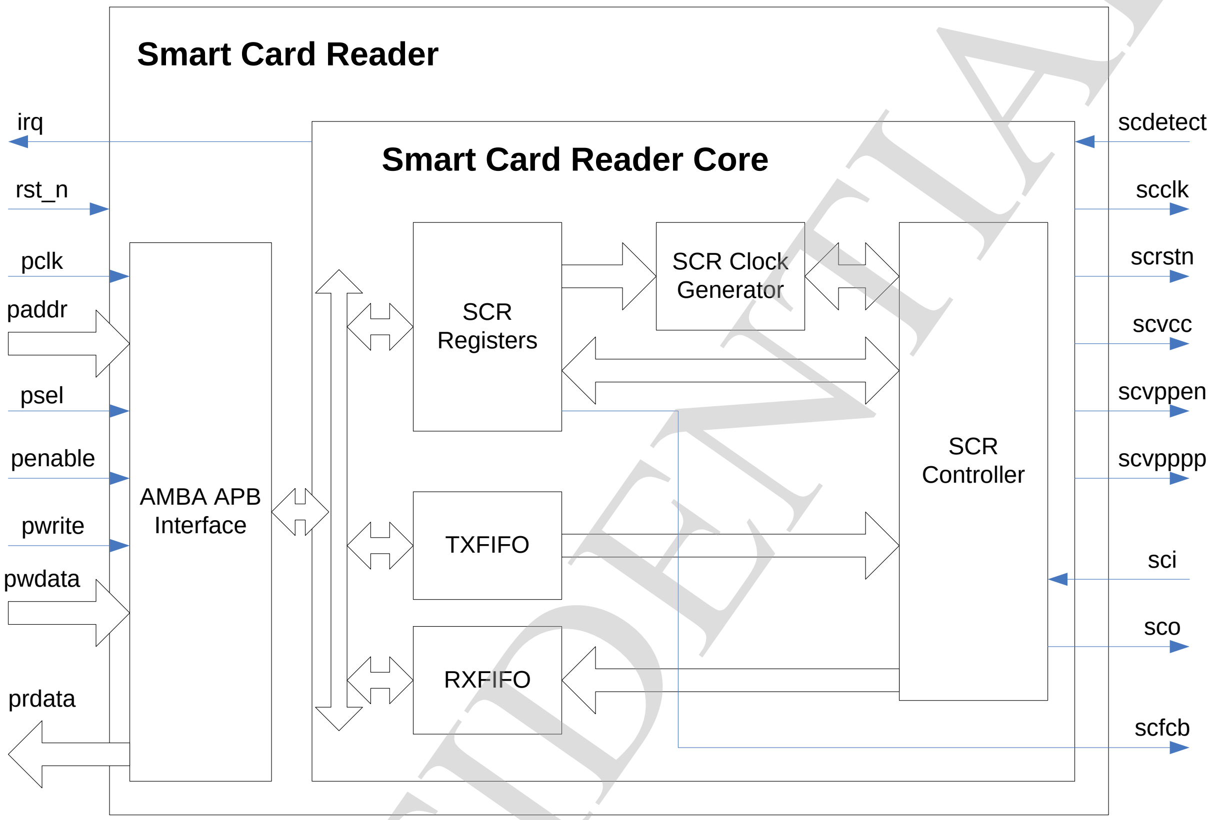
6.14.1. Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and smart card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, and data transfer, etc.

It features:

- Support APB slave interface for easy integration with AMBA-based host systems
- Support the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Perform functions needed for complete smart card sessions
- Support adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Support commonly used communication protocols:
  T=0: for asynchronous half-duplex character transmission
  T=1: for asynchronous half-duplex block transmission
- Support FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Support configurable timing functions:Smart card activation time, Smart card reset time, Guard time, Timeout timers
- Support synchronous and other non-ISO 7816 and non-EMV cards

6.14.2. Smart Card Reader Block Diagram



6.14.3. Smart Card Reader Timing Diagram

Please refer ISO/IEC 7816 and EMV2000 Specification.

6.14.4. Smart Card Reader Register List

Module Name	Base Address

Module Name	Base Address
SCR0	0x01C2C400

Register Name	Offset	Description
SCR_CSR	0x000	Smart Card Reader Control and Status Register
SCR_INTEN	0x004	Smart Card Reader Interrupt Enable Register 1
SCR_INTST	0x008	Smart Card Reader Interrupt Status Register 1
SCR_FCSR	0x00c	Smart Card Reader FIFO Control and Status Register
SCR_FCNT	0x010	Smart Card Reader RX and TX FIFO Counter Register
SCR_RPT	0x014	Smart Card Reader RX and TX Repeat Register
SCR_DIV	0x018	Smart Card Reader Clock and Baud Divisor Register
SCR_LTIM	0x01c	Smart Card Reader Line Time Register
SCR_CTIM	0x020	Smart Card Reader Character Time Register
SCR_LCTLR	0x030	Smart Card Reader Line Control Register
SCR_FIFO	0x100	Smart Card Reader RX and TX FIFO Access Point

6.14.5. Smart Card Reader Register Description

6.14.5.1. SMART CARD READER CONTROL AND STATUS REGISTER

Offset: 0x0000			**Register Name: SCR_CSR** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
31	R	0	SCDET Smart Card Detected This bit is set to '1' when the *scdetect* input is active at least for a debounce time.
30	/	/	/
24	R/W	0	SCDETPOL Smart Card Detect Polarity This bit set polarity of *scdetect* signal.

Offset: 0x0000			Register Name: SCR_CSR Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
			0: Low Active 1: High Active
23:22	R/W	0	Protocol Selection (PTLSEL) 0x0 – T=0. 0x1 – T=1, no character repeating and no guard time is used when T=1 protocol is selected. 0x2 – Reserved 0x3 – Reserved
21	R/W	0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
20	R/W	0	TSRXE TS Receive Enable When set to '1', the TS character (the first ATR character) will be store in RXFIFO during card session.
19	R/W	0	CLKSTPPOL Clock Stop Polarity The value of the *scclk* output during the clock stop state.
18	R/W	0	PECRXE Parity Error Character Receive Enable Enables storage of the characters received with wrong parity in RX FIFO.
17	R/W	0	MSBF MSB First When high, inverse bit ordering convention (msb to lsb) is used.
16	R/W	0	DATAPOL Data Plorarity When high, inverse level convention is used (A='1', Z='0').
15:12	/	/	/
11	R/W	0	DEACTDeactivation. Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
10	R/W	0	ACT Activation. Setting of this bit initializes the activation sequence.

Offset: 0x0000			Register Name: SCR_CSR Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
			When the activation is finished, the ACT bit is automatically cleared.
9	R/W	0	WARMRST Warm Reset Command. Writing '1' to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
8	R/W	0	CLKSTOP Clock Stop. When this bit is asserted and the smart card I/O line is in 'Z' state, the SCR core stops driving of the smart card clock signal after the CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is deasserted. New character transmission can be started after CLKSTARTDELAY time. The expiration of both times is signaled by the CLKSTOPRUN bit in the interrupt registers.
7:3	/	/	Reserved
2	R/W	0	GINTEN Global Interrupt Enable. When high, IRQ output assertion is enabled.
1	R/W	0	RXEN Receiving Enable. When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
0	R/W	0	TXEN Transmission Enable. When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card.

6.14.5.2. SMART CARD READER INTERRUPT ENABLE REGISTER

Offset: 0x0004			Register Name: SCR_INTEN Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R/W	0	SCDEA Smart Card Deactivation Interrupt Enable.

Offset: 0x0004			Register Name: SCR_INTEN Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
22	R/W	0	SCACT Smart Card Activation Interrupt Enable.
21	R/W	0	SCINS Smart Card Inserted Interrupt Enable.
20	R/W	0	SCREM Smart Card Removed Interrupt Enable.
19	R/W	0	ATRDONE ATR Done Interrupt Enable.
18	R/W	0	ATRFAIL ATR Fail Interrupt Enable.
17	R/W	0	C2CFULL Two Consecutive Characters Limit Interrupt Enable.
16	R/W	0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt Enable.
15:13	/	/	/
12	R/W	0	RXPERR RX Parity Error Interrupt Enable.
11	R/W	0	RXDONE RX Done Interrupt Enable.
10	R/W	0	RXFIFOTHD RX FIFO Threshold Interrupt Enable.
9	R/W	0	RXFIFOFULL RX FIFO Full Interrupt Enable.
8	/	/	/
7:5	/	/	/
4	R/W	0	TXPERR TX Parity Error Interrupt Enable.
3	R/W	0	TXDONE TX Done Interrupt Enable.
2	R/W	0	TXFIFOTHD TX FIFO Threshold Interrupt Enable.
1	R/W	0	TXFIFOEMPTY

Offset: 0x0004			Register Name: SCR_INTEN Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
			TX FIFO Empty Interrupt Enable.
0	R/W	0	TXFIFODONE TX FIFO Done Interrupt Enable.

6.14.5.3. SMART CARD READER INTERRUPT STATUS REGISTER

This 16-bit register provides information about the state of each interrupt bit. You can clear the register bits individually by writing '1' to a bit you intend to clear.

Offset: 0x0008			Register Name: SCR_INTST Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R/W	0	SCDEA Smart Card Deactivation Interrupt. When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete.
22	R/W	0	SCACT Smart Card Activation Interrupt. When enabled, this interrupt is asserted after the Smart Card activation sequence is complete.
21	R/W	0	SCINS Smart Card Inserted Interrupt. When enabled, this interrupt is asserted after the smart card insertion.
20	R/W	0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal.
19	R/W	0	ATRDONE ATR Done Interrupt. When enabled, this interrupt is asserted after the ATR sequence is successfully completed.
18	R/W	0	ATRFAIL ATR Fail Interrupt. When enabled, this interrupt is asserted if the ATR sequence fails.
17	R/W	0	C2CFULL Two Consecutive Characters Limit Interrupt. When enabled, this interrupt is asserted if the time between two consecutive

Offset: 0x0008			Register Name: SCR_INTST Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
			characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.
16	R/W	0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt. When enabled, this interrupt is asserted in two cases: When the smart card clock is stopped. When the new character can be started after the clock restart. To distinguish between the two interrupt cases, we recommend reading the CLKSTOP bit in SCR_CTRL1 register.
15:13	/	/	/
12	R/W	0	RXPERR RX Parity Error Interrupt. When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used.
11	R/W	0	RXDONE RX Done Interrupt. When enabled, this interrupt is asserted after a character was received from the Smart Card.
10	R/W	0	RXFIFOTHD RX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
9	R/W	0	RXFIFOFULL RX FIFO Full Interrupt. When enabled, this interrupt is asserted if the RX FIFO is filled up.
8:5	/	/	/
4	R/W	0	TXPERR TX Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard time after the character transmission was repeated TXREPEAT times or T=1 protocol is used.
3	R/W	0	TXDONE TX Done Interrupt. When enabled, this interrupt is asserted after one character was transmitted to the smart card.

Offset: 0x0008			Register Name: SCR_INTST Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
2	R/W	0	TXFIFOTHD TX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.
1	R/W	0	TXFIFOEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out.
0	R/W	0	TXFIFODONE TX FIFO Done Interrupt. When enabled, this interrupt is asserted after all bytes from TX FIFO ware transferred to the Smart Card.

6.14.5.4. SMART CARD READER FIFO CONTROL AND STATUS REGISTER

Offset: 0x000c			Register Name: SCR_FCSR Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:11	/	/	/
10	R/W	0	RXFIFOFLUSH Flush RX FIFO. RX FIFO is flushed, when '1' is written to this bit.
9	R	0	RXFIFOFULL RX FIFO Full.
8	R	1	RXFIFOEMPTY RX FIFO Empty.
7:3	/	/	/
2	R/W	0	TXFIFOFLUSH Flush TX FIFO. TX FIFO is flushed, when '1' is written to this bit.
1	R	0	TXFIFOFULL TX FIFO Full.
0	R	1	TXFIFOEMPTY TX FIFO Empty.

6.14.5.5. SMART CARD READER FIFO COUNT REGISTER

Offset: 0x0010			Register Name: SCR_FIFOCNT Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:24	R/W	0	RXFTH RX FIFO Threshold These bits set the interrupt threshold of RX FIFO. The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold.
23:16	R/W	0	TXFTH TX FIFO Threshold These bits set the interrupt threshold of TX FIFO. The interrupt is asserted when the number of bytes in TX FIFO is equal to or less than the threshold.
15:8	R	0	RXFCNT RX FIFO Counter These bits provide the number of bytes stored in the RXFIFO.
7:0	R	0	TXFCNT TX FIFO Counter These bits provide the number of bytes stored in the TXFIFO.

6.14.5.6. SMART CARD READER REPEAT CONTROL REGISTER

Offset: 0x0014			Register Name: SCR_REPEAT Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
15:8	/	/	/
7:4	R/W	0	RXRPT RX Repeat This is a 4-bit register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the error signal during the guard time.
3:0	R/W	0	TXRPT

Offset: 0x0014			Register Name: SCR_REPEAT Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
			TX Repeat This is a 4-bit register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guard time.

6.14.5.7. SMART CARD READER CLOCK DIVISOR REGISTER

Offset: 0x0018			Register Name: SCR_CLKDIV Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0	BAUDDIV Baud Clock Divisor. This 16-bit register defines the divisor value used to generate the Baud Clock impulses from the system clock.
15:0	R/W	0	SCCDIV Smart Card Clock Divisor. This 16-bit register defines the divisor value used to generate the Smart Card Clock from the system clock. is the frequency of Smart Card Clock Signal. is the frequency of APB Clock.

6.14.5.8. SMART CARD READER LINE TIME REGISTER

Offset: 0x001c			Register Name: SCR_LTIM Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0	ATR ATR Start Limit. This 16-bit register defines the maximum time

Offset: 0x001c			Register Name: SCR_LTIM Default Value: 0x00000000
Bit	Read/Write	Default	Description
			between the rising edge of the *scrstn* signal and the start of ATR response. ATR Start Limit = 128* ATR*.
15:8	R/W	0	RST Reset Duration. This 16-bit register sets the duration of the Smart Card reset sequence. This value is same for the cold and warm reset. Cold/Warm Reset Duration = 128* RST*.
7:0	R/W	0	ACT Activation/Deactivation Time. This 16-bit register sets the duration of each part of the activation and deactivation sequence. Activation/Deactivation Duration = 128* ACT *. is the Smart Card Clock Cycle.

6.14.5.9. SMART CARD READER CHARACTER TIME REGISTER

Offset: 0x0020			Register Name: SCR_CTIM Default Value: 0x00000000
Bit	Read/Write	Default	Description
31:16	R/W	0	CHARLIMIT Character Limit. This 16-bit register sets the maximum time between the leading edges of two consecutive characters. The value is ETUs.
15:8	/	/	/
7:0	R/W	0	GUARDTIME Character Guard time. This 8-bit register sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in ETUs. The parity error is besides signaled during the guard time.

6.14.5.10. SMART CARD READER LINE CONTROL REGISTER

This register provides direct access to smart card pads without serial interface assistance. You can use this register feature with synchronous and any other non-ISO 7816 and non-EMV cards.

Offset: 0x0030			Register Name: SCR_PAD Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	DSCVPPPP Direct Smart Card Vpp Pause/Prog. It provides direct access to SCVPPPP output.
6	R/W	0	DSCVPPEN Direct Smart Card Vpp Enable. It provides direct access to SCVPPEN output.
5	R/W	0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSVPPEN and DSVPPPP signals during activation and deactivation sequence.
4	R/W	0	DSCVCC Direct Smart Card VCC. When DIRACCPADS='1', the DSCVCC bit provides direct access to SCVCC pad.
3	R/W	0	DSCRST Direct Smart Card Clock. When DIRACCPADS='1', the DSCRST bit provides direct access to SCRST pad.
2	R/W	0	DSCCLK Direct Smart Card Clock. When DIRACCPADS='1', the DSCCLK bit provides direct access to SCCLK pad.
1	R/W	0	DSCIO Direct Smart Card Input/Output. When DIRACCPADS='1', the DSCIO bit provides direct access to SCIO pad.
0	R/W	0	DIRACCPADS Direct Access to Smart Card Pads. When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

6.14.5.11. SMART CARD READER FIFO DATA REGISTER

Offset: 0x0100	Register Name: SCR_FIFO Default Value: 0x00000000

Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	FIFO_DATA This 8-bit register provides access to the RX and TX FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer.

6.14.6.Smart Card Reader Special Requirement

CLOCK GENERATOR

The Clock Generator generates the Smart Card Clock signal and the Baud Clock Impulse signal, used in timing the Smart Card Reader.

The Smart Card Clock signal is used as the main clock for the smart card. Its frequency can be adjusted using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock. The SCCLK frequency is given by the following equation:

$$f_{scclk} = \frac{f_{sysclk}}{2*(SCCDIV+1)}$$

-- Smart Card Clock Frequency

-- System Clock (PCLK) Frequency

The Baud Clock Impulse signal is used to transmit and receive serial between the Smart Card Reader and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV). The value is used to divide the system clock. The BUAD rate is given by the following equation:

$$BAUD = \frac{f_{sysclk}}{2*(BAUDDIV+1)}$$

-- Baud rate of the data stream between Smart Card and Reader

The duration of one bit, Elementary Time Unit (ETU), is defined in the ISO/IEC 7816-3 specification. During the first answer to reset response after the cold reset, the initial ETU must be equal to 372 Smart Card Clock Cycles.

$$\frac{1}{BAUD} = ETU = \frac{372}{f_{scclk}}$$

In this case, the BAUDDIV should be

.

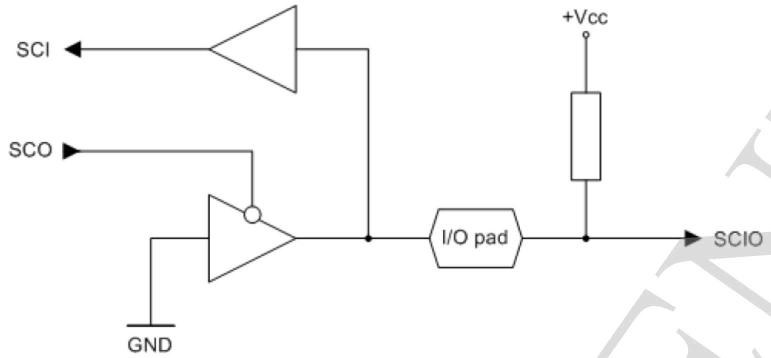
$$BAUDDIV = \frac{372*f_{sysclk}}{2*f_{scclk}} - 1 = 372*(SCCDIV+1) - 1$$

After the ATR is completed, the ETU can be changed according to Smart Card abilities.

$$\frac{1}{BAUD} = ETU = \frac{F}{D} * \frac{1}{f_{scclk}}$$

Parameters F and D are defined in the ISO/IEC 7816-3 Specification.

6.14.7. SCIO Pad Configuration



6.15. SATA Host

15.1. Overview

The SATA/AHCI Interface implements the Serial Advanced Technology Attachment (SATA) storage interface for physical storage devices.

The SATA/AHCI Interface features:

- Support SATA 1.5Gb/s and SATA 3.0Gb/s
- Comply with SATA Spec. 2.6, and AHCI Revision 1.3 specifications
- Support industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian
- OOB signaling detection and generation
- SATA 1.5Gb/s and SATA 3.0Gb/s speed negotiation when Tx OON signal is selected
- Support device hot-plugging
- Support power management features including automatic Partial to Slumber transition
- Internal DMA Engine for command and data transaction
- Support hardware-assisted Native Command Queuing (NCQ) up to 32 entries
- Support external SATA (eSATA)

15.2. SATA_AHCI Timing Diagram

Please refer to Serial ATA Specification Rev. 2.6 and Serial ATA Advanced Host Controller Interface (AHCI) Specification Rev. 1.1.

6.16. CAN

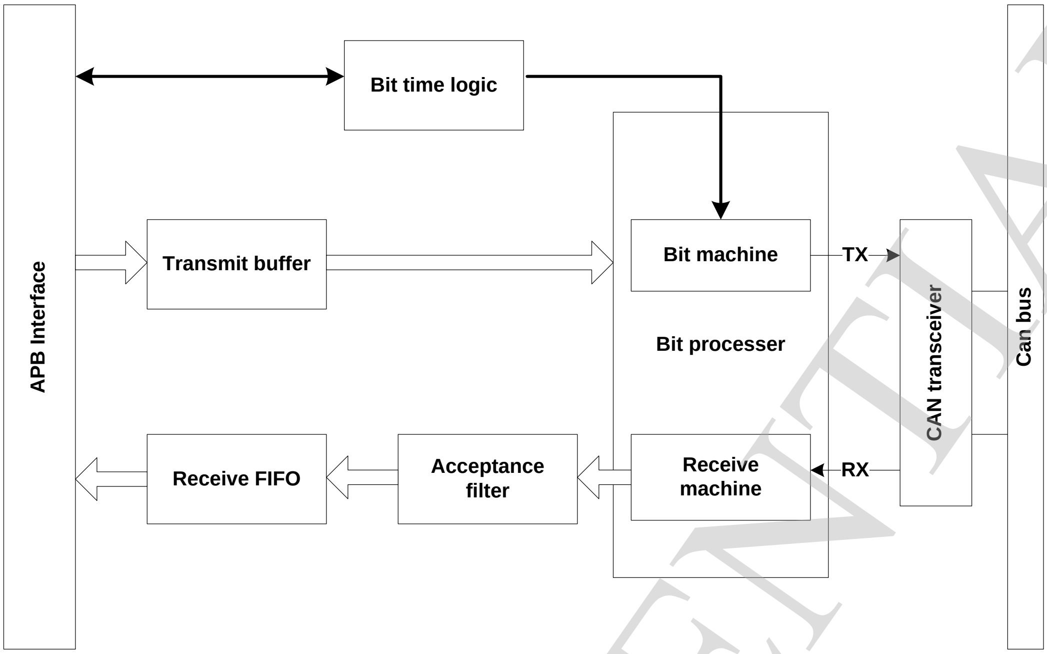
6.16.1. Overview

The CAN module is a controller for the Controller Area Network (CAN) used in automotive and general industrial environments. It implements the CAN 2.0A/B protocol as defined in the BOSCH CAN bus specification 2.0.

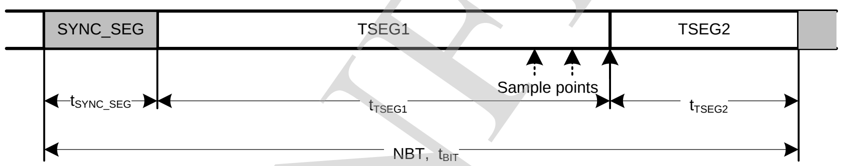
It features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Support APB 32-bit bus width operation
- Support the CAN 2.0A and 2.0B protocol specification
- Programmable data rate up to 1Mbps
- 64-byte receive buffers
- Support one shot transmission option
- Support two configurable filter modes
- Support listen-only mode
- Support self-test mode

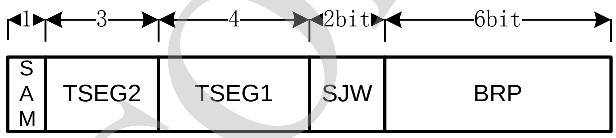
6.16.2. CAN System Block Diagram



6.16.3. CAN Bit Time Configuration



CAN bit timing segment



NBT x BPR = f_{base} / f_{canbus}, f_{base} = f_{osc} / 2 = 1 / (2 x t_{clk}), (NBT = 8~25 recommended)

TQ = 2 x t_{clk} x (32 x BRP.5 + 16 x BRP.4 + 8 x BRP.3 + 4 x BRP.2 + 2 x BRP.1 + BRP.0 + 1)

t_{clk} = 1/f_{osc}

$t_{syncseg}$ =1 x TQ

t_{tseg1} =TQ x (8 x TSEG1.3 + 4 x TSEG1.2 + 2 x TSEG1.1 + TSEG1.0 + 1)

t_{tseg2}=TQ x (4 x TSEG2.2 + 2 x TSEG2.1 + TSEG2.0 + 1)

6.17. Keypad

6.17.1. Overview

The keypad interface is used to connect external keypad devices. It can provide up to 8 rows and 8 columns. Key press or key release can be detected to the CPU by an interrupt. To prevent the switching noises, internal debouncing filter is provided.

It features:

- Support industry-standard AMBA Peripheral Bus (APB) and is fully compliant with the AMBA Specification, Revision 2.0.
- Interrupt for key press or key release
- Internal debouncing filter to prevent the switching noises

6.17.2. Keypad Interface Register List

Module Name	Base Address
KP	0x01C23000

Register Name	Offset	Description
KP_CTL	0x00	Keypad Control Register
KP_TIMING	0x04	Keypad Timing Parameter Register
KP_INT_CFG	0x08	Keypad Interrupt Configure Register
KP_INT_STA	0x0C	Keypad Interrupt Status Register
KP_IN0	0x10	Keypad Row Input Data Register 0
KP_IN1	0x14	Keypad Row Input Data Register 1

6.17.3. Keypad Interface Register Description

6.17.3.1. KEYPAD CONTROL REGISTER

Offset: 0x00			Register Name: KP_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0	ROW_INPUT_MSK Keypad Row Input Mask When set to ‘1’, the corresponding input is masked.
15:8	R/W	0	Keypad Column Output Mask When set to ‘1’, the corresponding output is masked.
7:1	/	/	/
0	R/W	0	IF_ENB Keypad Interface enable

Offset: 0x00			Register Name: KP_CTL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
			0: Disable 1: Enable

6.17.3.2. KEYPAD TIMING REGISTER

Offset: 0x04			Register Name: KP_TIMING Default Value: 0x0200_0100
Bit	Read/Write	Default	Description
31:16	R/W	0x200	DBC_CYCLE Keypad Debounce Clock Cycle n It is used for filter switching noises. When row input is low level, the Keypad Interface would delay (n+1) clock to check whether it is still keeping on low level. If it is true, the Keypad Interface would scan the external keypad's state and get these state into internal registers. After scan, the interrupt is generated if enabled. Notes: The value below 0x10 can't be used.
15:0	R/W	0x100	SCAN_CYCLE Keypad Scan Period Clock Cycle n When the Keypad Interface is enabled, it would scan the external keypad in period. The period time is 8*(n+1)/kp_clk. The kp_clk is input clock for Keypad Interface from CCU. Notes: The value below 0x10 can't be used.

6.17.3.3. KEYPAD INTERRUPT CONFIGURE REGISTER

Offset: 0x08			Register Name: KP_INT_CFG Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:2	/	/	/
1	R/W	0	REDGE_INT_EN Keypad input rising edge (key release) interrupt enable 0: Disable

Offset: 0x08			Register Name: KP_INT_CFG Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
			1: Enable
0	R/W	0	FEDGE_INT_EN Keypad input falling edge (key press) interrupt enable 0: Disable 1: Enable

6.17.3.4. KEYPAD INTERRUPT STATUS REGISTER

Offset: 0x0C			Register Name: KP_INT_STA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/
1	R/W	0	REDGE_FLAG Keypad input rising edge (key release) interrupt status When it is '1', ther key released interrupt occurred. The interrupt is cleared when write '1'.
0	R/W	0	FEDGE_FLAG Keypad input falling edge (key press) interrupt status When it is '1', the corresponding pressed interrupt occurred. The interrupt is cleared when write '1'.

6.17.3.5. KEYPAD INPUT DATA REGISTER 0

Offset: 0x10			Register Name: KP_IN0 Default Value: 0xffff_ffff
Bit	**Read/Write**	**Default**	**Description**
[8i+7:8i] (i=0~3)	R/W	0xff	COL_STA0 Keypad row input byte for column n scan (n from 0 to 3)

6.17.3.6. KEYPAD INPUT DATA REGISTER 1

Offset: 0x14			Register Name: KP_IN1 Default Value: 0xffff_ffff
Bit	**Read/Write**	**Default**	**Description**
[8i+7:8i] (i=0~3)	R/W	0xff	COL_STA1 Keypad row input byte for column n scan (n from 4 to 7)

6.17.4. Keypad Interface Special Requirement

6.17.4.1. KEYPAD INTERFACE PIN LIST

Port Name	Width	Direction	Description
KP_OUT	8	OUT	
KP_IN	8	IN	

Appendix A

Glossary

A

AES	Advanced Encryption Standard	A specification for the encryption of electronic data established by the U.S.National Institute of Standards and Technology (NIST) in 2001
AGC	Automatic Gain Control	An adaptive system found in electronic devices that automatically controls the gain of a signal: the average output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels.
AHB	AMBA High-speed Bus	A bus protocol introduced in Advanced Microcontroller Bus Architecture version 2 published by ARM Ltd company
APB	Advanced Peripheral Bus	APB is designed for low bandwidth control accesses, which has an address and data phase similar to AHB, but a much reduced, low complexity signal list (for example no bursts).
AVS	Audio Video Standard	A compression standard for digital audio and video

C

CIR	Consumer IR	The CIR (Consumer IR) interface is used for remote control through infra-red light
CRC	Cyclic Redundancy Check	A type of hash function used to produce a checksum in order to detect errors in data storage or transmission
CSI	CMOS Sensor Interface	The hardware block that interfaces with different image sensor interfaces and provides a standard output that can be used for subsequent image processing

D

DES	Data Encryption Standard	A previously predominant algorithm for the encryption of electronic data
DEU	Detail Enhancement Unit	A unit used for display engine frontend data post processing
DLL	Delay-Locked Loop	A digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator, replaced by a delay line
DRC	Dynamic Range Compression	It reduces the volume of loud sounds or amplifies quiet sounds by narrowing or "compressing" an audio signal's dynamic range.
DVFS	Dynamic Voltage and Frequency Scaling	Dynamic voltage scaling is a power management technique where the voltage used in a component is increased or decreased, depending on circumstances. Dynamic frequency scaling is a technique whereby the frequency of a microprocessor can be automatically adjusted on the fly so that the power consumption or heat generated by the chip can be reduced. These two are often used together to save power in mobile devices.

E

EHCI	Enhanced Host Controller Interface	The register-level interface for a Host Controller for the USB Revision 2.0.
eMMC	Embedded Multi-Media Card	An architecture consisting of an embedded storage solution with MMC interface, flash memory and controller, all in a small BGA package

F

FBGA	Fine Ball Grid Array	FBGA is based on BGA technology, but comes with thinner contacts and is mainly used in SoC design

G

GIC	Generic Interrupt Controller	A centralized resource for supporting and managing interrupts in a system that includes at least one processor

H

HDMI	High-Definition Multimedia Interface	A compact audio/video interface for transmitting uncompressed digital data

I

I2S	IIS	An electrical serial bus interface standard used for connecting digital audio devices together

L

LSB	Least Significant Bit	The bit position in a binary integer giving the units value, that is, determining whether the number is even or odd. It is sometimes referred to as the right-most bit, due to the convention in positional notation of writing less significant digits further to the right.
LRADC	Low Resolution Analog to Digital Converter	A module which can transfer analog signals to digital signals

M

MAC	Media Access Control	A sublayer of the data link layer, which provides addressing and channel access control mechanisms that make it possible for several terminals or network nodes to communicate within a multiple access network that incorporates a shared medium, e.g.Ethernet.
MII	Media Independent Interface	An interface originally designed to connect a fast Ethernet MAC-block to a PHY chip, which now has been extended to support reduced signals and increased speeds
MSB	Most Significant Bit	The bit position in a binary number having the greatest value, which is sometimes referred to as the left-most bit due to the convention in positional notation of writing more significant digits further to the left

N

NTSC	National Television System Committee	An analog television system that is used in most of North America, and many other countries

O

OHCI	Open Host Controller Interface	A register-level interface that enables a host controller for USB or FireWire hardware to communicate with a host controller driver in software
OSD	On-Screen Display	A feature of visual devices like VCRs and DVD players that displays program, position, and setting data on a connected TV or computer display

P

PAL	Phase Alternating Line	An analogue television color encoding system used in broadcast television systems in many countries
PCM	Pulse Code Modulation	A method used to digitally represent sampled analog signals

PID	Packet Identifier	Each table or elementary stream in a transport stream is identified by a 13-bit packet ID (PID). A demultiplexer extracts elementary streams from the transport stream in part by looking for packets identified by the same PID.

S

SPI	Synchronous Peripheral Interface	A synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame

T

TP	Touch Panel	A human-machine interactive interface
TS	Transport Stream	A data stream defined by ISO13818-1, which consists of one or more programs with video and audio data.

U

USB OTG	Universal Serial Bus On-The-Go	A dual-role controller, which supports both Host and Device functions and is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a