A10 Datasheet

V1.30

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Revision History

Version	Date	Section/ Page	Changes compared to previous issue
V1.00	2011.08.22		Initial version
V1.10	2012.02.17		LCD/tv timing controller overview
V1.20	2012.03.29		Revise some description
V1.21	2012.04.06		Revise some USB description
V1.30	2012.08.24		Revise some pin description

Technical Items

NO.	Abbreviation	Full Name	Description
1	ARM Cortex™-A8	ARM Cortex™-A8	a processor core designed by ARM Holdings implementing the ARM v7 instruction set architecture
2	Mali-400	Mali-400	A 2D/3D graphic processor unit designed by ARM Holdings
3	SDRAM	Synchronous Dynamic Random Access Memory	dynamic random access memory (DRAM) that is synchronized with the system bus
4	PWM	Pulse Width Modulator	a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches
5	SPI	Serial Peripheral Interface	a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame
6	UART	Universal Asynchronous Receiver/Transmitter	used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set
7	DMA	Dynamic-Memory-Allocation	the allocation of memory storage for use in a computer program during the run-time of that program
8	I2S	IIS	an electrical serial bus interface standard used for connecting digital audio devices together
9	PCM	Pulse Code Modulation	method used to digitally represent sampled analog signals
10	AC97	Audio Codec 97	Intel Corporation's Audio Codec standard developed by the Intel Architecture Labs in 1997, and used mainly in motherboards, modems, and sound cards.
11	Audio Codec	Audio Codec	a computer program implementing an algorithm that compresses and decompresses digital audio data according to a given audio file format or streaming media audio format.
12	SD	Security Digital3.0	a non-volatile memory card format developed by the SD Card Association for use in portable devices.
13	USB OTG	USB On-The-Go	dual-role controller, which supports both Host and device functions and is full compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a
14	EHCI	Enhanced Host Controller Interface	a high-speed controller standard that is publicly specified
15	LRADC	Low Resolution Analog to Digital Converter	A module which can transfer analog signal to digital signal
16	TP	Touch Panel Controller	A Human-Machine Interactive Interface
17	TS	Transport Stream	A data stream defined by ISO13818-1, which consists of one or more programs with video and audio data.
18	CAN	Controller–area network	a vehicle bus standard designed to allow microcontrollers

			and devices to communicate with each other within a vehicle without a host computer
19	PATA	Parallel Advanced Technology Attachment	An old computer bus interface for connecting hard disk drivers, optical drivers, and compact flash card
20	SATA	Serial Advanced Technology Attachment	a computer bus interface for connecting host bus adapters to mass storage devices such as hard disk drives and optical drives.
21	CSI	CMOS Sensor Interface	the hardware block that interfaces with different image sensor interfaces and provides a standard output that can be used for subsequent image processing.
22	HDMI	High-Definition Multimedia Interface	a compact audio/video interface for transmitting uncompressed digital data

Contents

1. Introduction

With ARM Cortex A8 core, A10 will drive SoC into a brand new era of connected Smart HD which can enhance the application of connected HD SOC as well as user experiences of consumer electronics like multimedia products. Due to its outstanding connected HD video performance and cost efficiency, the highly integrated A10 is target at cool HD pad which can bring end-users better experiences of surfing, watching, gaming and reading.

The A10 is dedicated to furthering the development of connected HD video CODEC application, and 1080P H.264 high profile encoding technology can become one of the benchmarks. Besides its remarkable super HD 2160p video decoding capability, A10 can stream smoothly HD video over internet, including FLASH10.3/HTML5/3RD APK.

Besides self-developed display acceleration frame, MALI400 2D/3D GPU has also been introduced to strengthen the connected smart HD SOC in terms of high profile display so that it can support popular smart systems such as Android2.3/3.0 better and improve the performance of Android-loaded products as well as user experience.

There is no doubt that low power consumption and excellent user experience will be always on the top of end-users' wish list. A10 has adopted Allwinnertech's most advanced technology of video CODEC and power consumption is much lower during 1080p decoding process. What's more, Allwinnertech will keep applying progressive VLSI design under new process so that end products can become even more competitive with shorter R&D cycle and easier production advantages.

2. Feature

CPU

- ARM **Cortex-A8** Core
- 32KB **I-Cache**/32KB **D-Cache**/256K **L2 Cache**
- Using **NEON** for video, audio,and graphic workloads eases the burden of supporting more delicated accelerators across the SoC and enable the system to support the standards of tomorrow
- **RCT JAVA-Accelerations** to optimize just in time(JIT) and dynamitic adaptive compilation(DAC), and reduces memory footprint up to three times
- **Trustzone technology** allows for secure transactions and digital right managements(DRM)

GPU

3D

- support Open GL ES 2.0 / open VG 1.1

2D

- support BLT / ROP2/3/4
- Rotation 90/180/270 degree
- Mirror / alpha (including plane and pixel alpha) / color key support
- Scaling function with 4*4 taps and 32 phase
- Support format conversion

VPU

- **Video Decoding** (Super HD 2160P)
  Support all popular video formats, including **VP8, AVS, H.264**, H.263, VC-1, MPEG-1/2/4
  Support 1920*1080@60fps in all formats
- **Video Encoding**
  Support encoding in H.264 High Profile format
  1080p@60fps
  720p @100fps

Display Processing Ability

- Four moveable and size-adjustable layers
- Support 8 tap scale filter in horizontal and 4 tap in vertical direction for scaling
- support Multi-format image input
- support Alpha blending / color key / gamma
- support Hardware cursor / sprite
- support Vertical keystone correction
- support Output color correction (luminance / hue / saturation etc)
- support motion adaptive de-interlace
- support Video enhancement

- support 3D format content input/output format convert/display (including HDMI)

Display Output Ability

- Support HDMI V1.3/V1.4
- Flexible LCD interface (CPU / Sync RGB / LVDS) up to 1920*1080 resolution
- CVBS / YPbPr up to 1920*1080 resolution

ImageInput Ability

- Dual camera sensor interface (CSI0 supports ISP function)

Memory

- 16/32-bits SDRAM controller
  support **DDR2** SDRAM and **DDR3** SDRAM up to 800Mbps
  Memory Capacity up to 16 G-bits
- 8-bits NAND Flash Controller with 8 chip select and 2 r/b signals
  Support **SLC/MLC/TLC/DDR NAND**
  ECC up to **64bit**

Peripherals

- 1 USB 2.0 **OTG** controller for general application/2 USB2.0 EHCI Controller for HOST application
- 4 high-speed Memory controller supports SD version 3.0 and MMC version 4.2
- **8 UARTs** with 64 Bytes TX FIFO and 64 Bytes RX FIFO,
  1 UART with full modem function
  2 UARTs with RTS/CTS hardware flow control
  5 UARTs with two wires
- **4 SPI** controllers
  1 dedicated SPI controller for serial NOR Flash boot application
  3 SPI for general applications
- **3 Two-Wire** Interfaces up to 400Kbps
- Key Matrix (8x8) with internal debounce filter
- IR controller supports MIR, FIR and IR remoter
- 2-CH 6-bits LRADC for line control
- Internal 4-wire touch panel controller with pressure sensor and 2-point touch
- I2S/PCM controller for 8-channel output and 2-channel input
- AC97 controller compatible with AC97 version 2.3 standard
- Internal 24-bits Audio Codec for 2 channel headphone, 2 channel microphone, 2 channel FM input and Line input
- 2 PWM controllers

System

- 8 channel normal DMA and 8 channel dedicated DMA
- Internal (32K+64K) SRAM on chip
- 6 timers, 1 RTC timer and 1 watchdog

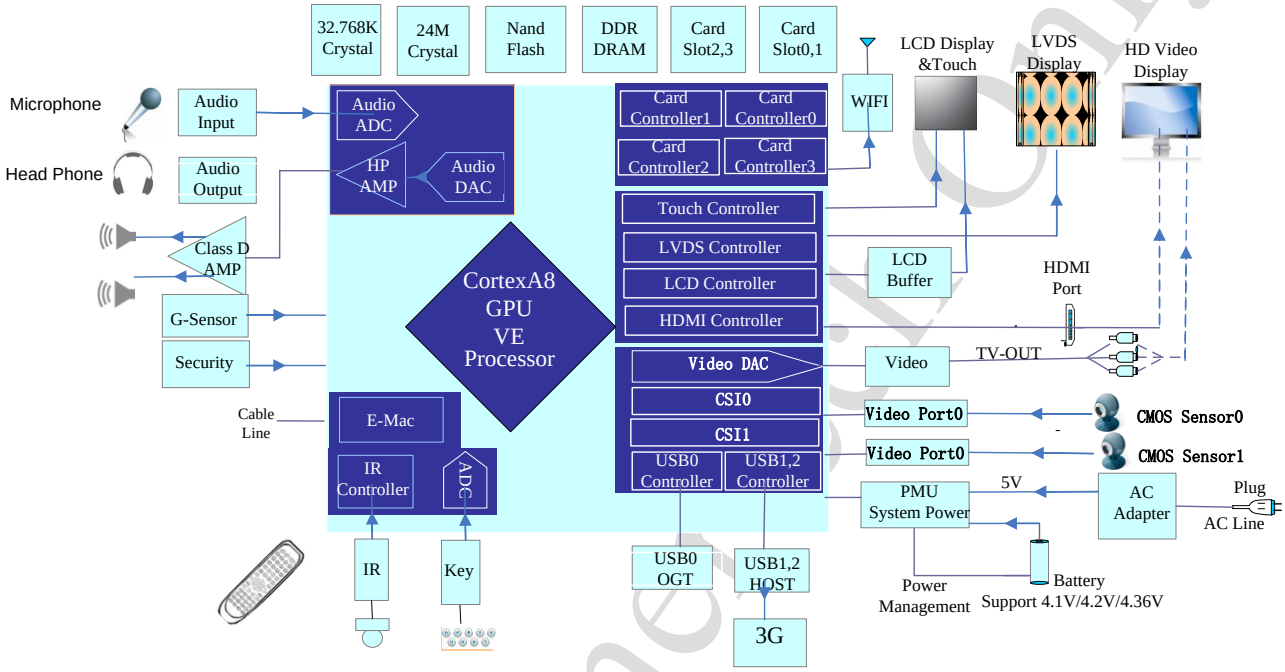
Security

- Security System
  Support DES, 3DES, AES encryption and decryption.
  Support SHA-1, MD5 message digest
  Support hardware 64-bit random generator
- 128-bits EFUSE chip ID

Package

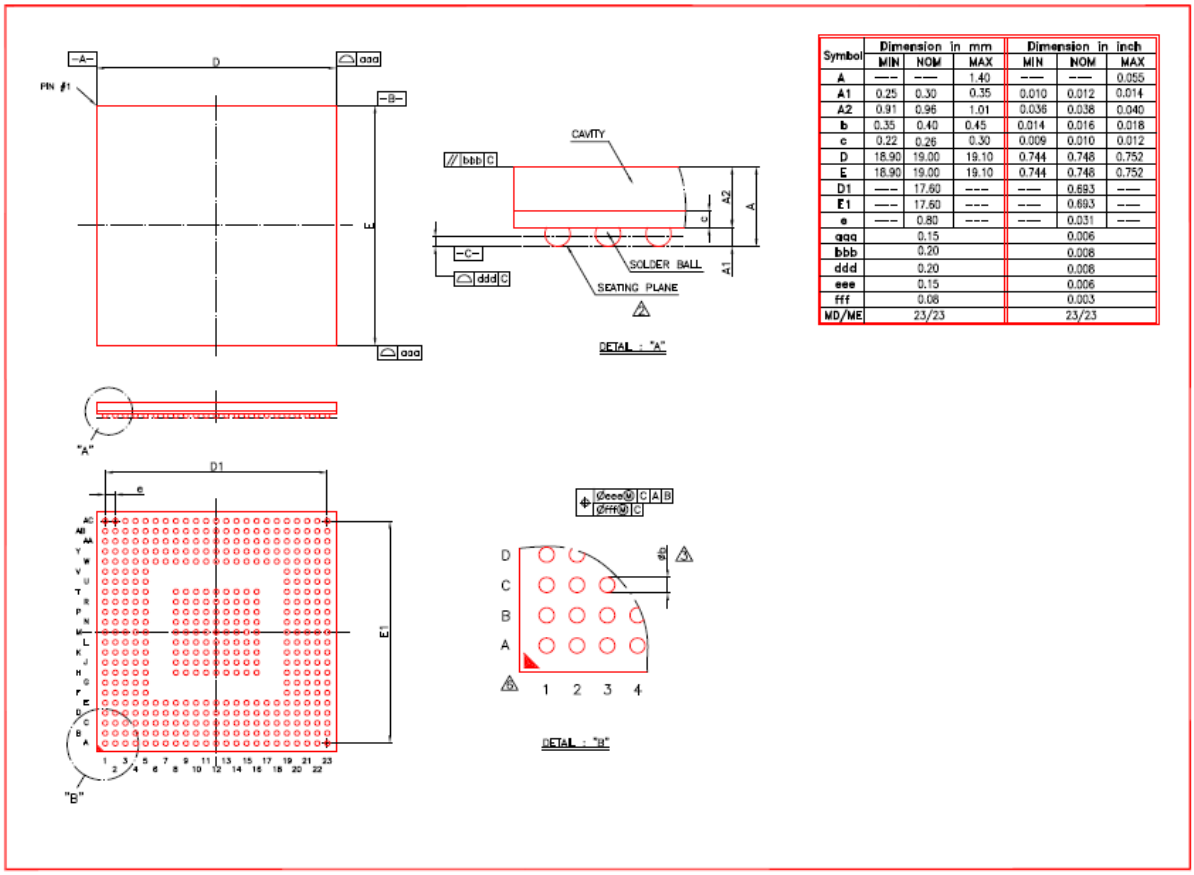
- TFBGA441package
- 0.8mm pitch

3. Functional Block Diagram



4. Pin Assignments

4.1. Dimension



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		

Figure 4-1 A10 TFBGA441 Package Dimension

4.2. Pin Map

The following pin maps show the top view of the 441-pin FBGA package pin assignments in four quadrants (A, B, C, D).

	1	2	3	4	5	6	7	8	9	10	11
A	PH15	PH13	PH10	PH6	PH3	PH0	PB22	PB18	PB16	PB14	PB8
B	PH16	PH14	PH11	PH7	PH4	PH1	PB23	PB19	PB17	PB15	PB13
C	PH17	PH18	PH12	PH8	PH5	PH2	PB21	PB20	PB12	PB11	PB10
D	PH19	PH20	PH21	PH9	PA0	PA2	PA4	PA6	PA8	PA10	PA12
E	PH22	PH23	PH24	PH25	PA1	PA3	PA5	PA7	PA9	PA11	PA13
F	CLK32K_IN	CLK32K_OUT	PH26	PH27	NMI#						
G	SDQM3	SDQ30	GND_DRAM	GND_DRAM	VCC_DRAM						
H	SDQ25	SDQ27	SVREF0	SVREF1	VCC_DRAM			VCC	VCC	VCC	VDD_CPU
J	SDQ28	SDQS3#	ODT1	SCKE1	GND_DRAM			VCC	VCC	VCC	GND
K	SDQS3	SDQ31	SBA0	SBA2	GND_DRAM			RTC_VDD	VDD_INT	VDD_INT	GND
L	SDQ24	SDQ26	SA10	SBA1	VCC_DRAM			VDD_INT	VDD_INT	GND	GND

Figure 4-2 TFBGA441 Pin Map-Top View [Quadrant A]

12	13	14	15	16	17	18	19	20	21	22	23	
PB6	PB4	PB2	PB0	PI8	PI6	PI4	PI2	PI0	PE11	PE9	PE8	A
PB7	PB5	PB3	PB1	PI9	PI7	PI5	PI3	PI1	PE10	PE7	PE6	B
PB9	PA17	RESET#	PI14	PI12	PI10	PG11	PG9	PG7	PG5	PE5	PE4	C
PA14	PA16	PI19	PI15	PI13	PI11	PG10	PG8	PG4	PG3	PE3	PE2	D
PA15	PI21	PI20	PI18	PI17	PI16	VCC_CSI1	PG6	PG2	PG1	PE1	PE0	E
							VCC_CSI0	PG0	PC24	PC18	PC17	F
							PC23	PC15	PC14	PC11	PC10	G
VDD_CPU	VDD_CPU	VDD_CPU	VCC	TEST			VCC_NAND	PC13	PC12	PC9	PC8	H
VDD_CPU	VDD_CPU	VCC	VDD_INT	VDD_INT			VCC_NAND	PC22	PC21	PC7	PC6	J
GND	GND	ULGND	VDD_INT	ULVDD			PF5	PF4	PC20	PC5	PC4	K
GND	UGND_T	UGND_C	UVCC_T	UVCC_C			PF3	PF2	PC19	PC3	PC2	L

Figure 4-3 TFBGA441 Pin Map-Top View [Quadrant B]

M	SDQ29	SDQ23	SA7	SA3	VCC_DRAM			VDD_DLL	GND_DLL	GND	GND
N	SDQ16	SDQ18	SCKE0	SA5	GND_DRAM			NC	VDD_DLL	GND_DLL	GND
P	SDQ21	SDQS2#	SA12	SA9	GND_DRAM			NC	VDD_DLL	GND_DLL	GND
R	SDQS2	SDQM2	SA14	SA1	VCC_DRAM			NC	VDD_INT	VDD_INT	GND
T	SDQ22	SDQ17	SWE	SRAS	VCC_DRAM			VDD_INT	GND	JTAG_SEL	GND
U	SDQ19	SDQ20	SCAS	SA2	GND_DRAM						
V	SCK	SCK#	SCS0	SA6	GND_DRAM						
W	SDQM1	SDQ14	SA11	SA0	VCC_DRAM	VCC_DRAM	VCC_DRAM	UBOOT_SEL	GND_LVDS	GND_LVDS	GND_LVDS
Y	SDQ9	SDQ11	SA13	SA4	SVREF2	VCC_DRAM	GND_DRAM	GND_DRAM	PD24	PD20	PD18
AA	SDQ12	SDQS1#	SA8	SCS1	ODT0	SRST	SZQ	SVREF3	PD25	PD21	PD19
AB	SDQS1	SDQ8	SDQ13	SDQ0	SDQ5	SDQS0	SDQ6	SDQ3	PD26	PD22	PD8
AC	SDQ15	SDQ10	SDQ7	SDQ2	SDQS0#	SDQM0	SDQ1	SDQ4	PD27	PD23	PD9
	1	2	3	4	5	6	7	8	9	10	11

Figure 4-4 TFBGA441 Pin Map-Top View [Quadrant C]

GND	GND	NC	NC	NC			PF1	PF0	PC16	PC1	PC0	M
GND	NC	NC	NC	NC			VCC_CARD	DM0	DP0	CLK24M_OUT	CLK24M_IN	N
GND	GND_HDMI	GND_HDMI	PLLGND	PLLVP25			NC	DM1	DP1	HPD_HDMI	CEC_HDMI	P
GND	GND_HDMI	NC	NC	NC			NC	DM2	DP2	SDA_HDMI	SCL_HDMI	R
GND	VP_HMDI	NC	NC	NC			AVCC	NC	NC	TX2N_HDMI	TX2P_HDMI	T
							AGND	NC	NC	TX1N_HDMI	TX1P_HDMI	U
							HPGND	VRA2	NC	TX0N_HDMI	TX0P_HDMI	V
VCC_LVDS	VCC_LVDS	VCC_LVDS	VCC33_TVOUT	NC	NC	GND33_TVOUT	HPR	VRA1	VRP	TXCN_HDMI	TXCP_HDMI	W
PD16	PD14	PD12	PD10	NC	NC	NC	HPL	FMINL	FMINR	XP_TP	YP_TP	Y
PD17	PD15	PD13	PD11	NC	NC	NC	HPCOM	HPCOMFB	VMIC	XN_TP	YN_TP	AA
PD6	PD4	PD2	PD0	TVOUT1	TVOUT3	NC	HPVCCIN	LINEINL	LINEINR	LRADC1	LRADC0	AB
PD7	PD5	PD3	PD1	TVOUT0	TVOUT2	NC	HPVCC	MICIN1	MICIN2	MIC1OUTP	MIC1OUTN	AC
12	13	14	15	16	17	18	19	20	21	22	23	

Figure 4-5 TFBGA441Pin Map-Top View [Quadrant D]

5. Pin Description

5.1. Pin Characteristics

1. **BALL#:** Ball numbers on the bottom side associated with each signals on the bottom.
2. **Pin Name:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in function 0).
3. **Function:** Multiplexing function number.
   Function 0 is the the default function, but is not necessarily the primary mode.
   Functions 1 to 5 are possible modes for alternate functions.
4. **Type:** signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - A = Analog
   - AIO = Analog Input/Output
   - PWR = Power
   - GND = Ground
5. **Pin Reset State:** The state of the terminal at reset (power up).
   - 0: The buffer drives VOL(pull down/pull up resistor not activated)
   - 0 (PD): The buffer drives V_{OL} with an active pull down resistor.
   - 1: The buffer drives VOH (pull down/pull up resistor not activated).
   - 1 (PU): The buffer drives V_{OH} with an active pull up resistor.
   - Z: High-impedance
   - L: High-impedance with an active pull down resistor.
   - H: High-impedance with an active pull up resistor.
6. **Pull Up/Down:** Denotes the presence of an internal pull up or pull down resister. Pull up and pull down resistor can be enabled or disabled via software.
7. **Buffer Strength:** Drive strength of the associated output buffer.

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
AB4	SDQ0		I/O			
AC7	SDQ1		I/O			
AC4	SDQ2		I/O			
AB8	SDQ3		I/O			
AC8	SDQ4		I/O			
AB5	SDQ5		I/O			
AB7	SDQ6		I/O			
AC3	SDQ7		I/O			

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
AB2	SDQ8		I/O			
Y1	SDQ9		I/O			
AC2	SDQ10		I/O			
Y2	SDQ11		I/O			
AA1	SDQ12		I/O			
AB3	SDQ13		I/O			
W2	SDQ14		I/O			
AC1	SDQ15		I/O			
N1	SDQ16		I/O			
T2	SDQ17		I/O			
N2	SDQ18		I/O			
U1	SDQ19		I/O			
U2	SDQ20		I/O			
P1	SDQ21		I/O			
T1	SDQ22		I/O			
M2	SDQ23		I/O			
L1	SDQ24		I/O			
H1	SDQ25		I/O			
L2	SDQ26		I/O			
H2	SDQ27		I/O			
J1	SDQ28		I/O			
M1	SDQ29		I/O			
G2	SDQ30		I/O			
K2	SDQ31		I/O			
H3	SVREF0		I			
H4	SVREF1		I			
Y5	SVREF2		I			
AA8	SVREF3		I			
AB6	SDQS0		I/O			
AC5	SDQS0 #		O			
AC6	SDQM0		O			
AB1	SDQS1		I/O			
AA2	SDQS1 #		O			
W1	SDQM1		O			
R2	SDQM2		I/O			
P2	SDQS2 #		O			
K1	SDQS3		I/O			
J2	SDQS3 #		O			
G1	SDQM3		O			
V2	SCK#		O			

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
V1	SCK		O			
J4	SCKE1		O			
N3	SCKE0		O			
W4	SA0		O			
R4	SA1		O			
U4	SA2		O			
M4	SA3		O			
Y4	SA4		O			
N4	SA5		O			
V4	SA6		O			
M3	SA7		O			
AA3	SA8		O			
P4	SA9		O			
L3	SA10		O			
W3	SA11		O			
P3	SA12		O			
Y3	SA13		O			
R3	SA14		O			
K3	SBA0		O			
L4	SBA1		O			
K4	SBA2		O			
T3	SWE		O			
U3	SCAS		O			
T4	SRAS		O			
V3	SCS0		O			
AA4	SCS1		O			
AA5	ODT0		O			
J3	ODT1		O			
AA7	SZQ					
AA6	SRST		O			
N8/P8/R8	NC					
M8/N9/P9	VDD_DLL		P			
M9/N10/P10	GND_DLL		P			
D5	PA0	0/1	I/O			
	ERXD3	2				
	SPI1_CS0	3				
	UART2_RTS	4				
E5	PA1	0/1	I/O			
	ERXD2	2				
	SPI1_CLK	3				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	UART2_CTS	4				
D6	PA2	0/1	I/O			
	ERXD1	2				
	SPI1_MOSI	3				
	UART2_TX	4				
E6	PA3	0/1	I/O			
	ERXD0	2				
	SPI1_MISO	3				
	UART2_RX	4				
D7	PA4	0/1	I/O			
	ETXD3	2				
	SPI1_CS1	3				
E7	PA5	0/1	I/O			
	ETXD2	2				
	SPI3_CS0	3				
D8	PA6	0/1	I/O			
	ETXD1	2				
	SPI3_CLK	3				
E8	PA7	0/1	I/O			
	ETXD0	2				
	SPI3_MOSI	3				
D9	PA8	0/1	I/O			
	ERXCK	2				
	SPI3_MISO	3				
E9	PA9	0/1	I/O			
	ERXERR	2				
	SPI3_CS1	3				
D10	PA10	0/1	I/O			
	ERXDV	2				
	UART1_TX	4				
E10	PA11	0/1	I/O			
	EMDC	2				
	UART1_RX	4				
D11	PA12	0/1	I/O			
	EMDIO	2				
	UART6_TX	3				
	UART1_RST	4				
E11	PA13	0/1	I/O			
	ETXEN	2				
	UART6_RX	3				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	UART1_CTS	4				
D12	PA14	0/1	I/O			
	ETXCK	2				
	UART7_TX	3				
	UART1_DTR	4				
E12	PA15	0/1	I/O			
	ECRS	2				
	UART7_RX	3				
	UART1_DSR	4				
D13	PA16	0/1	I/O			
	ECOL	2				
	CAN_TX	3				
	UART1_DCD	4				
C13	PA17	0/1	I/O			
	ETXERR	2				
	CAN_RX	3				
	UART1_RING	4				
A15	PB0	0/1	I/O			
	TWI0_SCK	2				
B15	PB1	0/1	I/O			
	TWI0_SDA	2				
A14	PB2	0/1	I/O			
	PWM0	2				
B14	PB3	0/1	I/O			
	IR_TX	2				
	NC	3				
	EINT16	5				
A13	PB4	0/1	I/O			
	IR_RX	2				
B13	PB5	0/1	I/O			
	I2S_MCLK	2				
	AC97_MCLK	3				
A12	PB6	0/1	I/O			
	I2S_BCLK	2				
	AC97_BCLK	3				
B12	PB7	0/1	I/O			
	I2S_LRCK	2				
	AC97_SYNC	3				
A11	PB8	0/1	I/O			
	I2S_DO0	2				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	AC97_DO	3				
C12	PB9	0/1	I/O			
	I2S_DO1	2				
C11	PB10	0/1	I/O			
	I2S_DO2	1				
C10	PB11	0/1	I/O			
	I2S_DO3	1				
C9	PB12	0/1	I/O			
	I2S_DI	2				
	AC97_DI	3				
	NC	4				
B11	PB13	0/1	I/O			
	SPI2_CS1	2				
	NC	4				
A10	PB14	0/1	I/O			
	SPI2_CS0	2				
	JTAG_MS0	3				
B10	PB15	0/1	I/O			
	SPI2_CLK	2				
	JTAG_CK0	3				
A9	PB16	0/1	I/O			
	SPI2_MOSI	2				
	JTAG_DO0	3				
B9	PB17	0/1	I/O			
	SPI2_MOSO	2				
	JTAG_DI0	3				
A8	PB18	0/1	I/O			
	TWI1_SCK	2				
B8	PB19	0/1	I/O			
	TWI1_SDA	2				
C8	PB20	0/1	I/O			
	TWI2_SCK	2				
C7	PB21	0/1	I/O			
	TWI2_SDA	2				
A7	PB22	0/1	I/O			
	UART0_TX	2				
	IR1_TX	3				
B7	PB23	0/1	I/O			
	UART0_RX	2				
	IR1_RX	3				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
M23	PC0	0/1	I/O			
	NWE#	2				
	SPI0_MOSI	3				
M22	PC1	0/1	I/O			
	NALE	2				
	SPI0_MISO	3				
L23	PC2	0/1	I/O			
	NCLE	2				
	SPI0_CLK	3				
L22	PC3	0/1	I/O		Pull Up (default)	
	NCE1	2				
	SDC1_CMD	3				
K23	PC4	0/1	I/O		Pull Up (default)	
	NCE0	1				
K22	PC5	0/1	I/O			
	NRD	1				
	SDC1_CLK	2				
J23	PC6	0/1	I/O		Pull Up (default)	
	NRB0	2				
	SDC2_CMD	3				
J22	PC7	0/1	I/O		Pull Up (default)	
	NRB1	2				
	SDC2_CLK	3				
H23	PC8	0/1	I/O			
	ND0	2				
	SDC2_D0	3				
H22	PC9	0/1	I/O			
	ND1	2				
	SDC2_D1	3				
G23	PC10	0/1	I/O			
	ND2	2				
	SDC2_D2	3				
G22	PC11	0/1	I/O			
	ND3	2				
	SDC2_D3	3				
H21	PC12	0/1	I/O			
	ND4	2				
	SDC1_D0	3				
H20	PC13	0/1	I/O			
	ND5	2				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	SDC1_D1	3				
G21	PC14	0/1	I/O			
	ND6	2				
	SDC1_D2	3				
G20	PC15	0/1	I/O			
	ND7	2				
	SDC1_D3	3				
M21	PC16	0/1	I/O		Pull Down (default)	
	NWP	1				
F23	PC17	0/1	I/O		Pull Up (default)	
	NCE2	1				
F22	PC18	0/1	I/O		Pull Up (default)	
	NCE3	1				
L21	PC19	0/1	I/O			
	NCE4	1				
	SPI2_CS0	2				
	EINT12	5				
K21	PC20	0/1	I/O			
	NCE5	1				
	SPI2_CLK	2				
	EINT13	5				
J21	PC21	0/1	I/O			
	NCE6	1				
	SPI2_MOSI	2				
	EINT14	5				
J20	PC22	0/1	I/O			
	NCE7	1				
	SPI2_MISO	2				
	EINT15	5				
G19	PC23	0/1	I/O		Pull Up (default)	
	SPI0_CS0	2				
F21	PC24	0/1	I/O			
	NDQS					
AB15	PD0	0/1	I/O			
	LCD0_D0	2				
	LVDS0_VP0	3				
AC15	PD1	0/1	I/O			
	LCD0_D1	2				
	LVDS0_VN0	3				
AB14	PD2	0/1	I/O			

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	LCD0_D2	2				
	LVDS0_VP1	3				
AC14	PD3	0/1	I/O			
	LCD0_D3	2				
	LVDS0_VN1	3				
AB13	PD4	0/1	I/O			
	LCD0_D4	2				
	LVDS0_VP2	3				
AC13	PD5	0/1	I/O			
	LCD0_D5	2				
	LVDS0_VN2	3				
AB12	PD6	0/1	I/O			
	LCD0_D6	2				
	LVDS0_VPC	3				
AC12	PD7	0/1	I/O			
	LCD0_D7	2				
	LVDS0_VNC	3				
AB11	PD8	0/1	I/O			
	LCD0_D8	2				
	LVDS0_VP3	3				
AC11	PD9	0/1	I/O			
	LCD0_D9	2				
	LVDS0_VN3	3				
Y15	PD10	0/1	I/O			
	LCD0_D10	2				
	LVDS1_VP0	3				
AA15	PD11	0/1	I/O			
	LCD0_D11	2				
	LVDS1_VN0	3				
Y14	PD12	0/1	I/O			
	LCD0_D12	2				
	LVDS1_VP1	3				
AA14	PD13	0/1	I/O			
	LCD0_D13	2				
	LVDS1_VN1	3				
Y13	PD14	0/1	I/O			
	LCD0_D14	2				
	LVDS1_VP2	3				
AA13	PD15	0/1	I/O			
	LCD0_D15	2				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	LVDS1_VN2	3				
Y12	PD16	0/1	I/O			
	LCD0_D16	2				
	LVDS1_VPC	3				
AA12	PD17	0/1	I/O			
	LCD0_D17	2				
	LVDS1_VNC	3				
Y11	PD18	0/1	I/O			
	LCD0_D18	2				
	LVDS1_VP3	3				
AA11	PD19	0/1	I/O			
	LCD0_D19	2				
	LVDS1_VN3	3				
Y10	PD20	0/1	I/O			
	LCD0_D20	2				
	CSI1_MCLK	3				
AA10	PD21	0/1	I/O			
	LCD0_D21	2				
	SMC_VPPEN	3				
AB10	PD22	0/1	I/O			
	LCD0_D22	2				
	SMC_VPPPP	3				
AC10	PD23	0/1	I/O			
	LCD0_D23	2				
	SMC_DET	3				
Y9	PD24	0/1	I/O			
	LCD0_CLK	2				
	SMC_VCCEN	3				
AA9	PD25	0/1	I/O			
	LCD0_DE	2				
	SMC_RST	3				
AB9	PD26	0/1	I/O			
	LCD0_HSYNC	2				
	SMC_SLK	3				
AC9	PD27	0/1	I/O			
	LCD0_VSYNC	2				
	SMC_SDA	3				
E23	PE0	0/1	I/O			
	TS0_CLK	2				
	CSI0_PCK	3				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
E22	PE1	0/1	I/O			
	TS0_ERR	2				
	CSI0_CK	3				
D23	PE2	0/1	I/O			
	TS0_SYNC	2				
	CSI0_HSYNC	3				
D22	PE3	0/1	I/O			
	TS0_DVLD	2				
	CSI0_VSYNC	3				
C23	PE4	0/1	I/O			
	TS0_D0	2				
	CSI0_D0	3				
C22	PE5	0/1	I/O			
	TS0_D1	2				
	CSI0_D1	3				
B23	PE6	0/1	I/O			
	TS0_D2	2				
	CSI0_D2	3				
B22	PE7	0/1	I/O			
	TS0_D3	2				
	CSI0_D3	3				
A23	PE8	0/1	I/O			
	TS0_D4	2				
	CSI0_D4	3				
A22	PE9	0/1	I/O			
	TS0_D5	2				
	CSI0_D5	3				
B21	PE10	0/1	I/O			
	TS0_D6	2				
	CSI0_D6	3				
A21	PE11	0/1	I/O			
	TS0_D7	2				
	CSI0_D7	3				
M20	PF0	0/1	I/O			
	SDC0_D1	2				
	JTAG_MS1	4				
M19	PF1	0/1	I/O			
	SDC0_D0	2				
	JTAG_DI1	4				
L20	PF2	0/1	I/O			

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	SDC0_CLK	2				
	UART0_TX	4				
L19	PF3	0/1	I/O			
	SDC0_CMD	2				
	JTAG_DO1	4				
K20	PF4	0/1	I/O			
	SDC0_D3	2				
	UART0_RX	4				
K19	PF5	0/1	I/O			
	SDC0_D2	2				
	JTAG_CK1	4				
F20	PG0	0/1	I/O			
	TS1_CLK	2				
	CSI1_PCLK	3				
	SDC1_CMD	4				
E21	PG1	0/1	I/O			
	TS1_ERR	2				
	CSI1_MLCK	3				
	SDC1_CLK	4				
E20	PG2	0/1	I/O			
	TS1_SYNC	2				
	CSI1_HSYNC	3				
	SDC1_D0	4				
D21	PG3	0/1	I/O			
	TS1_DVLD	2				
	CSI1_VSYNC	3				
	SDC1_D1	4				
D20	PG4	0/1	I/O			
	TS1_D0	2				
	CSI1_D0	3				
	SDC1_D2	4				
	CSI0_D8	5				
C21	PG5	0/1	I/O			
	TS1_D1	2				
	CSI1_D1	3				
	SDC1_D3	4				
	CSI0_D9	5				
E19	PG6	0/1	I/O			
	TS1_D2	2				
	CSI1_D2	3				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	UART3_TX	4				
	CSI0_D10	5				
C20	PG7	0/1	I/O			
	TS1_D3	2				
	CSI1_D3	3				
	UART3_RX	4				
	CSI0_D11	5				
D19	PG8	0/1	I/O			
	TS1_D4	2				
	CSI1_D4	3				
	UART3_RTS	4				
	CSI0_D12	5				
C19	PG9	0/1	I/O			
	TS1_D5	2				
	CSI1_D5	3				
	UART3_CTS	4				
	CSI0_D13	5				
D18	PG10	0/1	I/O			
	TS1_D6	2				
	CSI1_D6	3				
	UART4_TX	4				
	CSI0_D14	5				
C18	PG11	0/1	I/O			
	TS1_D7	2				
	CSI1_D7	3				
	UART4_RX	4				
	CSI0_D15	5				
A6	PH0	0/1	I/O			
	LCD1_D0	2				
	ATAA0	3				
	UART3_TX	4				
	EINT0	6				
	CSI1_D0	7				
B6	PH1	0/1	I/O			
	LCD1_D1	2				
	ATAA1	3				
	UART3_RX	4				
	EINT1	6				
	CSI1_D1	7				
C6	PH2	0/1	I/O			
	LCD1_D2	2				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	ATAA2	3				
	UART3_RTS	4				
	EINT2	6				
	CSI1_D2	7				
A5	PH3	0/1	I/O			
	LCD1_D3	2				
	ATAIRQ	3				
	UART3_CTS	4				
	EINT3	6				
	CSI1_D3	7				
B5	PH4	0/1	I/O			
	LCD1_D4	1				
	ATAD0	2				
	UART4_TX	3				
	EINT4					
	CSI1_D4					
C5	PH5	0/1	I/O			
	LCD1_D5	2				
	ATAD1	3				
	UART4_RX	4				
	EINT5	6				
	CSI1_D5	7				
A4	PH6	0/1	I/O			
	LCD1_D6	2				
	ATAD2	3				
	UART5_TX	4				
	MS_BS	5				
	EINT6	6				
	CSI1_D6	7				
B4	PH7	0/1	I/O			
	LCD1_D7	2				
	ATAD3	3				
	UART5_RX	4				
	MS_CLK	5				
	EINT7	6				
	CSI1_D7	7				
C4	PH8	0/1	I/O			
	LCD1_D8	2				
	ATAD4	3				
	KP_IN0	4				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	MS_D0	5				
	EINT8	6				
	CSI1_D8	7				
D4	PH9	0/1	I/O			
	LCD1_D9	2				
	ATAD5	3				
	KP_IN1	4				
	MS_D1	5				
	EINT9	6				
	CSI1_D9	7				
A3	PH10	0/1	I/O			
	LCD1_D10	2				
	ATAD6	3				
	KP_IN2	4				
	MS_D2	5				
	EINT10	6				
	CSI1_D10	7				
B3	PH11	0/1	I/O			
	LCD1_D11	2				
	ATAD7	3				
	KP_IN3	4				
	MS_D3	5				
	EINT11	6				
	CSI1_D11	7				
C3	PH12	0/1	I/O			
	LCD1_D12	2				
	ATAD8	3				
	PS2_SCK1	4				
	EINT12	6				
	CSI1_D12	7				
A2	PH13	0/1	I/O			
	LCD1_D13	2				
	ATAD9	3				
	PS2_SDA1	4				
	SMC_RST	5				
	EINT13	6				
	CSI1_D13	7				
B2	PH14	0/1	I/O			
	LCD1_D14	2				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	ATAD10	3				
	PS2_KP_IN4	4				
	SMC_VPPEN	5				
	EINT14	6				
	CSI1_D14	7				
A1	PH15	0/1	I/O			
	LCD1_D15	2				
	ATAD11	3				
	KP_IN5	4				
	SMC_VPPPP	5				
	EINT15	6				
	CSI1_D15	7				
B1	PH16	0/1	I/O			
	LCD1_D16	2				
	ATAD12	3				
	KP_IN6	4				
	SMC_DET	5				
	EINT16	6				
	CSI1_D16	7				
C1	PH17	0/1	I/O			
	LCD1_D17	2				
	ATAD13	3				
	KP_IN7	4				
	SMC_VCCEN	5				
	EINT17	6				
	CSI1_D17	7				
C2	PH18	0/1	I/O			
	LCD1_D18	2				
	ATAD14	3				
	KP_OUT0	4				
	SMC_SLK	5				
	EINT18	6				
	CSI1_D18	7				
D1	PH19	0/1	I/O			
	LCD1_D19	2				
	ATAD15	3				
	KP_OUT1	4				
	SMC_SDA	5				
	EINT19	6				
	CSI1_D19	7				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
D2	PH20	0/1	I/O			
	LCD1_D20	2				
	ATAOE	3				
	CAN_TX	4				
	EINT20	6				
	CSI1_D20	7				
D3	PH21	0/1	I/O			
	LCD1_D21	2				
	ATADREQ	3				
	CAN_RX	4				
	EINT21	6				
	CSI1_D21	7				
E1	PH22	0/1	I/O			
	LCD1_D22	2				
	ATADACK	3				
	KP_OUT2	4				
	CSI1_D22	5				
	SDC1_CMD	7				
E2	PH23	0/1	I/O			
	LCD1_D23	2				
	ATACS0	3				
	KP_OUT3	4				
	SDC1_CLK	5				
	CSI1_D23	7				
E3	PH24	0/1	I/O			
	LCD1_CLK	2				
	ATACS1	3				
	KP_OUT4	4				
	SDC1_D0	5				
	CSI1_PCLK	7				
E4	PH25	0/1	I/O			
	LCD1_DE	2				
	ATAIORDY	3				
	KP_OUT5	4				
	SDC1_D1	5				
	CSI1_FIELD	7				
F3	PH26	0/1	I/O			
	LCD1_HSYNC	2				
	ATAIORDY	3				
	KP_OUT6	4				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	SDC1_D2	5				
	CSI1_HSYNC	7				
F4	PH27	0/1	I/O			
	LCD1_VSYNC	2				
	ATAIOW	3				
	KP_OUT7	4				
	SDC1_D3	5				
	CSI1_VSYNC	7				
A20	PI0	0/1	I/O			
	NC	2				
B20	PI1	0/1	I/O			
	NC	2				
A19	PI2	0/1	I/O			
	NC	2				
B19	PI3	0/1	I/O			
	PWM1	2				
A18	PI4	0/1	I/O			
	SDC3_CMD	2				
B18	PI5	0/1	I/O			
	SDC3_CLK	2				
A17	PI6	0/1	I/O			
	SDC3_D0	2				
B17	PI7	0/1	I/O			
	SDC3_D1	2				
A16	PI8	0/1	I/O			
	SDC3_D2	2				
B16	PI9	0/1	I/O			
	SDC3_D3	2				
C17	PI10	0/1	I/O			
	SPI0_CS0	2				
	UART5_TX	3				
	EINT22	6				
D17	PI11	0/1	I/O			
	SPI0_CLK UART5_RX	2 3				
	EINT23	6				
C16	PI12	0/1	I/O			
	SPI0_MOSI	2				
	UART6_TX	3				
	EINT2	6				
D16	PI13	0/1	I/O			

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
	SPI0_MISO	2				
	UART6_RX	3				
	EINT25	6				
C15	PI14	0/1	I/O			
	SPI0_CS1	2				
	PS2_SCK1	3				
	TCLKIN0	4				
	EINT26	6				
D15	PI15	0/1	I/O			
	SPI1_CS1	2				
	PS2_SDA1	3				
	TCLKIN1	4				
	EINT27	6				
E17	PI16	0/1	I/O			
	SPI1_CS0	2				
	UART2_RTS	3				
	EINT28	6				
E16	PI17	0/1	I/O			
	SPI1_CLK	2				
	UART2_CTS	3				
	EINT29	6				
E15	PI18	0/1	I/O			
	SPI1_MOSI	2				
	UART2_TX	3				
	EINT30	6				
D14	PI19	0/1	I/O			
	SPI1_MISO	2				
	UART2_RX	3				
	EINT31	6				
E14	PI20	0/1	I/O			
	PS2_SCK0	2				
	UART7_TX	3				
	HSCL	6				
E13	PI21	0/1	I/O			
	PS2_SDA0	2				
	UART7_RX	3				
	HSDA	6				
T9	GND		I		pull-up	
W8	UBOOT_SEL		I		pull-up	
T10	JTAG_SEL	0/1	I/O		pull-up	

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
H16	TEST	0	I/O		pull-down	
F5	NMI#	0	A			
C14	RESET#	0	A			
N20	DM0	0/1	IO			
N21	DP0	0/1	IO			
P20	DM1	0	PWR	-	-	-
P21	DP1	0	GND	-	-	-
L16	UVCC_C	0	PWR	-	-	-
L14	UGND_C	0	GND	-	-	-
L15	UVCC_T	0/1	PWR			
L13	UGND_T	0/1	GND			
K16	ULVDD		PWR			
K14	ULGND		GND			
R20	DM2		IO			
R21	DP2		IO			
Y22	XP_TP	0	AI			
AA22	XN_TP	0	AI			
Y23	YP_TP	0	AI			
AA23	YN_TP	0	AI			
AC23	MIC1OUTN	0				
AC22	MIC1OUTP	0				
Y21	FMINR	0				
Y20	FMINL	0				
AA21	VMIC	0		-		-
AC21	MICIN2	0		-		-
AC20	MICIN1	0		-		-
W20	VRA1	0				
V20	VRA2	0				
T19	AVCC	0				
W21	VRP	0				
AB21	LINEINR	0		-		-
AB20	LINEINL	0				
U19	AGND	0				
W19	HPR	0				
Y19	HPL	0				
V19	HPGND	0				
AA20	HPCOMFB	0				
AC19	HPVCC	0				
Y19	HPL	0				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
AB23	LRADC0	0	AI			
AB22	LRADC1	0	AI			
AC16	TVOUT0	0	AO			
AB16	TVOUT1	0	AO			
AC17	TVOUT2	0	AO			
AB17	TVOUT3	0	AO			
W15	VCC33_TVOUT	0	PWR	-	-	-
W18	GND33_TVOUT	0	GND	-	-	-
AC18	NC	0				
AB18	NC	0				
AA17	NC	0				
Y17	NC	0				
W16	NC	0				
Y18	NC	0				
W17	NC	0				
AA18	NC	0				
AA16	NC	0				
Y16	NC	0				
V23	TX0P_HDMI	0				
V22	TX0N_HDMI	0				
U23	TX1P_HDMI	0				
U22	TX1N_HDMI	0				
T23	TX2P_HDMI	0				
T22	TX2N_HDMI	0				
W23	TXCP_HDMI	0				
W22	TXCN_HDMI	0				
T13	VP_HDMI	0				
P13/R13/P14	GND_HDMI	0				
R23	SCL_HDMI	0				
R22	SDA_HDMI	0				
P22	HPD_HDMI	0				
P23	CEC_HDMI	0				
R14/T14	NC					
T20	NC	0				
T21	NC	0				
U21	NC	0				
U20	NC	0				
V21	NC	0				
P19/R19	NC	0				
M16/M15	NC	0				

BALL#	Pin Name	Function	Type	Reset State	Pull Up/Down	Buffer Strength (mA)
N15/N16	NC	0				
M14/N13	NC	0				
F1	CLK32K_IN	0	A			
F2	CLK32K_OUT	0	A			
K8	RTC_VDD	0	PWR	-	-	-
N23	CLK24M_IN	0	A			
N22	CLK24M_OUT	0	A			
R16/T16/R15/T15	NC	0	PWR	-	-	-
P16	PLLVP25	0				
P15	PLLGND	0	GND	-	-	-
H8/H9/H10 J8/J9/J10 J14/H15	VCC(8)	0	PWR	-	-	-
N19	VCC_CARD	0	PWR	-	-	-
H19/J19	VCC_NAND(2)	0	PWR	-	-	-
G5/H5/L5/M5/ R5/T5/ W5/W6/W7/Y6/	VCC_ DRAM (10)	0	PWR	-	-	-
J5/k5/N5/P5/ U5/V5/Y7/ Y8/G3/G4	GND_DRAM (10)	0	GND	-	-	-
J12/J13/H11/ H12/H13/H14	VDDCPU(6)					
T8/R9/R10 L8/L9/K9/K10 K15/J15/J16	VDD_INT(10)					
L10/L11/L12/ K11/K12/K13/ J11/M10/M11/ M12/M13/N11/N12/ P11/P12/R11/R12/ T11/T12	GND(19)	0	GND		-	-
W12/W13/W14	VCC_ LVDS (3)	0	PWR	-	-	-
W9/W10/W11	GND_LVDS (3)	0	GND	-	-	-
F19	VCC_CSI0					
E18	VCC_CSI1					

Table 5-1 Pin Characteristics (FBGA441)

5.2. Multiplexing Characteristics

The following tables provide a description of the A10 multiplexing on the FBG441 package.

Port A(PA)	Multiplex Function Select					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi 7
PA0	ERXD3	SPI1_CS0	UART2_RTS			
PA1	ERXD2	SPI1_CLK	UART2_CTS			
PA2	ERXD1	SPI1_MOSI	UART2_TX			
PA3	ERXD0	SPI1_MISO	UART2_RX			
PA4	ETXD3	SPI1_CS1				
PA5	ETXD2	SPI3_CS0				
PA6	ETXD1	SPI3_CLK				
PA7	ETXD0	SPI3_MOSI				
PA8	ERXCK	SPI3_MISO				
PA9	ERXERR	SPI3_CS1				
PA10	ERXDV		UART1_TX			
PA11	EMDC		UART1_RX			
PA12	EMDIO	UART6_TX	UART1_RTS			
PA13	ETXEN	UART6_RX	UART1_CTS			
PA14	ETXCK	UART7_TX	UART1_DTR			
PA15	ECRS	UART7_RX	UART1_DSR			
PA16	ECOL	CAN_TX	UART1_DCD			
PA17	ETXERR	CAN_RX	UART1_RING			

Table 5-1 Port A(PA)Multiplexing Function Select Table

Port B(PB)	Multiplex Function Select					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PB0	TWI0_SCK					
PB1	TWI0_SDA					

PB2	PWM0					
PB3	IR0_TX		NC			
PB4	IR0_RX					
PB5	I2S_MCLK	AC97_MCLK				
PB6	I2S_BCLK	AC97_BCLK				
PB7	I2S_LRCK	AC97_SYNC				
PB8	I2S_DO0	AC97_DO				
PB9	I2S_DO1					
PB10	I2S_DO2					
PB11	I2S_DO3					
PB12	I2S_DI	AC97_DI	NC			
PB13	SPI2_CS1		NC			
PB14	SPI2_CS0	JTAG_MS0				
PB15	SPI2_CLK	JTAG_CK0				
PB16	SPI2_MOSI	JTAG_DO0				
PB17	SPI2_MISO	JTAG_DI0				
PB18	TWI1_SCK					
PB19	TWI1_SDA					
PB20	TWI2_SCK					
PB21	TWI2_SDA					
PB22	UART0_TX	IR1_TX				
PB23	UART0_RX	IR1_RX				

Table 5-3 Port B(PB) Multiplex Function Select Table

Port C(PC)	**Multiplex Function Select**					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PC0	NWE#	SPI0_MOSI				
PC1	NALE	SPI0_MISO				
PC2	NCLE	SPI0_CLK				
PC3	NCE1					
PC4	NCE0					
PC5	NRE#					

PC6	NRB0	SDC2_CMD				
PC7	NRB1	SDC2_CLK				
PC8	NDQ0	SDC2_D0				
PC9	NDQ1	SDC2_D1				
PC10	NDQ2	SDC2_D2				
PC11	NDQ3	SDC2_D3				
PC12	NDQ4					
PC13	NDQ5					
PC14	NDQ6					
PC15	NDQ7					
PC16	NWP					
PC17	NCE2					
PC18	NCE3					
PC19	NCE4	SPI2_CS0				
PC20	NCE5	SPI2_CLK				
PC21	NCE6	SPI2_MOSI				
PC22	NCE7	SPI2_MISO				
PC23		SPI0_CS0				

Table 5-4 Port C(PC) Multiplex Function Select Table

Port D(PD)	**Multiplex Function Select**					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PD0	LCD0_D0	LVDS0_VP0				
PD1	LCD0_D1	LVDS0_VN0				
PD2	LCD0_D2	LVDS0_VP1				
PD3	LCD0_D3	LVDS0_VN1				
PD4	LCD0_D4	LVDS0_VP2				
PD5	LCD0_D5	LVDS0_VN2				
PD6	LCD0_D6	LVDS0_VPC				
PD7	LCD0_D7	LVDS0_VNC				
PD8	LCD0_D8	LVDS0_VP3				
PD9	LCD0_D9	LVDS0_VN3				

PD10	LCD0_D10	LVDS1_VP0				
PD11	LCD0_D11	LVDS1_VN0				
PD12	LCD0_D12	LVDS1_VP1				
PD13	LCD0_D13	LVDS1_VN1				
PD14	LCD0_D14	LVDS1_VP2				
PD15	LCD0_D15	LVDS1_VN2				
PD16	LCD0_D16	LVDS1_VPC				
PD17	LCD0_D17	LVDS1_VNC				
PD18	LCD0_D18	LVDS1_VP3				
PD19	LCD0_D19	LVDS1_VN3				
PD20	LCD0_D20	CSI1_MCLK				
PD21	LCD0_D21	SMC_VPPEN				
PD22	LCD0_D22	SMC_VPPPP				
PD23	LCD0_D22	SMC_DET				
PD24	LCD0_CLK	SMC_VCCEN				
PD25	LCD0_DE	SMC_RST				
PD26	LCD0_HSYNC	SMC_SLK				
PD27	LCD0_VSYNC	SMC_SDA				

Table 5-5 Port D(PD) Multiplex Function Select Table

Port E(PE)	**Multiplex Function Select**					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PE0	TS0_CLK	CSI0_PCLK				
PE1	TS0_ERR	CSI0_MCLK				
PE2	TS0_SYNC	CSI0_HSYNC				
PE3	TS0_DVLD	CSI0_VSYNC				
PE4	TS0_D0	CSI0_D0				
PE5	TS0_D1	CSI0_D1				
PE6	TS0_D2	CSI0_D2				
PE7	TS0_D3	CSI0_D3				
PE8	TS0_D4	CSI0_D4				
PE9	TS0_D5	CSI0_D5				

PE10	TS0_D6	CSI0_D6				
PE11	TS0_D7	CSI0_D7				
PE12	TS0_CLK	CSI0_PCLK				
PE13	TS0_ERR	CSI0_MCLK				
PE14	TS0_SYNC	CSI0_HSYNC				
PE15	TS0_DVLD	CSI0_VSYNC				
PE16	TS0_D0	CSI0_D0				
PE17	TS0_D1	CSI0_D1				
PE18	TS0_D2	CSI0_D2				
PE19	TS0_D3	CSI0_D3				
PE20	TS0_D4	CSI0_D4				
PE21	TS0_D5	CSI0_D5				
PE22	TS0_D6	CSI0_D6				
PE23	TS0_D7	CSI0_D7				
PE24	TS0_CLK	CSI0_PCLK				
PE25	TS0_ERR	CSI0_MCLK				
PE26	TS0_SYNC	CSI0_HSYNC				
PE27	TS0_DVLD	CSI0_VSYNC				
PE28	TS0_D0	CSI0_D0				
PE29	TS0_D1	CSI0_D1				
PE30	TS0_D2	CSI0_D2				
PE31	TS0_D3	CSI0_D3				

Table 5-6 Port E(PE) Multiplex Function Select Table

Port F(PF)	**Multiplex Function Select**					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PF0	SDC0_D1		JTAG_MS1			
PF1	SDC0_D0		JTAG_DI1			
PF2	SDC0_CLK		UART0_TX			
PF3	SDC0_CMD		JTAG_DO1			
PF4	SDC0_D3		UART0_RX			
PF5	SDC0_D2		JTAG_CK1			

Table 5-7 Port F(PF) Multiplex Function Select Table

Port G(PG)	Multiplex Function Select					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PG0	TS1_CLK	CSI1_PCLK	SDC1_CMD			
PG1	TS1_ERR	CSI1_MLCK	SDC1_CLK			
PG2	TS1_SYNC	CSI1_HSYNC	SDC1_D0			
PG3	TS1_DVLD	CSI1_VSYNC	SDC1_D1			
PG4	TS1_D0	CSI1_D0	SDC1_D2	CSI0_D8		
PG5	TS1_D1	CSI1_D1	SDC1_D3	CSI0_D9		
PG6	TS1_D2	CSI1_D2	UART3_TX	CSI0_D10		
PG7	TS1_D3	CSI1_D3	UART3_RX	CSI0_D11		
PG8	TS1_D4	CSI1_D4	UART3_RTS	CSI0_D12		
PG9	TS1_D5	CSI1_D5	UART3_CTS	CSI0_D13		

Table 5-8 Port G(PG) Multiplex Function Select Table

Port H (PH)	Multiplex Function Select					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PH0	LCD1_D0	ATAA0	UART3_TX		EINT0	CSI1_D0
PH1	LCD1_D1	ATAA1	UART3_RX		EINT1	CSI1_D1
PH2	LCD1_D2	ATAA2	UART3_RTS		EINT2	CSI1_D2
PH3	LCD1_D3	ATAIRQ	UART3_CTS		EINT3	CSI1_D3
PH4	LCD1_D4	ATAD0	UART4_TX		EINT4	CSI1_D4
PH5	LCD1_D5	ATAD1	UART4_RX		EINT5	CSI1_D5
PH6	LCD1_D6	ATAD2	UART5_TX		EINT6	CSI1_D6
PH7	LCD1_D7	ATAD3	UART5_RX		EINT7	CSI1_D7
PH8	LCD1_D8	ATAD4	KP_IN0		EINT8	CSI1_D8
PH9	LCD1_D9	ATAD5	KP_IN1		EINT9	CSI1_D9
PH10	LCD1_D10	ATAD6	KP_IN2		EINT10	CSI1_D10
PH11	LCD1_D11	ATAD7	KP_IN3		EINT11	CSI1_D11
PH12	LCD1_D12	ATAD8	PS2_SCK1		EINT12	CSI1_D12
PH13	LCD1_D13	ATAD9	PS2_SDA1	SMC_RST	EINT13	CSI1_D13

PH14	LCD1_D14	ATAD10	KP_IN4	SMC_VPPEN	EINT14	CSI1_D14
PH15	LCD1_D15	ATAD11	KP_IN5	SMC_VPPPP	EINT15	CSI1_D15
PH16	LCD1_D16	ATAD12	KP_IN6	SMC_DET	EINT16	CSI1_D16
PH17	LCD1_D17	ATAD13	KP_IN7	SMC_VCCEN	EINT17	CSI1_D17
PH18	LCD1_D18	ATAD14	KP_OUT0	SMC_SLK	EINT18	CSI1_D18
PH19	LCD1_D19	ATAD15	KP_OUT1	SMC_SDA	EINT19	CSI1_D19
PH20	LCD1_D20	ATAOE	CAN_TX		EINT20	CSI1_D20
PH21	LCD1_D21	ATADREQ	CAN_RX		EINT21	CSI1_D21
PH22	LCD1_D22	ATADACK	KP_OUT2	SDC1_CMD		CSI1_D22
PH23	LCD1_D23	ATACS0	KP_OUT3	SDC1_CLK		CSI1_D23
PH25	LCD1_CLK	ATACS1	KP_OUT4	SDC1_D0		CSI1_PCLK
PH26	LCD1_DE	ATAIORDY	KP_OUT5	SDC1_D1		CSI1_FIELD
PH27	LCD1_HSYNC	ATAIOR	KP_OUT6	SDC1_D2		CSI1_HSYNC

Table 5-9 Port H(PH) Multiplex Function Select Table

Port I(PI)	**Multiplex Function Select**					
	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PI0	NC					
PI1	NC					
PI2	NC					
PI3	PWM1					
PI4	SDC3_CMD					
PI5	SDC3_CLK					
PI6	SDC3_D0					
PI7	SDC3_D1					
PI18	SDC3_D2					
PI19	SDC3_D3					
PI10	SPI0_CS0	UART5_TX			EINT22	
PI11	SPI0_CLK	UART5_RX			EINT23	
PI12	SPI0_MOSI	UART6_TX			EINT24	

Table 5-10 Port I(PI) Multiplex Function Select Table

5.3. Power and Miscellaneous Signals

Many signals are available on multiple pins according to the software configuration of the multiplexing options.

1. Signal Name: The signal name
2. Description: Description of the signal
3. Type: type = Pin type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance
   - A = Analog
   - PWR = Power
   - GND = Ground
4. Pin #: Associated ball(s) number

5.3.1. Power Domain Signal Description

Signal Name	Description	Pin Name	Ball#
TV-OUT DAC Power			
TV-VCC	TV-OUT Power Supply	TV-VCC	R14
TV-GND	TV-OUT Ground	TV-GND	N12
Audio DAC Power			
HPVCC	Audio output DAC Power Supply	HPVCC	Y14
HPVCC_IN	Audio output DAC Power Supply	HPVCC_IN	W14
HPGND	Audio output DAC Ground	HPGND	N11
Audio ADC Power			
VMIC	Microphone ADC Power Supply	VMIC	V17
USB Power			
UVCC0	USB0 PHY Analog Power Supply	UVCC0	P17
ULVDD0	USB0 Digital Power Supply	ULVDD0	T16
UVCC_C	USB1 PHY Analog Power Supply	UVCC_C	P16
UVCC_T	USB2 PHY Analog Power Supply	UVCC_T	R16
ULVDD1	USB1/2 Digital Power Supply	ULVDD1	U16
UGND0	USB0 PHY Analog Ground	UGND0	K12
ULGND0	USB0 Digital Ground	ULGND0	L13
UGND_C	USB1 PHY Analog Ground	UGND_C	L12
UGND_T	USB2 PHY Analog Ground	UGND_T	M13
ULGND1	USB1/2 Digital Ground	ULGND1	M12
RTC Power			
RTC_VDD	RTC Power Supply	RTC_VDD	V13
PLL Power			
PLL_VDD	PLL Power Supply	PLL_VDD	V20

Signal Name	Description	Pin Name	Ball#
PLL_GND	PLL Ground	PLL_GND	N13
Core Power			
VDD	Core Chip Power Supply	VDD(13)	H8\J8\K8\K9\K10\J10\ H10\H9\J9\M8\M9\N8\N9
GND	Core Chip Ground	GND(13)	L8\L9\L10\M10\ N10\L11\K11\J11\ H11\J12\J13\H13\H12
IO Power			
VCC	IO Power Supply	VCC(10)	K7\L7\M7\N7\P7\P8\ P9\P10\H7\J7
Card Power			
Card VCC	Card Power Supply	Card VCC	U12
NAND Power			
NAND_VCC	NAND Flash Power Supply	NAND_VCC(2)	G10\G7
DRAM Power			
DRAM_VCC	DRAM Power Supply	DRAM_VCC(10)	H16\G16\G15\F16\ F15\E16\E15\E14\ F14\E13
DRAM_GND	DRAM Ground	DRAM_GND(10)	K15\K14\J14\H14\ G14\G13\G12\G11\ F12\F11
LVDS Power			
LVDS_VCC	LVDS Power Supply	LVDS_VCC(1)	P18
LVDS_GND	LVDS Ground	LVDS_GND(1)	K13
Analog Power			
AVCC	Analog Power Supply	AVCC(1)	Y19
AGND	Analog Ground	AGND(1)	M11

Table 5-11 Power Domain Signal Description

5.3.2. Miscellaneous Signal Description

Signal Name	Description	Type	Pin Name	Ball#
JTAG Interface				
JTAG_SEL0	JTAG port Select bit0	I	JTAG0#	R8
JTAG_SEL1	JTAG port Select bit1	I	JTAG1#	R9
JTAG Port 0				
JTAG_MS0	JTAG Mode Select	I	PB14	P11
JTAG_CK0	JTAG Clock	I	PB15	R11
JTAG_DO0	JTAG test DataOutput	O	PB16	T11
JTAG_DI0	JTAG test Data Input	I	PB17	U11
JTAG Port 1				
JTAG_MS1	JTAG Mode Select	I	PF0	V11
JTAG_CK1	JTAG Clock	I	PF5	V12
JTAG_DO1	JTAG test DataOutput	O	PF11	W11
JTAG_DI1	JTAG test Data Input	I	PF3	Y12
Clock				
HOSCI	Main 24MHz crystal Input for internal OSC	AI	HOSCI	W20
HOSCO	Main 24MHz crystal Output for internal OSC	AO	HOSCO	Y20
LOSCI	32K768Hz crystal Input for RTC	AI	LOSCI	Y13
LOSCO	32K768Hz crystal Output for RTC	AO	LOSCO	W13
Reset				
RESET#	System Reset	AI	RESET#	T12
FIQ				
NMI#	External Fast Interrupt Request	I	NMI#	R12
Boot				
BOOT_SEL	Boot Mode Select	I	BOOTS	P12
Test				
TEST	Test Pin(Pull down Internal default)	I	TEST	G6
Others				
BIAS	Bias of the CPU connect a 200Kohm Resistor to ground	A	BIAS	Y18
VRP	=AVCC=3.0V	A	VRP	W19
VRA1	=1.5V	A	VRA1	W18
VRA2	=0V	A	VRA2	V18

Signal Name	Description	Type	Pin Name	Ball#
NC	Not Connected	NC(27)	NC	E11\E12\F13\H15\ J15\J16\K16\L14\ L15\L16\L17\L18\ L19\L20\M14\M15\ M16\M17\M18\N16\ N17\N18\R15\U17\ U18\V16\V19

Table 5-12 Miscellaneous Signal Description

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 6-1) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the A10.

Note: Absolute maximum ratings are not operating ranges. Operation at absolute maximum ratings is not guaranteed.

Symbol	Parameter		Min	Typ	Unit
TS	Storage Temperature		-20	125	℃
II/O	In/Out current for input and output		/	/	mA
VESD	ESD stress voltage	HBM(human body model)		/	VESD
		CDM(charged device model)	-	-	
VCC	DC Supply Voltage for I/O		2.7	3.3	V
VDD	DC Supply Voltage for Internal Digital Logic		1.0	1.3	V
VCC_ANALOG	DC Supply Voltage for Analog Part		2.7	3.3	V
VCC_DRAM	DC Supply Voltage for DRAM Part		1.3	2.0	V
VCC_USB	DC Supply Voltage for USB PHY		2.7	3.3	V
VCC_TV	DC Supply Voltage for TV-OUT DAC		2.7	3.3	V
VCC_LRADC	DC Supply Voltage for LRADC		3.0	3.0	V
VCC_HP	DC Supply Voltage for Audio DAC		2.7	3.3	V
VDD_PLL	DC Supply Voltage for PLL		1.2	1.3	V
VDD_RTC	DC Supply Voltage for RTC		1.2	1.3	V

Table 6-1 Multiplexing Characteristics

6.2. Recommended Operating Conditions

All A10 modules are used under the operating Conditions contained in Table 6-2.

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Operating Temperature[Commercial]	-25	–	+85	℃
	Operating Temperature[Extended]	-40	–	+85	℃
GND	Ground	0	0	0	V
VCC	DC Supply Voltage for I/O	/	3.3	/	V
VDD	DC Supply Voltage for Internal Digital Logic	/	1.2	/	V
VCC_ANALOG	DC Supply Voltage for Analog Part	/	3.0	/	V
VCC_DRAM	DC Supply Voltage for DRAM Part	/	1.5	/	V
VCC_USB	DC Supply Voltage for USB PHY	/	3.3	/	V
VCC_TV	DC Supply Voltage for TV-OUT DAC	/	3.3	/	V
VDD_RTC	DC Supply Voltage for RTC	/	1.25	/	V

Table 6-2 Recommended Operating Conditions

6.3. DC Electrical Characteristics

Table 6-3 summarized the DC electrical characteristics of A10.

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level input voltage	2.4	3.0	3.3	V
VIL	Low-level input voltage	0	0.5	1.0	V
VHYS	Hysteresis voltage	/	/	/	mV
IIH	High-level input current	/	/	/	uA
IIL	Low-level input current	/	/	/	uA
VOH	High-level output voltage	3.3	3.3	3.3	V
VOL	Low-level output voltage	0	0	0	V
IOZ	Tri-State Output Leakage Current	/	/	/	uA
CIN	Input capacitance	/	/	/	pF
COUT	Output capacitance	/	/	/	pF

Table 6-3 DC Electrical Characteristics

6.4. Oscillator Electrical Characteristics

The A10 contains two oscillators: a 24.000 MHz oscillator and a 32.768kHz oscillator. Each oscillator requires a specific crystal.

The A10 device operation requires the following two input clocks:

- The 32.768kHz frequency is used for low frequency operation.
- The 24.000MHz frequency is used to generate the main source clock of the A10 device.

6.4.1. 24MHz Oscillator Characteristics

The 24.0MHz crystal is connected between the HOSCI (amplifier input) and HOSCO (amplifier output). Table 6-4 lists the 24.MHz crystal specifications.

Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range		24.000		MHz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 ℃	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm

PON	Drive level	–	–	50	uW
CL	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
RS	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
CM	Motional capacitance	–	–		pF
CSHUT	Shunt capacitance	–	–		pF
RBIAS	Internal bias resistor				MΩ

Table 6-4 24MHz Oscillator Characteristics

6.4.2. 32.768kHz Oscillator Characteristics

The 32.768kHz crystal is connected between the LOSCI (amplifier input) and LOSCO (amplifier output). Table 6-5 lists the 32.768kHz crystal specifications.

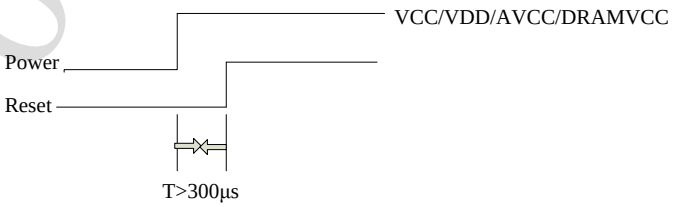
Symbol	Parameter	Min	Typ	Max	Unit
1/(tCPMAIN)	Crystal Oscillator Frequency Range		32.768		MHz
tST	Startup Time	–	–		ms
	Frequency Tolerance at 25 ℃	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
PON	Drive level	–	–	50	uW
CL	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
RS	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
CM	Motional capacitance	–	–		pF
CSHUT	Shunt capacitance	–	–		pF
RBIAS	Internal bias resistor				MΩ

Table 6-5 32.768kHz Oscillator Characteristics

6.5. Power up/down and Reset Specifications

This section includes specification for the following:

- Power-up sequence
- Power-down sequence



6.5.1. Power-up Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation. Figure 6-x shows this sequence and is detailed in Table 6-x

6.5.2. Power-down Sequence

The sequence indicated in Figure 6-x and detailed in Table 6-x is the required timing parameters for power-dow

7. Clock Controller

The clock controller provides management for clock generation, division, distribution, synchronization and gating. It consists of 7PLLs, 24MHz crystal, an on-chip RC Oscillator and a 32768Hz low power crystal Oscillator. The 24MHz crystal Oscillator is mandatory and generates input clock source for PLLs and main digital blocks, while it is recommended to use low-power and accurate 32768Hz crystal Oscillator for RTC.

7.1. Clock Tree Diagram

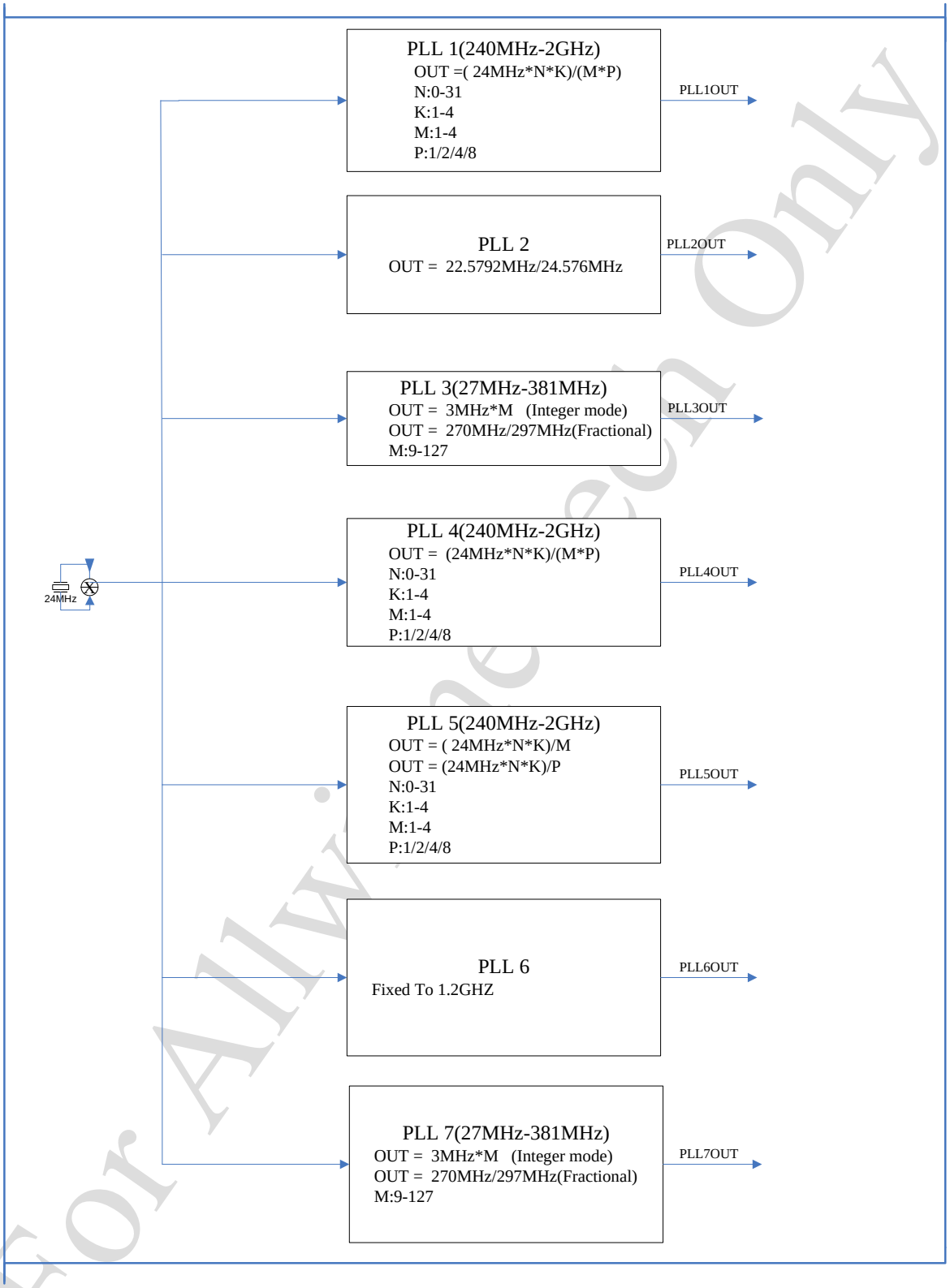


Figure7-1 Clock Generation from PLL Outputs

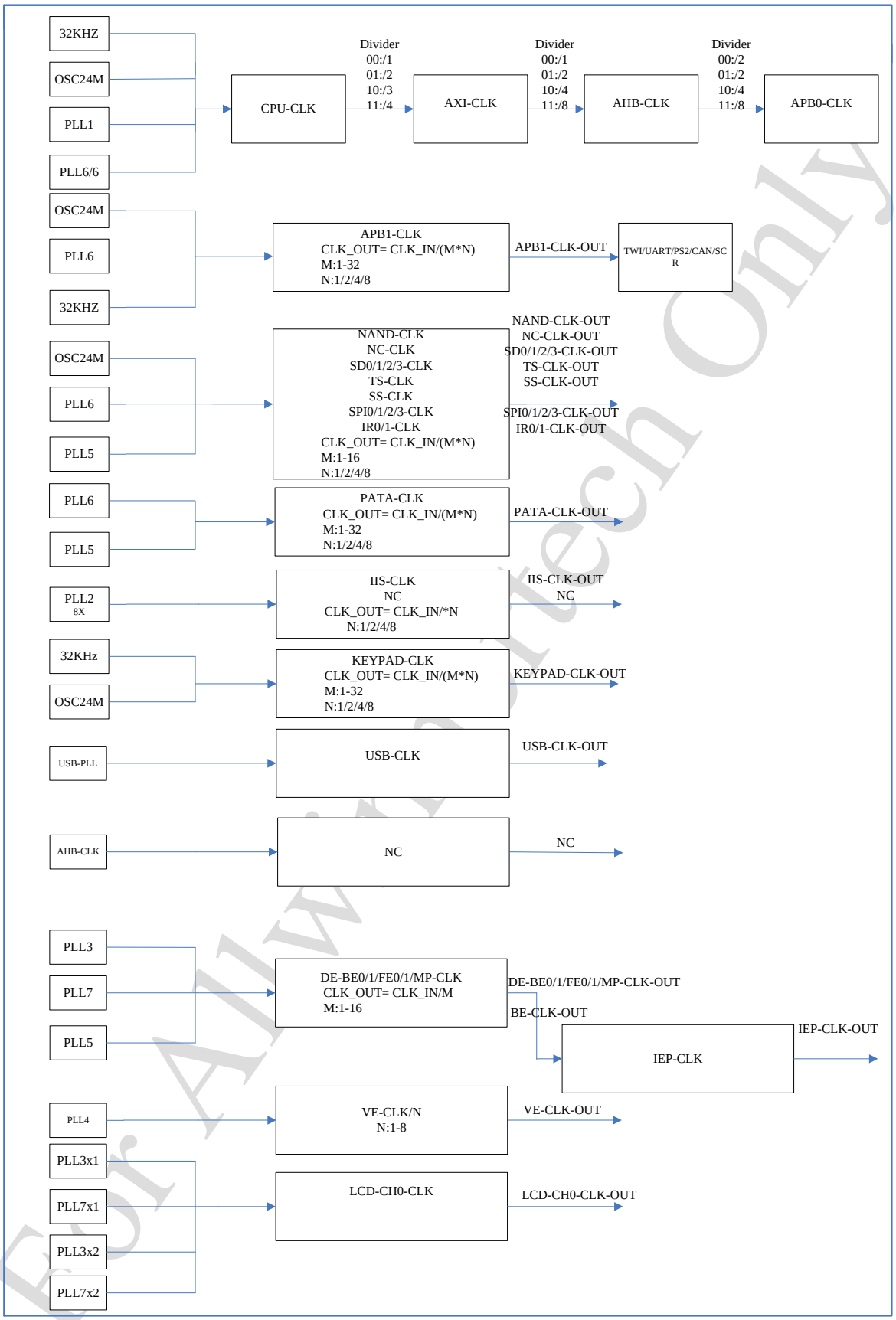


Figure 7-2 Bus Clock Generation (I)

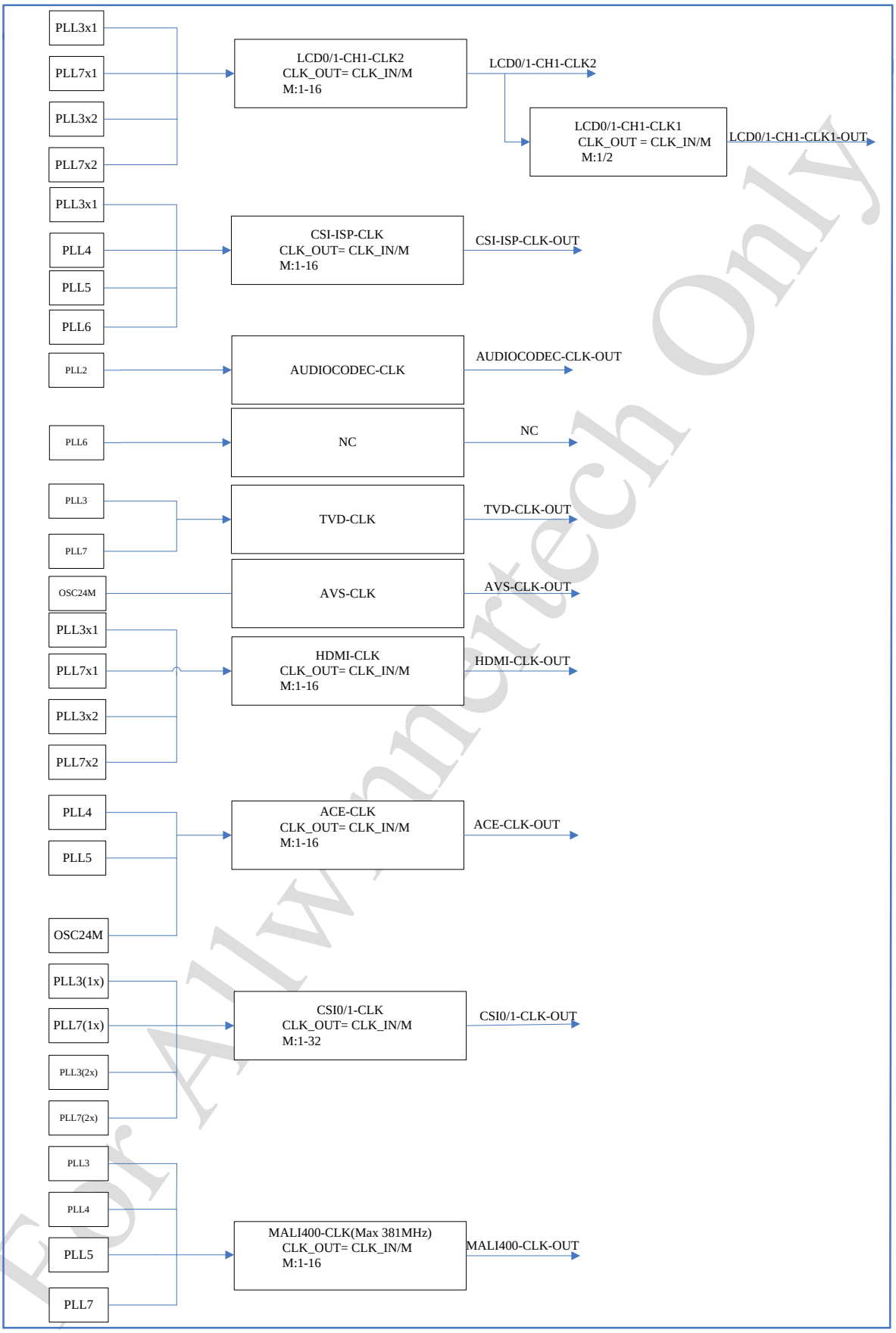


Figure 7-3 Bus Clock Generation (II)

8. PWM

8.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to active state and count from 0x0000.

The PWM divider divides the clock(24MHz) by 1-4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode,the output will be a square waveform,the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

8.2. PWM Signal Description

Signal Name	Description	Type	Pin Name	Ball#
PWM0	PWM output for port 0	O	PB2	B1
PWM1	PWM output for port 1	O	PI3	G5

Table 8-1 PWM Signal Description

9. Timer Controller

9.1. Overview

The chip implements 6 timers. Timer 0 and 1 can take their inputs from internal RC oscillator, external 32768Hz crystal or OSC24M. They provide the operating system's scheduler interrupt. They are designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode. Timer 2 is used for OS to generate a periodic interrupt.

The Watchdog timer is a timing device that resumes the controller operation after malfunctioning due to noise and system errors. The watchdog timer can be used as a normal 16-bit interval timer to request interrupt service. The watchdog timer generates a general reset signal.

The Real Time Clock (RTC) can be used as a calendar. RTC can operate using the backup battery while the system power is off. Although power is off, backup battery can store the time by Second, Minute, Hour (HH-MM-SS), Day, Month, and Year (YY-MM-DD) data. It has a built-in leap year generator and an independent power pin (RTCVDD).

The Alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated.

10. Interrupt Controller

10.1. Overview

The Interrupt Controller in A10 can handle individually maskable interrupt sources up to 95. With the 4-level programmable interrupt priority, developer can define the priority for each interrupt source, permitting higher priority interrupts to be serviced even if a lower priority interrupt is being treated.

The Interrupt Controller is featured as following:

- Support 95 vectored nIRQ interrupt
- 4 programmable interrupt priority levels
- Fixed interrupt priority of the same level
- Support Hardware interrupt priority level masking
- Programmable interrupt priority level masking
- Generates IRQ and FIQ
- Generates Software interrupt
- One external NMI interrupt source

10.2. External Interrupt Signal Description

Signal Name	Description	Type	Pin Name	Ball#
EINT0	External Interrupt source 0	I	PG0	T19
EINT1	External Interrupt source 1	I	PG1	T20
EINT2	External Interrupt source 2	I	PG2	R19
EINT3	External Interrupt source 3	I	PG3	R20
EINT4	External Interrupt source 4	I	PG4	P19
EINT5	External Interrupt source 5	I	PG5	P20
EINT6	External Interrupt source 6	I	PG6	N19
EINT7	External Interrupt source 7	I	PG7	N20
EINT8	External Interrupt source 8	I	PG8	M19
EINT9	External Interrupt source 9	I	PG9	M20
EINT10	External Interrupt source 10	I	PE24	T1
EINT11	External Interrupt source 11	I	PE25	T2
EINT12	External Interrupt source 12	I	PC19	C10
EINT13	External Interrupt source 13	I	PC20	G9
EINT14	External Interrupt source 14	I	PC21	F9
EINT15	External Interrupt source 15	I	PC22	E9
EINT16	External Interrupt source 16	I	PB3	G4
EINT17	External Interrupt source 17	I	PB9	E3
EINT18	External Interrupt source 18	I	PB10	E2
EINT19	External Interrupt source 19	I	PB11	E1

Signal Name	Description	Type	Pin Name	Ball#
EINT20	External Interrupt source 20	I	PB18	T3
EINT21	External Interrupt source 21	I	PB19	T4
EINT22	External Interrupt source 22	I	PB20	P1
EINT23	External Interrupt source 23	I	PB21	P2
EINT24	External Interrupt source 24	I	PH0	C6
EINT25	External Interrupt source 25	I	PH1	D6
EINT26	External Interrupt source 26	I	PH2	E6
EINT27	External Interrupt source 27	I	PH3	F6
EINT28	External Interrupt source 28	I	PI4	D3
EINT29	External Interrupt source 29	I	PI5	A2
EINT30	External Interrupt source 30	I	PI6	T7
EINT31	External Interrupt source 31	I	PI7	U7

Table10-1 External Interrupt Signal Description

11. DMA Controller

11.1. Overview

Many peripherals on the A10 use direct memory access (DMA) transfers. There are two kinds of DMA, namely, Normal DMA and Dedicated DMA. For Normal DMA, ONLY one channel can be activated and the sequence is determined by the priority level. For Dedicated DMA, at most 8-channels can be activated at the same time as long as there is conflict of their source or destination.

Both Normal DMA and Dedicated DMA can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be consistently aligned. Although the increase mode of Normal DMA should be address aligned, there is no need for its byte counter always goes in multiple. The Dedicated DMA can only transfer data between DRAM and modules. DMA Source Address, Destination Address can be modified even if DMA transfers have started.

12. NAND Flash Controller

12.1. Overview

The NFC is the NAND Flash Controller which supports all NAND/MLC flash memory available in the market. New type flash can be supported by software re-configuration. The NFC can support 8 NAND flash with 1.8/3.3 V voltage supply. There are 8 separate chip select lines (CE#) for connecting up to 8 flash chips with2 R/B signals.

The On-the-fly error correction code (ECC) is built-in NFC for enhancing reliability. BCH is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control for reading or writing external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kind of modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NAND Flash Controller (NFC) includes the following features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Supports 8-bit Data Bus Width
- Supports 1024, 2048, 4096, 8192, 16384 bytes size per page
- Supports 1.8/3.3 V voltage supply Flash
- Up to 8 flash chips which are controlled by NFC_CEx#
- Supports Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NFC status information is reported by its' registers and interrupt is supported
- One Command FIFO
- External DMA is supported for transferring data
- Two 256x32-bit RAM for Pipeline Procession
- Support SDR, DDR and Toggle NAND
- Support self –debug for NFC debug

12.2. NAND Flash Controller Signal Description

Signal Name	Description	Type

NCE[7:0]	NAND FLASH Chip Select bit	O
NRB[1:0]	NAND FLASH Chip Ready/Busy bit	I
NWE	NAND FLASH Chip Write Enable	O
NRD	NAND FLASH Chip Read Enable	O
NALE	NAND FLASH Chip Address Latch Enable	O
NCLE	NAND FLASH Chip Command Latch Enable	O
NWP	NAND FLASH Chip Write Protect	O
ND[7:0]	NAND FLASH Data bit	I/O

Table 12-1. NAND Flash Controller Signal Description

13. SD3.0 Controller

13.1. SD 3.0 Overview

The SD3.0 controller can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

The SD3.0 controller includes the following features:

- Supports Secure Digital memory protocol commands (up to SD3.0)
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands (up to MMC4.3)
- Supports CE-ATA digital protocol commands
- Supports eMMC boot operation and alternative boot operation
- Supports UHS-1card voltage switching and DDR R/W operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.3) or CE-ATA device
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports SDIO read wait
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 16x32-bit (64 bytes total) FIFO for data transfer
- Support 3.3 V and 1.8V IO pad

13.2. SD3.0 Controller Signal Description

SDCx=SDC[3:0]

Signal Name	Description	Type
SDCx_CLK	SDx/SDIOx/MMCx Output Clock	O
SDCx_CMD	SDx/SDIOx/MMCx Cmmand Line	I/O
SDCx_D[3:0]	SDx/SDIOx/MMCx Data bit	I/O

Table 13-2. SD3.0 Controller Signal Description

14. Two Wire Interface

14.1. Overview

This 2-Wire Controller is designed to be used as an interface between CPU host and the serial 2-Wire bus. It can support all the standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This 2-Wire Controller can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

The 2-Wire Controller includes the following features:

- Software-programmable for Slave or Master
- Support Repeated START signal
- Support Multi-master systems
- Support 10-bit addressing with 2-Wire bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Support operation from a wide range of input clock frequencies

14.2. TWI Controller Signal Description

TWIx=TWI[2:0]

Signal Name	Description	Type
TWIx_SCK	TWI-BUS Clock for Channel x	I/O
TWIx_SDA	TWI-BUS Data for Channel x	I/O

Table 14-1. TWI Controller Signal Description

15. SPI Interface

15.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with fewer software interrupts. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode. It includes the following features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals for SPI0 and SPI1 has one chip select
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Support dedicated DMA

15.2. SPI Controller Signal Description

SPIx=SPI[2:0]

Signal Name	Description	Type
SPIx_CS0	SPIx Chip Select	I/O
SPIx_MOSI	SPIx Master data Out, Slave data In	I/O
SPIx_MISO	SPIx Master data In, Slave data Out	I/O
SPIx_CLK	SPIx Clock	I/O

Table 15-1. SPI Controller Signal Description

16. UART Interface

16.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Support IrDa 1.0 SIR
- Interrupt support for FIFOs, Status Change

16.2. UART Controller Signal Description

UARTx=[7:0]

Signal Name	Description	Type
UARTx_TX	UARTx Transmit Data	O
UARTx_RX	UARTx Receive Data	I

Table 16-1. UART Controller Signal Description

17. IR Interface

17.1. Overview

Fast Infrared Interface (FIR) signals are multiplexed with UART2 signals using a system configuration for a complete infrared interface that supports SIR, CIR, MIR, and FIR modes. The Serial Infrared (SIR) protocol, which supports data rate which supports data rates up to 1.875 Mbit/s is implemented in each UART module. The IR includes the following features:

- Compliant with IrDA 1.1 for MIR and FIR
- Full physical layer implementation
- Supports 0.576 Mbit/s and 1.152 Mbit/s Medium Infrared (MIR) physical layer protocol
- Support 4 Mbit/s FIR physical layer protocol defined by IrDA version 1.4
- Support CIR for remote control or wireless keyboard
- Hardware CRC16 for MIR and CRC32 for FIR
- Dual 16x8-bits FIFO for data transfer
- Programmable FIFO thresholds
- Interrupt and DMA Support

17.2. IR Controller Signal Description

IRx=IR[1:0]

Signal Name	Description	Type
IRx_TX	IR Transmit Data	O
IRx_RX	IR Receive Data	I

Table 17-1. IR Controller Signal Description

18. USB OTG Controller

18.1. Overview

The USB OTG is dual-role controller, which supports both Host and device functions. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode.

The USB2.0 OTG controller (SIE) includes the following features:

- Complies with USB 2.0 Specification
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode and support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Support up to 5 User-Configurable Endpoints for Bulk , Isochronous, Control and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)

18.2. USB OTG Controller Signal Description

Signal Name	Description	Type
DM0	USB0 OTG Data(-)	AIO
DP0	USB0 OTG Data(+)	AIO

Table 18-1. USB OTG Controller Signal Description

19. USB HOST Controller

19.1. Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

The USB host controller includes the following features:

- Including an internal DMA Controller for data transfer with memory.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480-Mbps) Device only, Full-Speed (FS, 12Mbps) and Low-Speed (LS, 1.5Mbps) Device.
- Support only 1 USB Root Port shared between EHCI and OHCI.

19.2. USB HOST Controller Signal Description

USBx Host2.0=USB[1:0] Host2.0

Signal Name	Description	Type
DM1	USB1 HOST Data(-)	AIO
DP1	USB1 HOST Data(+)	AIO
DM2	USB2 HOST Data(-)	AIO
DP2	USB2 HOST Data(+)	AIO

Table 19-1. USB Host Controller Signal Description

20. Digital Audio Interface

20.1. Overview

The Digital Audio Interface can be configured as I2S interface or PCM interface by software. When configured as I2S interface, it can support the industry standard format for I2S, left-justified, or right-justified. When configured as PCM, it can be used to transmit digital audio over digital communication channels. It supports linear 13, 16-bits linear, 8-bit u-law or A-law compressed sample formats at 8K samples/sec, and can receive and transmit on any selection of the first four slots following PCM_SYNC.

It includes the following features:

- I2S or PCM configured by software
- Full-duplex synchronous serial interface
- Configurable Master / Slave Mode operation
- Support Audio data resolutions of 16, 20, 24
- I2S Audio data sample rate from 8Khz to 192Khz
- I2S Data format for standard I2S, Left Justified and Right Justified
- I2S support 8 channel output and 2 channel input
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law compressed sample
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Programmable FIFO thresholds
- Support Interrupt and DMA
- Two 32-bits Counters for AV sync application

20.2. Digital Audio Signal Description

Signal Name	Description	Type
I2S_MCLK	I2S Main Clock(system clock)	O
I2S_BCLK	I2S serial Bit Clock	I/O
I2S_LRCK	I2S Left or Right channel select clock(frame clock)	I/O
I2S_DO[3:0]	I2S serial Data Output bit	O
I2S_DI	I2S serial Data Input	I

Table 20-1. Digital Audio Controller Signal Description

21. AC97 Interface

21.1. Overview

The AC97 interface supports AC97 revision 2.3. AC97 Controller uses audio Controller link (AC-link) to communicate with AC97 Codec. In transmission mode, Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec converts the audio sample to an analog audio waveform. In receiving mode, Controller receives the stereo PCM data and the mono Microphone data from Codec then stores in memories.

AC97 Interface includes below features:

- Compliant with AC97 2.3 component Specification
- Full-duplex synchronous serial interface
- Support 2 channels, TX (stereo),RX (PCM stereo, MIC mono optional)
- Variable Sampling Rate AC97 Codec Interface support, up to 48KHz
- Support 2 channel and 6 channel audio data output
- Support DRA mode
- Support Only one primary Codec
- Channels support mono or stereo samples of 16(standard), 18(optional) and 20(optional) bit wide.
- One 96×20bits FIFO and one 32×20-bits FIFO for data transfer
- Programmable FIFO thresholds
- Support Interrupt and DMA

21.2. AC97 Signal Description

Signal Name	Description	Type
AC97_MCLK	AC97 Codec Input Mclk	O
AC97_BCLK	Digital Audio Serial Clock Provided by AC97 Codec	I
AC97_SYNC	Digital Audio Sample rate/sync	O
AC97_DO	Digital Audio Serial Data Input	I
AC97_DI	Digital Audio Serial Data Onput	O

Table 21-1. AC97 Controller Signal Description

22. Audio Codec

22.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplify.

The audio codec is featured as following:

- On-chip 24-bits DAC for play-back
- On-chip 24-bits ADC for recorder
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- Support 192K and 96K sample
- Support FM/ Line-in/ Microphone recorder
- Stereo headphone amplifier that can be operated in capless headphone mode
- Support to automatic change from Virtual Ground to True Ground to protect headphone amplifier

22.2. Audio Codec Signal Description

Signal Name	Description	Type
HPL	Headphone Left channel output	AO
HPR	Headphone Right channel output	AO
HPCOM	Headphone amplifier output	A
HPCOM_FB	Headphone amplifier Feedback	A
FMINL	Audio ADC(24bit) Input for Left channel of FM radio	AI
FMINR	Audio ADC(24bit) Input for Right channel of FM radio	AI
LINEINL	Audio ADC(24bit) Input for Left channel of Line In	AI
LINEINR	Audio ADC(24bit) Input for Right channel of Line In	AI
MICINL	Audio ADC(24bit) Input for Left channel of Microphone	AI
MICINR	Audio ADC(24bit) Input for Right channel of Microphone	AI

Table 22-1. Audio Codec Signal Description

23. LRADC

23.1. Overview

LRADC is 6-bits resolution for key application. The LRADC can work up to maximum conversion rate of 250Hz.

The LRADC is featured as following：

- Support APB 32-bits bus width
- Support Interrupt
- Support Hold Key and General Key
- Support Single Key and continue key mode
- 6-bits Resolution
- Voltage input range between 0 to 2V
- Sample Rate up to 250Hz

23.2. LRADC Signal Description

Signal Name	Description	Type
LRADC[1:0]	Low Resolution ADC0 input(6bit)	AI

Table 23-2. LRADC Signal Description

24. Keypad Interface

24.1. Overview

The Key Pad Interface block in A10 facilitates communication with external keypad devices. The ports can provide up to 8 rows and 8 columns. The events of key press or key release are delivered to the CPU by an interrupt. To prevent the switching noises, keypad interface comprise of internal debouncing filter.

The Keypad Interface includes the following features:

- Interrupt for key press or key release
- Internal debouncing filter to prevent the switching noises

24.2. Keypad Signal Description

Signal Name	Description	Type
KP_IN[7:0]	Keypad Interface Row data	I
KP_OUT[7:0]	Keypad Interface Column0 data	O

Table 24-1. Keypad Signal Description

25. Touch Panel

25.1. Overview

The TP controller can be configured either as a 4-wire resistive touch screen controller or a 12-bit resolution A/D converter. As a 4-wire resistive touch screen controller, it supports dual touch detection. As an A/D converter, it can locate of single touch through two times of A/D conversion.

The TP controller is featured as following:

- 12 bit SAR type A/D converter
- 4-wire I/F
- Dual Touch Detection
- Touch-pressure measurement (Support program set threshold)
- Sampling frequency: 2MHz (max)
- Support both Single-Ended and Ratiometric Conversion of Touch Screen Inputs
- TACQ up to 262ms
- Support Median and averaging filter which can reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

25.2. Touch Panel Signal Description

Signal Name	Description	Type
X[2:1]	Touch Pane ADC input(11bit)	AI
Y[2:1]	Touch Pane ADC input(11bit)	AI

Table 25-1. Touch Panel Signal Description

26. Port Controller

26.1. Port Description

The chip has 8 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 18 input/output port
- Port B(PB): 24 input/output port
- Port C(PC): 25 input/output port
- Port D(PD): 28 input/output port
- Port E(PE) : 12 input/output port
- Port F(PF) : 6 input/output port
- Port G(PG) : 12 input/output port
- Port H(PH) : 28 input/output port
- Port I(PI) : 22 input/output port
- Port S(PS) : 84 input/output port for DRAM controller

For various system configurations, these ports can be easily configured by software. All these ports (except PS) can be configured as GPIO if multiplexed functions not used. 32 external PIO interrupt sources are supported and interrupt mode can be configured by software.

27. Camera sensor interface

27.1. Feature

- 8 bits input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Received data double buffer support
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or tile-based Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software

27.2. Camera sensor Signal Description

Signal Name	Description	Type
CSI0		
CSI0_PCK	Camera Sensor Pixel Clock	I
CSI0_MCK	Camera Sensor Clock Output	O
CSI0_HSYNC	Camera Sensor Horizontal Synchronization	I
CSI0_VSYNC	Camera Sensor Verizontal Synchronization	I
CSI0_D[7:0]	Camera Sensor Data bit 0…7	I
CSI1		
CSI1_D[23:0]	Camera Sensor Data bit 0…23	I
CSI1_PCLK	Digital Image Pixel Clock input	
CSI1_FIELD		
CSI1_HSYNC	CMOS Sensor Horizontal Synchronization	I
CSI1_VSYNC	CMOS Sensor Verizontal Synchronization	I

Table 27-1. Camera sensor Signal Description

28. Universal LCD/TV Timing Controller

28.1. Overview

TCON in A10 is of high flexibility in timing configuration as well as LCD module compatibility.

- Support LVDS input LCD panels (Max 1920*1080 resolution, 24-bit color)
- Support HV-DE-Sync(digital parallel RGB) input LCD panels(Max 1920*1080 resolution, 24-bit color)
- Support HV-DE-Sync(digital serial RGB, both delta and stripe panel) input LCD panels(Max 1280*1024 resolution, up to true color)
- Support 18/16/9/8bit 8080 CPU I/F panels(Max 1920*1080 resolution)
- CCIR656 output interface for LCD panel or TV encoder
- Up to full HDTV timing for TV encoder

28.2. LCD Signal Description

LCDx=LCD[1:0]; LVDSx=LVDS[1:0]

Signal Name	Description	Type
LCDx_CLK	LCD RGB Pixel Clock	O
LCDx_DE	LCD RGB Data Enable	O
LCDx_HSYNC	LCD RGB Horizontal Synchronization	O
LCDx_VSYNC	LCD RGB Verizontal Synchronization	O
LCDx_D[23:0]	LCD Pixel Data bit 0…23	O
LVDSx_VP[3:0]	LVDS Output Data+ for Channelx	O
LVDSx_VN[3:0]	LVDS Output Data- for Channelx	O

Table 28-1. LCD Signal Description

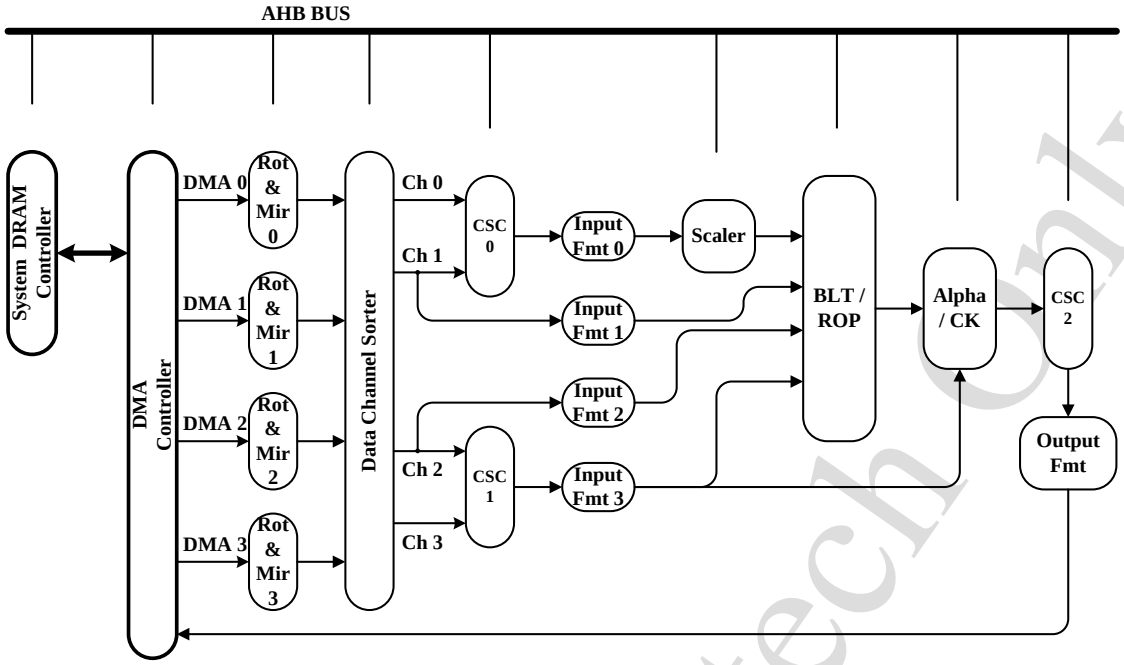
29. Mixer Processor

29.1. Overview

Mixer processor is a 2D graphics engine of high performance, and 2D image can be widely customized due to its high flexibility in configuration.

- Color format support
  ARGB 8888/4444/1555
  RGB565
  MONO 1/2/4/8 bpp
  Palette 1/2/4/8 bpp (input only)
  22/420
- Any format convert function
- Buffer block size
  Up to 8192*8192 pixels
- Support Memory scan order option
- Support Clipping
- ROP2
  Line / Rectangle / Point
  Block fill
- ROP3
  BitBLT
  PatBLT
  StretchBLT
- ROP4
  MaskBLT
- Rotation 90/180/270 degree
- Support mirror
- Alpha blending
  Support Plane & Pixel alpha
  Support Output alpha configurable
- Support Color key
- Scaling
  4*4 taps
  32 phase
- Support color space convert

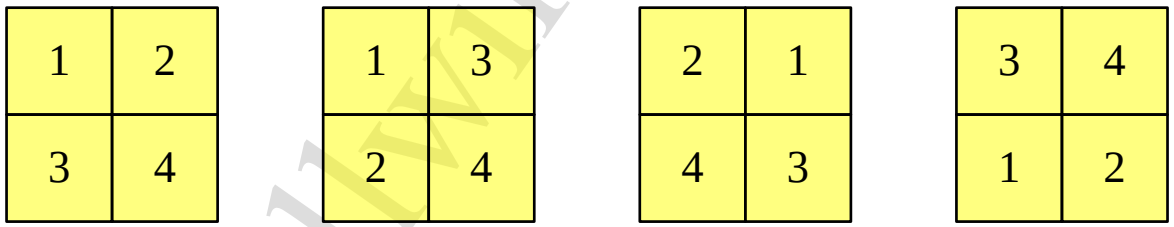
29.2. Block diagram



Mixer Processor General Diagram

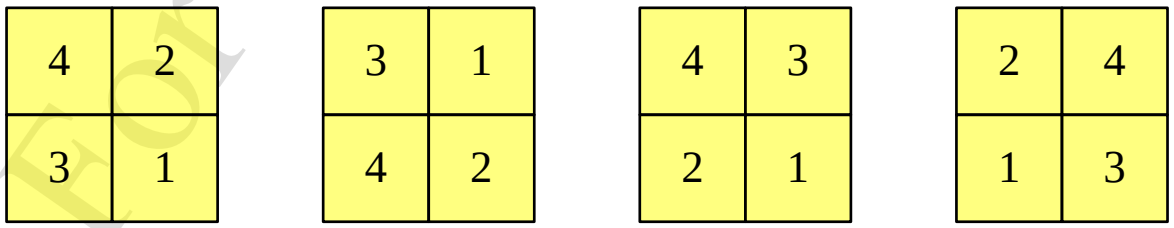
29.2.1. Layer rotation and mirroring control

Each layer data can be realized rotation and mirror operation function, total 8 operation according 8 control code, reference the following diagram.



Control code:

Normal A X Y



Control code:

AXY AY XY AX

30. TV Encoder

30.1. Feature

- Multi-standard support for NTSC-M, NTSCJAPAN,PAL (B, D, G, H, I, M, N,Combination N)@27M clock
- Support 480P, 576P@54M clock
- Support 720P,1080i@74.25M clock
- Support 1080P@148.5M clock
- Video input data port supports: CCIR-656 4:2:2 8-bit parallel input format
- Video output data port supports: 4 X12-bit DAC data output, Composite(CVBS) and Component S-video(Y/C) or Component YUV or RGB
- Analog signal output copyright protection
- Programmable 4 X DAC data path
- Plug status auto detecting

30.2. TV-OUT Signal Description

Signal Name	Description	Type
TV_OUT[3:0]	TV Analog Output(12bit DAC0..3)	AO
TV_VCC	TVDAC Analog Power	
TV_GND	TVDAC Analog Ground	

Table 30-1. TV-OUT Signal Description

31. Declaration

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