ATC2609 Datasheet

Version: 1.1

2015-09-16

Declaration

Disclaimer

Information given in this document is provided just as a reference or example for the purpose of using Actions' products, and cannot treated as a part of any quotation or contract for sale.

Actions products may contain design defects or errors known as anomalies or errata which may cause the products' functions to deviate from published specifications. Designers must not rely on the instructions of Actions' products marked "reserved" or "undefined". Actions reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

ACTIONS DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL EXPRESS OR IMPLIED WARRANTIES OF MERCHANTABILITY, ACCURACY, SECURITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY AND THE LIKE TO THE INFORMATON OF THIS DOCUMENT AND ACTIONS PRODUCTS.

IN NO EVENT SHALL ACTIONS BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES WHATSOEVER, INCLUDING, WITHOUT LIMITATION FOR LOST OF DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND ARISING FROM USING THE INFORMATON OF THIS DOCUMENT AND ACTIONS PRODUCTS. REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF ACTIONS OR OTHERS; STRICT LIABILITY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER ACTIONS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES OR NOT.

Actions' products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of Actions and further testing and/or modification will be fully at the risk of the customer.

Ways of obtaining information

Copies of this document and/or other Actions product literature, as well as the Terms and Conditions of Sale Agreement, may be obtained by visiting Actions' website at: http://www.actions-semi.com or from an authorized Actions representative.

Trademarks

The word "Actions" and the logo are the trademarks of Actions Semiconductor Co., Ltd, and Actions (Zhuhai) Technology Co., Limited is authorized to use them. Word "炬芯" is the trademark of Actions (Zhuhai) Technology Co., Limited. Names and brands of other companies and their products that may from time to time descriptively appear in this document are the trademarks of their respective holders, no affiliation, authorization, or endorsement by such persons are claimed or implied except as may be expressly stated therein.

Rights Reserved

The provision of this document shall not be deemed to grant buyers any right in and to patent, copyright, trademark, trade secret, know how, and any other intellectual property of Actions or others.

Miscellaneous

Information contained or described herein relates only to the Actions products and as of the release date of this publication, abrogates and supersedes all previously published data and specifications relating to such products provided by Actions or by any other person purporting to distribute such information.

Actions reserves the rights to make changes to information described herein at any time without notice. Please contact your Actions sales representatives to obtain the latest information before placing your product order.

Additional Support

Additional product and company information can be obtained by visiting the Actions website at: http://www.actions-semi.com

Contents

Declaration ····· **ii**

Contents ····· **iv**

Revision History ····· **x**

1 Introduction ····· **1**

1.1 Overview ····· 1

1.2 Features ····· 1

1.3 Typical Applications ····· 4

1.4 Ordering Information ····· 4

2 Absolute Maximum Rating ····· **5**

3 Recommended Operating Conditions ····· **5**

4 Electrical Characteristics ····· **6**

4.1 Overshoot ····· 6

4.2 DC Characteristics ····· 6

5 Audio Codec Subsystem ····· **7**

5.1 Audio Diagram ····· 7

5.1.1 Register List ····· 7

5.1.2 Register Description ····· 8

5.1.2.1 AUDIOINOUT_CTL ····· 8

5.1.2.2 DAC_DIGITALCTL ····· 9

5.1.2.3 DAC_VOLUMECTL0 ····· 10

5.1.2.4 DAC_ANALOG0 ····· 10

5.1.2.5 DAC_ANALOG1 ····· 11

5.1.2.6 DAC_ANALOG2 ····· 12

5.1.2.7 DAC_ANALOG3 ····· 13

5.1.2.8 ADC_DIGITALCTL ····· 13

5.1.2.9 ADC_HPFCTL ····· 15

5.1.2.10 ADC_CTL ····· 16

5.1.2.11 AGC_CTL0 ····· 17

5.1.2.12 AGC_CTL1 ····· 18

5.1.2.13 AGC_CTL2 ····· 19

5.1.2.14 ADC_ANALOG0 ····· 21

5.1.2.15 ADC_ANALOG1 ····· 21

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

5.2 Audio Characteristics 22
5.2.1 DAC+PA 23
5.2.2 PA 24
5.2.3 ADC 26
5.3 PCM 26
5.3.1 PCM Interface 26
5.3.2 Register List 27
5.3.3 Register Description 27
5.3.3.1 PCM0_CTL, PCM1_CTL, PCM2_CTL 27
5.3.3.2 PCMIF_CTL 28

6 TWI Interface 29

6.1 Features 29
6.2 Register List 29
6.3 Register Description 30
6.3.1 SADDR 30

7 Power Management Unit 31

7.1 Features 31
7.2 Module Description 31
7.2.1 DC-DC Module 31
7.2.2 LDO Module 33
7.2.3 Charger Module 33
7.2.4 APDS Module 34
7.2.5 Power Modes 35
7.2.6 POR and Power ON/OFF Sequence Module 36
7.2.7 ONOFF & Reset Module 37
7.2.8 Coulombmeter 37
7.3 Register List 37
7.4 Register Description 39
7.4.1 PMU_SYS_CTL0 39
7.4.2 PMU_SYS_CTL1 41
7.4.3 PMU_SYS_CTL2 42
7.4.4 PMU_SYS_CTL3 44
7.4.5 PMU_SYS_CTL4 44
7.4.6 PMU_SYS_CTL5 45
7.4.7 PMU_SYS_CTL6 46
7.4.8 PMU_BAT_CTL0 46
7.4.9 PMU_BAT_CTL1 47
7.4.10 PMU_VBUS_CTL0 48
7.4.11 PMU_VBUS_CTL1 49
7.4.12 PMU_WALL_CTL0 49

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.13 PMU_WALL_CTL1 50
7.4.14 PMU_SYS_PENDING 51
7.4.15 PMU_APDS_CTL0 52
7.4.16 PMU_APDS_CTL1 54
7.4.17 PMU_APDS_CTL2 56
7.4.18 PMU_CHARGER_CTL 56
7.4.19 PMU_SWCHG_CTL0 57
7.4.20 PMU_SWCHG_CTL1 58
7.4.21 PMU_SWCHG_CTL2 60
7.4.22 PMU_SWCHG_CTL3 61
7.4.23 PMU_SWCHG_CTL4 62
7.4.24 PMU_DC_OSC 63
7.4.25 PMU_DC0_CTL0 63
7.4.26 PMU_DC1_CTL0 64
7.4.27 PMU_DC2_CTL0 64
7.4.28 PMU_DC3_CTL0 65
7.4.29 PMU_DC4_CTL0 65
7.4.30 PMU_DC_ZR 65
7.4.31 PMU_LDO0_CTL0 66
7.4.32 PMU_LDO1_CTL0 66
7.4.33 PMU_LDO2_CTL0 67
7.4.34 PMU_LDO3_CTL0 68
7.4.35 PMU_LDO4_CTL0 69
7.4.36 PMU_LDO6_CTL0 70
7.4.37 PMU_LDO7_CTL0 71
7.4.38 PMU_LDO8_CTL0 72
7.4.39 PMU_LDO9_CTL 72
7.4.40 PMU_OV_STATUS 73
7.4.41 PMU_UV_INT_EN 74
7.4.42 PMU_UV_STATUS 75
7.4.43 PMU_OC_INT_EN 77
7.4.44 PMU_OC_STATUS 78
7.4.45 PMU_OT_CTL 79
7.4.46 PMU_CM_CTL0 80
7.4.47 PMU_PWR_STATUS 80
7.4.48 PMU_S2_PWR 82
7.4.49 CLMT_CTL0 83
7.4.50 CLMT_DATA0 84
7.4.51 CLMT_DATA1 84
7.4.52 CLMT_DATA2 85
7.4.53 CLMT_DATA3 85
7.4.54 PMU_ADC12B_I 85
7.4.55 PMU_ADC12B_V 85
7.4.56 CLMT_OCV_TABLE 85

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.57 CLMT_R_TABLE ····· 86

8 Auxiliary ADC ····· 88

8.1 Module Description ····· 88

8.2 Register List ····· 88

8.3 Register Description ····· 89

8.3.1 PMU_AUXADC_CTL0 ····· 89

8.3.2 PMU_AUXADC_CTL1 ····· 90

8.3.3 PMU_BATVADC ····· 91

8.3.4 PMU_BATIADC ····· 91

8.3.5 PMU_WALLVADC ····· 91

8.3.6 PMU_WALLIADC ····· 91

8.3.7 PMU_VBUSVADC ····· 92

8.3.8 PMU_VBUSIADC ····· 92

8.3.9 PMU_SYSPWRADC ····· 92

8.3.10 PMU_REMCONADC ····· 92

8.3.11 PMU_SVCCADC ····· 92

8.3.12 PMU_CHGIADC ····· 93

8.3.13 PMU_IREFADC ····· 93

8.3.14 PMU_ICTEMPADC ····· 93

8.3.15 PMU_AUXADC0 ····· 93

8.3.16 PMU_AUXADC1 ····· 93

8.3.17 PMU_ICTEMPADC_ADJ ····· 94

9 Clock Management Unit ····· 95

9.1 Universal Clock ····· 95

9.1.1 Register List ····· 95

9.1.2 Register Description ····· 95

9.1.2.1 CMU_DEVRST ····· 95

9.2 Real Time Clock ····· 95

9.2.1 Module Description ····· 96

9.2.2 Register List ····· 96

9.2.3 Register Description ····· 97

9.2.3.1 RTC_CTL ····· 97

9.2.3.2 RTC_MSALM ····· 98

9.2.3.3 RTC_HALM ····· 98

9.2.3.4 RTC_YMDALM ····· 98

9.2.3.5 RTC_MS ····· 99

9.2.3.6 RTC_H ····· 99

9.2.3.7 RTC_DC ····· 99

9.2.3.8 RTC_YMD ····· 99

10 Infrared Remote Controller ····· 100

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

10.1 Features ····· 100
10.2 Modules Description ····· 100
10.2.1 9012 Protocol ····· 100
10.2.2 NEC Protocol (8-bit) ····· 101
10.2.3 RC5 Protocol ····· 102
10.2.4 RC6 Protocol ····· 103
10.3 Register List ····· 104
10.4 Register Description ····· 105
10.4.1 IRC_CTL ····· 105
10.4.2 IRC_STAT ····· 105
10.4.3 IRC_CC ····· 106
10.4.4 IRC_KDC ····· 106
10.4.5 IRC_WK ····· 107
10.4.6 IRC_RCC ····· 107

11 Interrupt Controller ····· 108
11.1 Features ····· 108
11.2 Block Diagram ····· 108
11.3 Register List ····· 109
11.4 Register Description ····· 109
11.4.1 INTS_PD ····· 109
11.4.2 INTS_MSK ····· 109

12 General Purpose I/O ····· 111
12.1 Features ····· 111
12.2 Registers List ····· 111
12.3 Register Description ····· 111
12.3.1 MFP_CTL ····· 111
12.3.2 PAD_VSEL ····· 112
12.3.3 GPIO_OUTEN ····· 113
12.3.4 GPIO_INEN ····· 113
12.3.5 GPIO_DAT ····· 113
12.3.6 PAD_DRV ····· 114
12.3.7 PAD_EN ····· 115

13 Pin Description ····· 116
13.1 ATC2609 Pin Assignment ····· 116
13.2 ATC2609 Pin Definition ····· 117

14 Package and Ordering Information ····· 119

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

14.1 Package Drawing 119

Appendix 120

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Revision History

Date	Revision	Description
2015-03-05	1.0	First Release
2015-09-15	1.1	Update pin 57/58 name

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

1 Introduction

1.1 Overview

ATC2609 is an integrated Audio Codec and Power Management IC, which provides a cost effective, single-chip solution for portable smart systems. It acts as a slave device on TWI interface controlled by Master. Integrated Audio CODEC provides all necessary functions for high-quality recording and playback. Programmable on-chip amplifiers allow direct connection to headphones. Digital and analog microphone interface are both supported.
Internal Power Management circuit controls the start-up, shutdown, as well as sleep and wake-up sequence of each power signals. It also detects and handles abnormal conditions such like overvoltage and overcurrent.

ATC2609 includes 6 programmable DC-DC converters, one of the DC-DCs is used for battery charging switch, 10 low-dropout (LDO) regulators providing suitable supply voltages for each part of the system, including on-chip audio CODEC as well as off-chip components such as a digital core, memory chips, WiFi and sensor modules. Each of these is voltage programmable. ATC2609 can be powered by a lithium battery, a wall adaptor or Host USB port.

On-chip battery charger supports both trickle charging and fast (constant current and constant voltage) charging for single-cell Lithium battery. Built-in Coulombmeter supports accurate battery capacity monitor. Charging current, termination voltage, and charger time-out are programmable to fit different types of batteries.

An external 32.768 kHz crystal oscillator should be supplied to ATC2609 system to get an accurate clock for Real Time Clock (RTC) and alarm function capable of waking up the system. IR and multi-channel ADC capable of waking up the system are also integrated.

1.2 Features

Audio CODEC

- **ADC**
  - Built-in stereo 21-bit input sigma-delta ADCs
  - SNR>88dB, SNR(A-WEIGHTING)>91dB, THD<-82dB
  - Support sample rate of 96k/48k/32k/24k/16k/12k/8k/44.1k/22.5k/11.025k
  - A digital high-pass filter can be switched in line with the ADCs under serial control to remove residual DC offsets and Wind Noise
- **DAC**
  - Built-in 2.0 channel 24-bit input sigma-delta DACs
  - SNR>93dB, SNR (A-WEIGHTING)>96dB, THD<-80dB
  - Each channel has independent digital volume and mute control
  - Support sample rate of 192k/96k/48k/32k/24k/16k/12k/8k/176.4k/88.2k/44.1k/22.05k/

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

11.025k

- **Headphone & PA**
  - Support stereo headphone output interface
  - Built-in stereo 20mW PA (Power Amplifier) for headphone with 41 level volume control
  - Zero cross function to eliminate the pop of changing the volume sharply
  - Support traditional mode and direct drive mode (for headphone)
  - An anti-pop circuit for suppressing noise of PA when enable or disable PA
- **Microphone**
  - Support mono full difference input or stereo single-ended input analog microphone
  - With a Configurable Automatic Gain Control (AGC), Zero Crossing and Noise Gating for analog microphone using
  - A stereo digital microphones (DMIC) interface is provided, with a data input to PMIC and a clock output for external stereo digital microphones
- **I2S**
  - Support 2.0 channel I2S transmitter and Receiver, slave mode only
  - Support sample rate of 192k/96k/48k/32k/24k/16k/12k/8k/176.4k/88.2k/44.1k/22.05k/ 11.025k
- **PCM Features**
  - Include 3 PCM Modules, PCM0(for Master), PCM1(for BT), PCM2(for Baseband)
  - Include PCM TX and PCM RX, slave mode only
  - Linear PCM (13~16bit), u-Law (8bit), A-Law (8bit)
  - PCM clock up to 2.048MHz
  - Long Frame Sync and Short Frame Sync

Power Supply Generation

- Over-voltage, over-current, over-temperature protection for DC-DCs and LDOs
- **6 DC-DCs:**
  - 1 DC-DC Buck Switch for Charger (Up to 3000mA)
  - 1 DC-DC Buck Converter (0.6~2.2V, Up to 3000mA)
  - 3 DC-DC Buck Converter (0.6~2.2V, Up to 2000mA)
  - 1 DC-DC Buck Converter (0.6~3.3V, Up to 1200mA)
- **10 LDOs:**
  - 3 LDO voltage regulator (2.3~3.3V, Up to 500mA), high PSRR
  - 5 LDO voltage regulator (0.7~3.3V, Up to 200mA), high PSRR
  - 1 LDO voltage regulator (2.6~3.3V, Up to 25mA), for standby use
  - 1 LDO voltage regulator (1.8V, Up to 20mA), for RTC use

Battery Charger 3A

- Single-cell Li-battery charger
- Switched mode charger with integrated power FET for up to 3A current
- 12-bit Coulombmeter
- Thermal protection for charge control

IR

- Support RC5\9012\NEC(8-bit)\RC6 protocol
- Compatible with 36KHz, 38KHz, 40KHz carrier

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

- Support IRC wake up

Power Saving Mode

- Several power saving modes including standby mode, sleep mode and deep-sleep mode
- “Always on” RTC with wake-up alarm
- In deep-sleep with RTC always on, the battery current can be less than 30μA

System Control

- Two-Wire Serial Interface
- Configurable power sequencing
- Power-on reset signal, sleep mode signal and fault conditions interrupt signal
- Adaptive power distribute system, autonomous power source selection (battery, wall adaptor or host USB port)

Additional Features

- A multi-channel 16-bit ADC, can be used as voltage, current measurement or Remote control
- Support interrupt to Master
- A few configurable GPIO pins
- ESD Level of HBM pass over 2000V for all IOs

Package

- QFN68, 8mm * 8mm, 0.4mm pin pitch

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

1.3 Typical Applications

ATC2609 mainly consists of Power Management Unit and Audio CODEC block. Figure 1-1 below shows the typical application diagram of ATC2609.

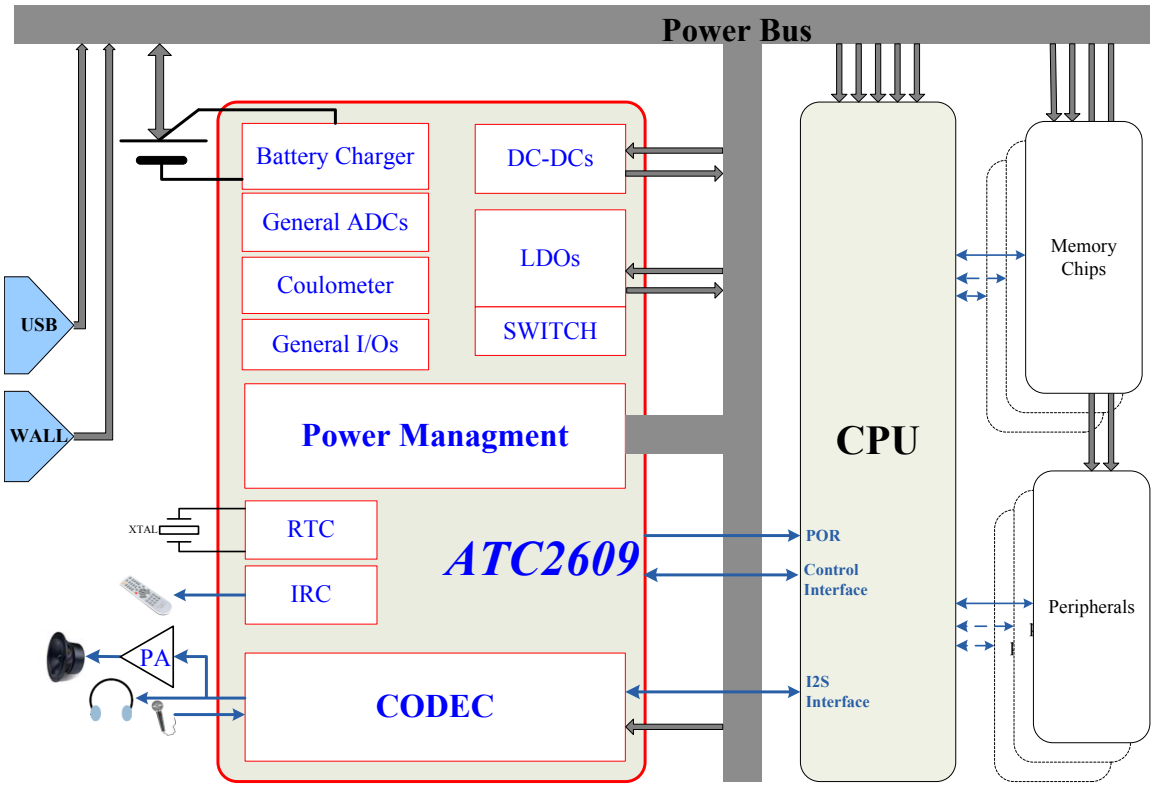


Figure 1-1 Typical Application diagram

1.4 Ordering Information

Table 1-1 Ordering Information

Part Numbers	Package	Size
ATC2609	QFN68	8mm * 8mm

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

2 Absolute Maximum Rating

These absolute maximum ratings are stress ratings, operating at or beyond these ratings for more than 1ms may result in permanent damage. Unless otherwise noted, all voltage values are relative to VSS.

Table 2-1 Max ratings of ATC2609

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	℃
Storage Temperature	Tstg	-55	+150	℃
Supply Voltage	DCxIN/WALL/VBUS/BAT/SYSPWR	-0.3	6.5	V
Input Voltage	Digital IO	-0.3	3.6	V
	Analog IO (FMIN/MICIN)	-0.3	3.6	V
ESD Stress Voltage	VESD (Human Body Model)	2000	-	V

3 Recommended Operating Conditions

Table 3-1 Recommended Operating Voltage

Parameter	Symbol	Min	Typ	Max	Unit
Wall adapter input source	WALL	4.5	5.0	5.5	V
USB VBUS input source	VBUS	4.75	5.0	5.25	V
Battery input source	BAT	3.4	3.8	4.2	V
Supply voltage	DCxVIN/LDOxIN/SWxIN	3.3		5.5	V
Core supply	VDD		1.8		V
IO supply	VCC		3.1		V
Ground	GND/AGND/DCxGND/CDPGNDx		0		V

Note: in DCxVIN/LDOxIN/SWxIN and DCxGND/CDPGNDx, x is number, for example, DC1VIN represents the Input Voltage of DC-DC1.

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

4 Electrical Characteristics

4.1 Overshoot

The maximum DC voltage on power supply pins is 6.5V. However, during voltage domains switching period, the device can tolerate overshoot for up to 10μs, as shown in Figure 4-1 below.

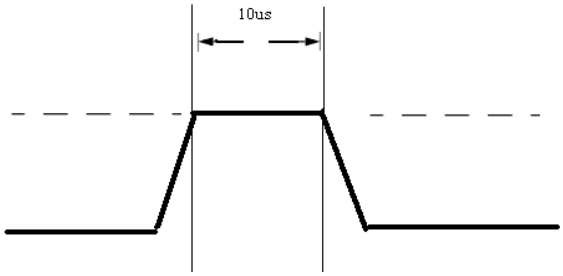


Figure 4-1 Tolerance for overshoot for up to 10μs

Table 4-1 Extreme Values for Input Pins

Parameter	Symbol	Start	Max	Unit
Supply voltage	DCxIN/WALL/VBUS/BAT	-0.3	12	V

ATC2609 can tolerate 1,000 times of such pulse. But exposed to overshoot circumstances for too many times may affect device's lifetime.

4.2 DC Characteristics

Table 4-2 DC Characteristics

VCC = 3.1V for IO Pins, Tamb = 0~70°C

Parameter	Symbol	Min	Typ	Max	Unit
Low-level input voltage	V_{IL}	-	-	0.8	V
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level output voltage	V_{OL}	-	-	0.4	V
High-level output voltage	V_{OH}	2.4	-	-	V

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

5 Audio Codec Subsystem

5.1 Audio Diagram

Audio Codec subsystem integrates I2S interface, DAC, ADC, AGC, PCM interface, MIC amplifier, FM amplifier, headphone PA. I2S interface in slave mode supports 2.0 channel transmitter and receiver. I2S supports sample rate of 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/22.05k/11.025k. The 2.0 channel Sigma-Delta DAC supports the same sample rate as I2S. The stereo 20mW PA (Power Amplifier) is integrated for headphone with 41-level volume control, Non-direct and Direct Drive mode both with anti-pop circuit are supported for headphone. The subsystem supports stereo analog microphones (AMIC) and stereo Digital Microphones (DMIC). The AMIC interface provides programmable bias output and the DMIC interface provides a clock signal for external stereo DMIC and a data signal for PMU. The analog microphone has the configurable Automatic Gain Control (AGC), Zero Crossing and Noise gating. For PCM, right channel data of ADC will be selected for PCM.

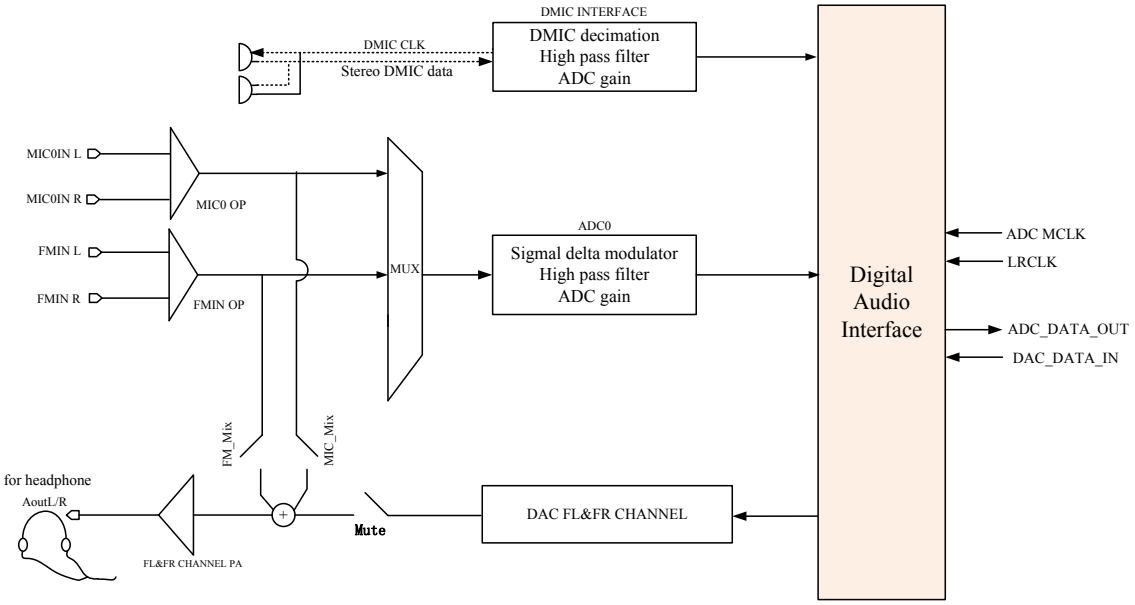


Figure 5-1 Audio Diagram & Signal Path

5.1.1 Register List

Table 5-1 AUDIO OUT IN Controller Registers Address

Name	Physical Base Address
AUDIO_OUT	0xA0
AUDIO_IN	0xA0

Table 5-2 Audio Registers

Offset	Register Name	Description

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

0x00	AUDIOINOUT_CTL	AUDIO IN/OUT Control for I2S Register
0x02	DAC_DIGITALCTL	DAC Control EN&MUTE Register
0x03	DAC_VOLUMECTL0	DAC FL&FR VOLUME Control Register
0x04	DAC_ANALOG0	DAC Analog 0 Register
0x05	DAC_ANALOG1	DAC Analog 1 Register
0x06	DAC_ANALOG2	DAC Analog 2 Register
0x07	DAC_ANALOG3	DAC Analog 3 Register
0x08	ADC_DIGITALCTL	ADC Digital Control Register
0x09	ADC_HPFCTL	ADC High Pass Filter Control Register
0x0A	ADC_CTL	ADC control register
0x0B	AGC_CTL0	AGC Control 0 Register
0x0C	AGC_CTL1	AGC Control 1 Register
0x0D	AGC_CTL2	AGC Control 2 Register
0x0E	ADC_ANALOG0	ADC Analog 0 Register
0x0F	ADC_ANALOG1	ADC Analog 1 Register

5.1.2 Register Description

5.1.2.1 AUDIOINOUT_CTL

AUDIO IN/OUT Control for I2S Register
Offset = 0x00

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	MDD	MCLK Divided to DAC 0:DIV=1 1:DIV=2	RW	0
10	-	Reserved	-	-
9	OCIEN	Direct Drive Output Over Current status IRQ 1: enable 0: disable If DAC_ANALOG2[5] is enabled and DAC_ANALOG3[14] is high, when this bit is enabled, an interrupt will be sent to the interrupt controller.	RW	0
8	OEN	I2S Output Enable. 0: Disable 1: Enable	RW	0
7	-	Reserved	-	-
6:5	IMS	I2S RX&TX Mode Select 00:3 wires mode 01:4 wires mode 10:6 wires mode 11:Reserved	RW	00

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

4:2	-	Reserved	-	-
1	INEN	I2S Input Enable. 0: Disable 1: Enable	RW	0
0	IWLS	I2S input word length select 0:32-bit 1:Reserved	RW	0

5.1.2.2 DAC_DIGITALCTL

DAC Control EN_MUTE Register

Offset = 0x02

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	RW	0
11:10	DACINSEL	DAC input source select 00:I2S (music) 01:PCM0_IN(key tone) 10:PCM2_IN(voice) 11:PCM0_IN add PCM2_IN(voice add key tone)	RW	00
9	-	Reserved	-	-
8	DISRS	DAC INPUT SAMPLE RATE SEL 0:MCLK/256 1:MCLK/128	RW	0
7:6	DBWFL_FR	DACFL&FR BANDWIDTH 00:WIDE 01:MIDDLE 10:NARROW 11:Reserved	RW	00
5:4	DOSRSFL_FR	DAC FL&FR OUTPUT SAMPLE RATE SEL 00:MCLK/16 01:MCLK/8 10:MCLK/4 11:MCLK/2	RW	00
3	DMFR	DACFR DIGITAL MUTE 1:MUTE 0:UNMUTE	RW	0
2	DMFL	DACFL DIGITAL MUTE 1:MUTE 0:UNMUTE	RW	0
1	DEFR	DACFR DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
0	DEFL	DACFL DIGITAL ENABLE 1:ENABLE	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:DISABLE		

5.1.2.3 DAC_VOLUMECTL0

DAC FL_FR VOLUME CONTROL ((3/8) dB/level)
Offset = 0x03

Bit(s)	Name	Description	Access	Reset
15:8	DACFR_VOLUME	VOLUME CONTROL (3/8) dB/level 0xFF :+24 dB …… 0xBF : 0 dB 0xBE : -3/8 dB …… 0x00 : -72 dB	RW	BE
7:0	DACFL_VOLUME	VOLUME CONTROL (3/8) dB/level 0xFF :+24 dB …… 0xBF : 0 dB 0xBE : -3/8 dB …… 0x00 : -72 dB	RW	BE

5.1.2.4 DAC_ANALOG0

DAC Analog Register
Offset = 0x04

Bit(s)	Name	Description	Access	Reset
15:14	PAIB	PA bias current control. 11:biggest 00:smallest	RW	01
13:12	OPDAVB	OPDA bias voltage control. 11:biggest 00:smallest	RW	01
11	-	Reserved	-	-
10:8	OPDAIB	OPDA bias current control. 111:biggest 000:smallest	RW	011
7:6	OPDTSIB	OPDTS bias current control. 11:biggest 00:smallest	RW	01
5:4	OPVBIB	OPVB bias current control. 11:biggest 00:smallest	RW	01

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

3	-	Reserved	-	-
3	KFEN	Karaoke Mix Function Enable 0:disable 1:enable Note: when enable this bit, MIC0INL and MIC0INR will be added and transmitted to PA	RW	0
2:0	OPGIB	OPG bias current control. 111:biggest 000:smallest	RW	101

5.1.2.5 DAC_ANALOG1

DAC Analog Register

Offset = 0x05

Bit(s)	Name	Description	Access	Reset
15	MICMUTE	MIC mute, 0: mute 1: unmute	RW	0
14	FMMUTE	FM mute, 0: mute 1: unmute	RW	0
13:11	-	Reserved	-	-
10	DACFL_FRMUTE	DACFL&FR Playback Mute 0: mute DAC Playback, 1: enable DAC playback	RW	0
9:8	PAIQ	PA output stage IQ control. 00:smallest 11:biggest	RW	00
7	-	Reserved	-	-
6	PASW	PA output swing select. 0:2.828Vpp 1:1.6Vpp This bit will control the attenuation before DAC's output goes into PA. Set this bit to 1 when PA is driving a headphone, there must to be attenuation for DAC's output (from about 2.4Vpp to 1.6Vpp) and PA will output 1.6Vpp at max volume. Set it to 0, there will be no attenuation and PA will output 2.4Vpp and can function as LINEOUT.	RW	1
5:0	VOLUME	Headphone Amp Volume Control. 41 levels in total (Values between 0b000000 and 0b101000 are valid. Any value over 0b101000 set to it will be	RW	000000

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		taken as 0b101000 actually. Reading value will just show what you have written to it.)		

5.1.2.6 DAC_ANALOG2

DAC Analog2 Register
Offset = 0x06

Bit(s)	Name	Description	Access	Reset
15	PAZD	PA OUTPUT Volume Near ZERO DETECT: 0:Invalid 1:Valid When this bit is selected 1,“click” of volume tuning will cut down. But if small volume is selected, this bit should be 0 to avoid some issue.	RW	0
14:12	-	Reserved	-	-
11	DACI	DAC Current select: 0:Small 1:Large	RW	0
10	P2IB	PA bias Double for ATP2 mode: 0: *1 1: *2	RW	0
9	ATP2CE	For ATP2,On-chip ramp Connect EN: 0: Disconnect 1: Connect	RW	0
8	PAVDC	Antipop2 pa discharge control: 0: switch open 1: switch close ,discharge	RW	0
7	-	Reserved	-	-
6	PAMIX	PA OUTPUT mix config: 0: NOT MIX 1:AOUTFL+AOUTFR to AOUTFL and AOUTFR	RW	0
5	DDOVV	Direct Drive overload protect and recover 0: Overload protect and recover is valid 1: Overload protect and recover is invalid	RW	0
4	OPVROEN	Analog circuit of the internal DAC_OPVRO enable, 0: Disable 1: Enable	RW	0
3	DDATPR	Direct Drive antipop_VRO Resistant Connect Enable: 0: disconnect 1: connect	RW	0
2:0	OPVROOSIB	Analog circuit of the internal DAC_OPVRO output stage IQ control.	RW	000

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		111:biggest 000:smallest		

5.1.2.7 DAC_ANALOG3

DAC Analog3 Register
Offset = 0x07

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14	OVLS	DAC VRO overload state: 1: VRO overload 0: VRO normal work state	R	0
13	VLCHD	Volume change Delay bit: 0: disable 1: enable	RW	0
12:11	-	Reserved	-	-
10	BIASN	All DAC&PA Bias enable 0: disable 1: enable	RW	0
9	ATPLP2_FR_FL	Channel FR&FL Antipop2 LOOP2 enable 0: disable 1: enable	RW	0
8:7	OPCM1IB	OPCM1 bias current control. 11:biggest 00:smallest	RW	01
6:4	OPVROIB	OPVRO bias current control. 000:smallest 111:biggest	RW	011
3	PAOSEN_FR_FL	PA FR&FL output stage enable 0: disable 1: enable	RW	0
2	PAEN_FR_FL	PA FR&FL enable 0: disable 1: enable	RW	0
1	DACEN_FL	DAC FL ANALOG enable 0: disable 1: enable	RW	0
0	DACEN_FR	FR DAC ANALOG enable 0: disable 1: enable	RW	0

5.1.2.8 ADC_DIGITALCTL

ADC Digital Control Register
Offset=0x08

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Bits	Name	Description	Access	Reset
15:13	-	Reserved	-	-
12	ADCOS	ADC OUTPUT SELECT 0: I2S OUTPUT 1: PCM	RW	0
11	ADLR	ADCL And ADCR Added enable 0: disable 1: enable *Note: this bit is designed for karaoke use, when this Bit is 1, ADCL data and ADCR data are added and transmitted to MCU.*	RW	0
10	-	Reserved	-	-
9:6	ADGC	ADC DIGITAL Gain Control 0000: 0dB 0001: 3dB 0010: 6dB 0011: 9dB 0100: 12dB 0101: 15dB 0110: 18dB 0111: 21dB 1000: 24dB 1001: 27dB 1010: 30dB 1011: 33dB 1100: 36dB 1101: 39dB 1110: 42dB 1111: 45dB	RW	0000
5	DCD	DMIC CLOCK Divide 0: div = 4 1: div = 2 (for voice recording)	RW	0
4	DCEN	DMIC CLOCK enable 0: disable 1: enable	RW	0
3	VREN	Voice Recording enable 0: disable 1: enable *Note: when this bit is set to 1, bit[5] also should be set to 1.*	RW	0
2	DRFS	DMIC Rising or falling edge sampling Select 0: Left channel sampling at rising edge, Right channel: sampling at falling edge; 1: Left channel sampling at falling edge, Right channel: sampling at rising edge;	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

1	DMLEN	DMIC Left filter enable 0: disable 1: enable	RW	0
0	DMREN	DMIC Right filter enable 0: disable 1: enable	RW	0

Note1: when DMIC is enabled, ADC should be disabled, and when ADC is enabled, DMIC should be disabled. That is to say, when ADC_DIGITALCTL bit[0] or bit[1] is 1, both ADC_CTL bit[2] and bit[3] should be set to 0. When ADC_CTL bit[2] or bit[3] is 1, both ADC_DIGITALCTL bit[0] and bit[1] should be set to 0.

In single channel mode, only when DMIC left filter is enabled, the output of DMIC right filter is zero, and if DMIC right filter is enabled, the output of DMIC left filter will be zero.

Note2: PCM0(for Master), PCM1(for BlueTooth), PCM2(for Base Band).

5.1.2.9 ADC_HPFCTL

ADC Digital Control Register

Offset=0x09

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15:8</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>7:6</td><td>SRSEL0</td><td>SR select for removing wind noise filter0
00:8kHz/11.025kHz/12kHz
01:16kHz/22.05kHz/24kHz
10:32kHz/44.1kHz/48kHz
11:Reserved</td><td>RW</td><td>00</td></tr>
<tr><td>5:3</td><td>WNHPF0CUT</td><td>For Wind Noise filter0 Cut Off frequency
<table>
<tr><td></td><td colspan="9">SR fs(Hz)</td></tr>
<tr><td></td><td>8k</td><td>11.025k</td><td>12k</td><td>16k</td><td>22.05k</td><td>24k</td><td>32k</td><td>44.1k</td><td>48k</td></tr>
<tr><td>000</td><td>82</td><td>113</td><td>122</td><td>82</td><td>113</td><td>122</td><td>82</td><td>113</td><td>122</td></tr>
<tr><td>001</td><td>102</td><td>141</td><td>153</td><td>102</td><td>141</td><td>153</td><td>102</td><td>141</td><td>153</td></tr>
<tr><td>010</td><td>131</td><td>180</td><td>196</td><td>131</td><td>180</td><td>196</td><td>131</td><td>180</td><td>196</td></tr>
<tr><td>011</td><td>163</td><td>225</td><td>245</td><td>163</td><td>225</td><td>245</td><td>163</td><td>225</td><td>245</td></tr>
<tr><td>100</td><td>204</td><td>281</td><td>306</td><td>204</td><td>281</td><td>306</td><td>204</td><td>281</td><td>306</td></tr>
<tr><td>101</td><td>261</td><td>360</td><td>392</td><td>261</td><td>360</td><td>392</td><td>261</td><td>360</td><td>392</td></tr>
<tr><td>110</td><td>327</td><td>450</td><td>490</td><td>327</td><td>450</td><td>490</td><td>327</td><td>450</td><td>490</td></tr>
<tr><td>111</td><td>408</td><td>563</td><td>612</td><td>408</td><td>563</td><td>612</td><td>408</td><td>563</td><td>612</td></tr>
</table></td><td>RW</td><td>000</td></tr>
<tr><td>2</td><td>HPF0DW</td><td>Select High Pass Filter0 for DC offset or Wind Noise
0: for DC offset
1: for Wind Noise</td><td>RW</td><td>0</td></tr>
<tr><td>1</td><td>HPF0LEN</td><td>High Pass Filter0 L Enable
0: enable
1: disable</td><td>RW</td><td>0</td></tr>
</table>

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

0	HPF0REN	High Pass Filter0 R Enable 0: enable 1: disable	RW	0

5.1.2.10 ADC_CTL

ADC control register

Offset=0x0A

Bits	Name	Description	Access	Reset
15	VMICINEN	Internal MIC Power VMIC Control 0: disable 1: enable	RW	0
14	FMLEN	FM input left channel enable; 0: Disable 1: Enable	RW	0
13	FMREN	FM input right channel enable; 0: Disable 1: Enable	RW	0
12:10	FMGAIN	FM input gain control: 000:-3.0dB 001:-1.5dB 010:0.0dB 011:1.5dB 100:3.0dB 101:4.5dB 110:6.0dB 111:7.5dB	RW	010
9	VMICEXEN	External MIC Power VMIC enabled 0: disabled 1: enabled	RW	0
8:7	VMICEXST	External MIC Power VMIC voltage setting 00: 2.7V 01: 2.9V 10: 3.1V 11: 3.2V	RW	01
6	MIC0LEN	MIC0 input L Channel Enabled 0: disable 1: enable	RW	0
5	MIC0REN	MIC0 input R Channel Enabled 0: disable 1: enable	RW	0
4	MIC0FDSE	MIC0 input Fully differential or Single ended select 0: Fully Differential; 1: Single Ended;	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

3	ADLEN	ADC Left Channel Enable 0: disable 1: enable	RW	0
2	ADREN	ADC Right Channel Enable 0: disable 1: enable	RW	0
1:0	ADCIS	Sigma-Delta A/D Input Select: 00: Select MIC 01: Select FM 10: Select Internal Analog Mixer Output (AOUT) 11: Reserved	RW	01

5.1.2.11 AGC_CTL0

AGC Control Register 0

Offset = 0x0B

Bits	Name	Description	Access	Reset
15:12	AMP1G0L	AMP1 Left Channel Gain Select at AGC0 disabled 0000: 16.5dB 0001: 18.0dB 0010: 19.5dB 0011: 21.0dB 0100: 22.5dB 0101: 24.0dB 0110: 25.5dB 0111: 27.0dB 1000: 28.5dB 1001: 30.0dB 1010: 31.5dB 1011: 33.0dB 1100: 34.5dB 1101: 36.0dB 1110: 37.5dB 1111: 39.0dB AMP1 AGC Gain can be Read out when AGC0 is enabled, and can be written and read out when AGC0 is disabled.	RW	1001

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

11:8	AMP1G0R	AMP1 Right Channel Gain Select at AGC0 disabled 0000: 16.5dB 0001: 18.0dB 0010: 19.5dB 0011: 21.0dB 0100: 22.5dB 0101: 24.0dB 0110: 25.5dB 0111: 27.0dB 1000: 28.5dB 1001: 30.0dB 1010: 31.5dB 1011: 33.0dB 1100: 34.5dB 1101: 36.0dB 1110: 37.5dB 1111: 39.0dB AMP1 AGC Gain can be Read out when AGC0 is enabled, and can be written and read out when AGC0 is disabled.	RW	1001
7	IMICSHD	Internal MIC Power Controlled by External MIC Plug enable 0: disable 1: enable	RW	0
6:3	-	Reserved	-	-
2:0	AMP0GR1	AMP1 Gain Boost Range Select 000: +3.0dB 001: +6.0dB 010: +9.0dB 011: +12.0dB 100: +13.5dB 101: +15.0dB 110: +16.5dB 111: +18.0dB	RW	011

5.1.2.12 AGC_CTL1

AGC Control 1 Register

Offset=0x0C

Bits	Name	Description	Access	Reset
15:13	-	Reserved	-	-

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

12:10	NGT0	AGC0 Noise gate statistic time, (SCY = 1.36ms) 000: 4*SCY 001: 8*SCY 010: 16*SCY 011: 32*SCY 100: 64*SCY 101: 128*SCY 110: 256*SCY 111: 512*SCY	RW	001
9:7	ATKT0	AGC0 Attack(Gain ramp-down) Time for every Gain step, (SCY = 683μs) 000: 1*SCY 001: 2*SCY 010: 4*SCY 011: 8*SCY 100: 16*SCY 101: 32*SCY 110: 64*SCY 111: 128*SCY	RW	010
6:4	DCYT0	AGC0 Decay(Gain ramp-up) Time for every Gain step, (SCY = 5.46ms) 000: 16*SCY 001: 32*SCY 010: 64*SCY 011: 128*SCY 100: 256*SCY 101: 512*SCY 110: 1024*SCY 111: 2048*SCY	RW	001
3:2	CMR0	AGC0 RC filter cutoff frequency select 00 :207Hz 01: 414Hz 10 : 828Hz 11 : 1.65kHz	RW	10
1:0	SCY0	AGC0 sense Cycle select 00 :341μs 01: 683μs 10 :1366μs 11 :2732μs	RW	10

5.1.2.13 AGC_CTL2

AGC Control 2 Register

Offset=0x0D

Bits	Name	Description	Access	Reset

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

15:13	TARGL0	AGC0 AMP1 Target level select at AMP2GR=+6dB 000: -42dBFS 001: -39dBFS 010: -36dBFS 011: -33dBFS 100: -30dBFS 101: -27dBFS 110: -24dBFS 111: -21dBFS	RW	100
12:10	NGTHSEL0	AGC0 Noise Gate Threshold select at +28.5dB Gain (Peak sense) 000: -27dBFS 001: -30dBFS 010: -33dBFS 011: -36dBFS 100: -39dBFS 101: -42dBFS 110: -45dBFS 111: -51dBFS	RW	011
9	MICAAEN	ADC MIC to PA Path differential compensation enable 0: Disable 1: Enable	RW	0
8	-	Reserved	-	-
7	RMSINSEL0	AGC0 input source select 0: Left 1: Right	RW	0
6	-	Reserved	-	-
5	NGSLEN0	AGC0 Noise Gate maintain current Gain or keep silence 0: maintain current Gain 1: keep silence	RW	0
4	NGTEN0	AGC0 Noise Gate function enabled 0: disabled 1: enabled	RW	0
3	ZEROC0	AGC0 Gain change at zero-cross enabled 0: disabled 1: enabled	RW	0
2	GREN0	AGC0 Gain_con gain reset function enabled 0: disabled 1: enabled	RW	0
1	AGC0LEN	AGC0 Left channel Enabled 0: disabled 1: enabled	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

0	AGC0REN	AGC0 Right channel Enabled 0: disabled 1: enabled	RW	0

5.1.2.14 ADC_ANALOG0

ADC Analog 0 Register

Offset=0x0E

Bits	Name	Description	Access	Reset
15:13	IVSRMSTN	IVSRMS bias tune 000: -25% 001: -18.75% 010: -12.5% 011: -6.25% 100: 0% (Baseline value 2μA) 101: +6.25% 110: +12.5% 111: +18.75%	RW	100
12: 8	-	Reserved	-	-
7: 5	OPBC1	The bias current select for OPAD1 in A/D: 000: 3μA 001: 4μA 010: 5μA 011: 6μA 100: 7μA 101: 8μA 100: 9μA 110: 10μA 111: 11μA	RW	011
4:3	OPBC23	The bias current select for OPAD2/3 in A/D: 00: 2μA 01: 3μA 10: 4μA 11: 5μA	RW	01
2:0	VRDABC	Audio A/D Voltage Reference bias current select: 000: 2μA 001: 3μA 010: 4μA … 110: 8μA 111: 9μA	RW	001

5.1.2.15 ADC_ANALOG1

ADC Analog 1 Register

Offset=0x0F

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Bits	Name	Description	Access	Reset
15:13	LPFBC	Audio A/D LPF bias current select: 000: 3.0μA 001: 3.5μA 010: 4.0μA 011: 4.5μA 100: 5.0μA 101: 5.5μA 110: 6.0μA 111: 6.5μA	RW	100
12:11	LPFBUFBC	FD LPF BUF OP bias current select: 00: 4μA 01: 5μA 10: 6μA 11: 7μA	RW	01
10	ADCBIAS	ADC Total Bias Tune 0: Normal 1: +50%	RW	0
9:8	-	Reserved	-	-
7:6	FD1BC	MIC Preamp FDOP1 bias current select : 00: 3μA 01: 4μA 10: 5μA 11: 6μA	RW	01
5:4	FD2BC	MIC Preamp FDOP2 bias current select : 00: 2μA 01: 3μA 10: 4μA 11: 5μA	RW	01
3:2	FD1BUFBC	MIC Preamp FDOP2 bias current select : 00: 2μA 01: 3μA 10: 4μA 11: 5μA	RW	01
1:0	FMBC	FM Pre-amplifiers bias current select: 00: 3μA 01: 4μA 10: 5μA 11: 6μA	RW	01

5.2 Audio Characteristics

The audio characteristics are measured under the following conditions:
AVCC = 2.9V, VCC = 3.1V, VDD = AVDD = 1.8V, Vref = 1.5V.

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

When testing DAC+PA or PA, a 16Ohm or 32Ohm load resistor is applied.

5.2.1 DAC+PA

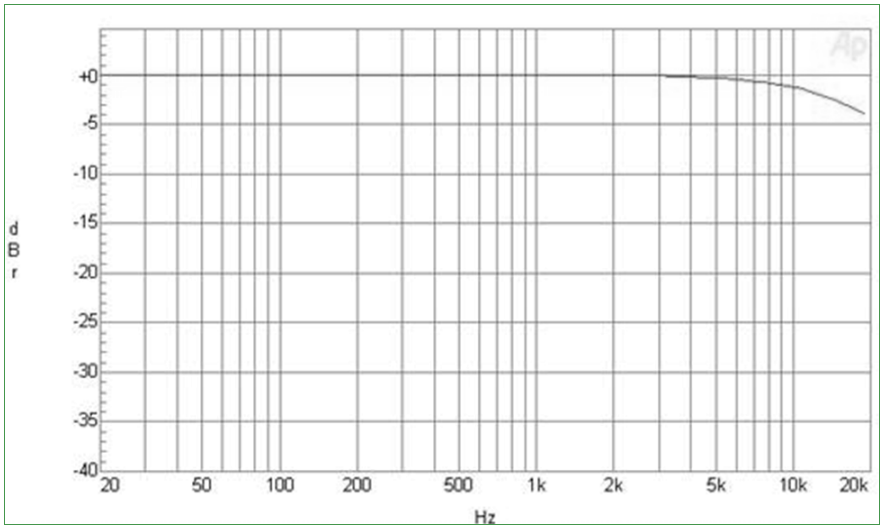
Table 5-5 DAC + Direct Drive PA characteristics

Characteristics	Min	Typ	Max	Unit
Noise		12		μV
SNR		93.3		dB
SNR(A-Weighting)		96.8		dB
Dynamic Range (-48dB Input)		90.7		dB
Dynamic Range (A-Weighting, -48dB Input)		94		dB
THD+N (0dB Input)		-80	-75	dB
Max Amp (0dB Input)		540		mV
Max Power		18.2		mW
Interchannel Isolation (1kHz, 0dB sine wave Input)		-73/-67 (Lmute/Rmute)		dB

Table 5-6 DAC + Non-Direct Drive PA @FS=48K characteristics

Characteristics	Min	Typ	Max	Unit
Noise		11		μV
SNR		93.5		dB
SNR(A-Weighting)		96.4		dB
Dynamic Range (-48dB Input)		90.6		dB
Dynamic Range (A-Weighting, -48dB Input)		93.5		dB
THD+N (0dB Input)		-81	-76	dB
Max Amp (0dB Input)		535		mV
Max Power		17.9@220μF		mW
Interchannel Isolation (1kHz, 0dB Sine wave Input)		-82/-70 (Lmute/Rmute)		dB

Figure 5-3 shows the frequency Response of DAC @ INPUT AMP = 0dB & load = 16R:



Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Figure 5-3 Frequency Response of DAC

Figure 5-4 below gives the FFT spectrum of DAC @ INPUT AMP = 0dB & 1 kHz:

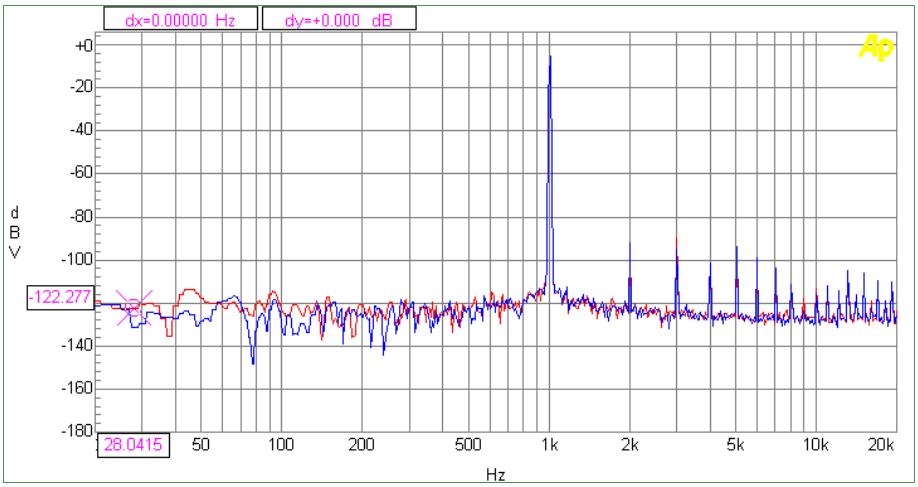


Figure 5-4 DAC FFT response

5.2.2 PA

Table 5-7 Non-Direct Drive PA characteristics

Characteristics	Min	Typ	Max	Unit
Noise		15		μV
SNR		92.4		dB
Dynamic Range		92.3		dB
THD+N		-84.2	-77	dB
Output Common Mode Voltage		1.5		Vrms
Full Scale Output Voltage@-60dB THD+N		0.596Vrms (1.785Vpp)		Vrms
Output Power @16.5Ohm		22.24		mW

Figure 5-5 below is the frequency Response of the Non-direct Drive PA @1.6Vpp input:

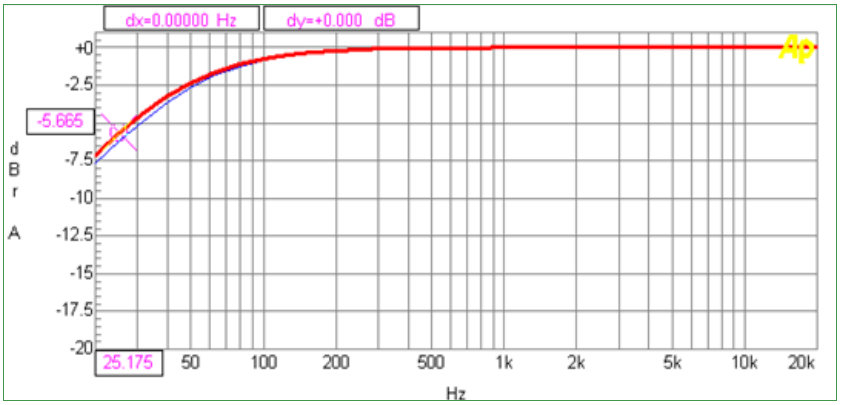


Figure 5-5 Frequency Response

Figure 5-6 gives the THD+N vs. INPUT AMP Curve of the Non-direct Drive PA:

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

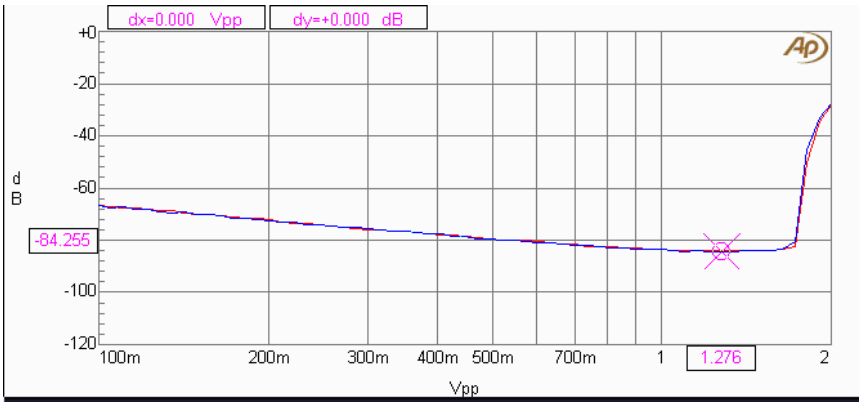


Figure 5-6 THD+N vs. INPUT AMP Curve

Table 5-8 Direct Drive PA Characteristics

Characteristics	Min	Typ	Max	Unit
Noise		15		μV
SNR		92.5		dB
Dynamic Range		92		dB
THD+N		-84.5	-78	dB
Output Common Mode Voltage		1.5		Vrms
Full Scale Output Voltage@-60dB THD+N		0.609Vrms (1.759Vpp)		Vrms
Output Power @16Ohm		23.2		mW

Figure 5-7 below is the Frequency Response of Direct Drive PA @1.6Vpp input:

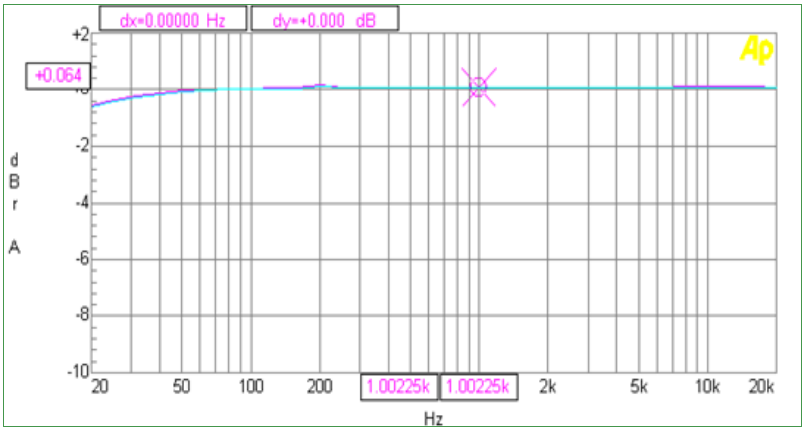


Figure 5-7 Frequency Response

Figure 5-8 is the THD+N vs. INPUT AMP Curve of the Direct Drive PA:

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

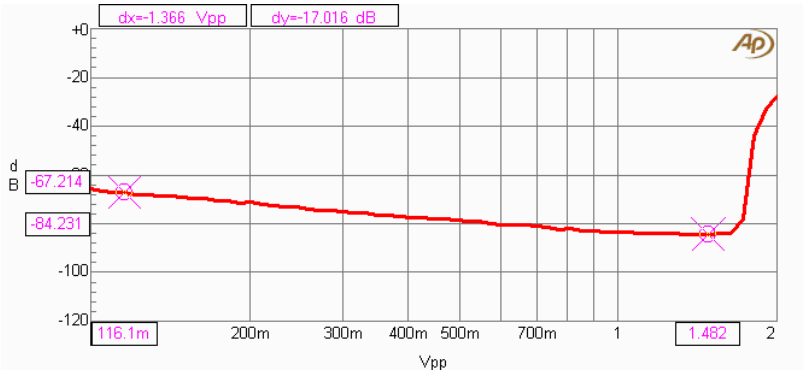


Figure 5-8 THD+N vs. Input AMP

5.2.3 ADC

Table 5-9 ADC characteristics

Test condition: Temp =25°C, AVCC = 3.0V, VCC = 1V, VDD = AVDD = 1.8V, Vref = 1.5V @2Vpp, 1 kHz, sine wave input

Characteristics	Min	Typ	Max	Unit
Dynamic Range (–40 dBFS Input), unweighting		89.6@48k		dB
Dynamic Range (–40 dBFS Input), weighting		91.5@48k		dB
THD+N, unweighting		-85.5@48k		dB
THD+N, weighting		-88.5@48k		dB

5.3 PCM

5.3.1 PCM Interface

There are 3 PCM modules integrated: PCM0 for Master, PCM1 for BlueTooth, PCM2 for Baseband. These three PCMs support Tx and Rx, only work in slave mode, the clock runs up to 2.048MHz.

Pulse Code Modulation (PCM) is a method of encoding an audio signal into digital format. PCM data can be Linear PCM(13~16bits), u-Law(8bits), A-Law(8bits). Long frame sync and short frame sync are supported. The Figure below gives a standard PCM transmission sequence.

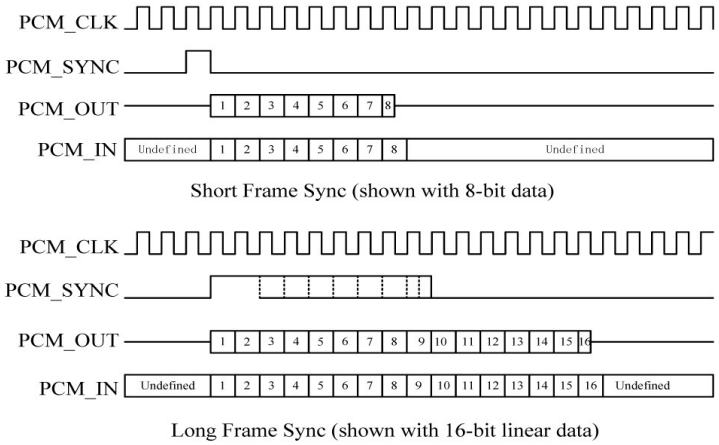


Figure 5-2 PCM Timing

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

5.3.2 Register List

Table 5-3 PCM IF Controller Registers Address

Name	Physical Base Address
PCM_IF	0xA0

Table 5-4 ADC Controller Registers

Offset	Register Name	Description
0x10	PCM0_CTL	PCM0 Control Register
0x11	PCM1_CTL	PCM1Control Register
0x12	PCM2_CTL	PCM2 Control Register
0x13	PCMIF_CTL	PCM Interface Control Register

5.3.3 Register Description

5.3.3.1 PCM0_CTL, PCM1_CTL, PCM2_CTL

PCM0/PCM1/PCM2 Control Register

PCM0_CTL Offset = 0x10

PCM1_CTL Offset = 0x11

PCM2_CTL Offset = 0x12

Bit(s)	Name	Description	Access	Reset
16:14	-	Reserved	-	-
13	EN	PCM Enable 0: Disable 1: Enable	RW	0
12	SEN	Sign Extension Enable (only when 16-bit slots are used). 0: Select zeros padding or audio gain. 1: Select sign extension. When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit compounded sample. When writing the bit is 1, the unused bits are both sign extension.	RW	0
11	SAMF	Sample Format 0: 8bit sample with 8 cycle slot duration 1: 8bit sample with 16 cycle slot duration	RW	0
10	IVEN	Inversion Enable. 0: Disable 1: Enable. When inversion is enabled, inversion is performed on even bits of A-Law and all bits of u-Law	RW	0
9	-	Reserved	-	-

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

8	FRMS	PCM Frame Mode Select 0: Short Frame Sync Mode 1: Long Frame Sync Mode	RW	0
7:6	-	Reserved	-	-
5	LMFR	LSB or MSB First. 0: MSB first 1: LSB first When transmitting and receiving voice samples.	RW	0
4	-	Reserved	-	-
3	DATO	PCM Data Output Mode. 0: Normal Output 1: Force PCM_OUT to output 0	RW	0
2:0	DATM	PCM Data Mode Select 000: u-Law(8-bit) 001: A-Law(8-bit) 010: linear PCM(13-bit) 011: linear PCM(14-bit) 100: linear PCM(15-bit) 101: linear PCM(16-bit)	RW	0

5.3.3.2 PCMIF_CTL

PCM Interface Control Register

Offset = 0x13

Bit(s)	Name	Description	Access	Reset
15:13	-	Reserved	-	-
12	P2OSS	PCM2OUT source select 0:ADC Right Channel 1:PCM1IN(From BT)	RW	0
11	P0OSS	PCM0OUT source select 0: voice recording when using MIC (MIC ADC record + Baseband Voice from PCM2 in + Master keytone or/and music from PCM0 in) 1: voice recording when using BT(BT voice from PCM1 in + Baseband Voice from PCM2 in + Master keytone or/and music from PCM0 in)	RW	0
10	-	Reserved	-	-
9	P1OSS	PCM1OUT source select 0:PCM2IN (from baseband) 1:PCM2IN + PCM0IN (baseband + master keytone or/and music)	RW	0
8:0	-	Reserved	-	-

PCM0(for Master), PCM1(for BlueTooth), PCM2(for Baseband)

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

6 TWI Interface

6.1 Features

ATC2609 can be accessed by Master through a standard TWI (Two-Wire Interface), which allows Master to write commands to and read status from ATC2609 by accessing its registers. TWI only occupies two pins namely SCL (Serial Clock) and SDA (Serial Data), information is transmitted serially on SDA and clock is driven on SCL by Master. ATC2609 is a slave device controlled by Master, The transmission speed of TWI interface supports 400Kbps and 3.4Mbps, 8-bit address and 16-bit data width with MSB transmitted first.

A typical sequence of Writing 16-bit data to a register is shown in the Figure below. A start bit is generated by Master, followed by a slave address, then register address and 16-bit data. A SACK acknowledge signal will be given by ATC2609 after every byte address or data transmission. The transmission stops when Master sends a stop bit. All the 16-bit data should be written before the register is updated.

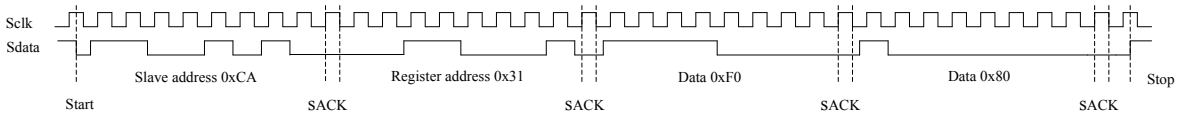


Figure 6-1 Writing 16-bit data to register through TWI bus

The Figure above shows a sequence of writing a 16-bit data 0xF080 to register 0x31, the slave address is 0xCA.

A typical 16-bit data read sequence is shown below. Firstly, Master writes slave address and register address to ATC2609. Then a start bit and the slave address is sent indicating a read sequence started. In the following 8-bit clock, Master reads data from ATC2609, during which Master sends a MACK signal every 8-bit data or address, mNACK signal will be sent to ATC2609 to stop the reading process, then Master generates a stop bit indicating the reading is completed.

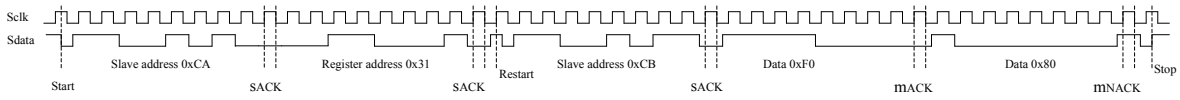


Figure 6-2 Reading 16-bit data from register through TWI bus

The Figure above illustrates Master reads 16-bit data 0xF080 from register 0x31, the slave address is 0xCA.

6.2 Register List

Table 6-1 TWI Interface Register Block Address

Block Name	Base Address
TWSI_REGISTER	0xF8

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Table 6-2 TWI Register Offset

Offset	Register Name	Description
0x08	SADDR	TWI serial interface slave device register

6.3 Register Description

6.3.1 SADDR

Two-Wire Serial interface slave device address register

Offset = 0x08

Bit(s)	Name	Description	Access	Reset
15:8	-	Reserved	-	-
7:1	SDA	Slave device address The register stores the slave device address used in slave mode.	RW	0b1100101
0	FTHM	Force to HS mode 0: Fast mode 1: High speed mode	RW	0x0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7 Power Management Unit

7.1 Features

The highly integrated Power Management Unit (PMU) in ATC2609 provides a full solution for the single cell lithium battery power system, the communication with Master is done through TWI interface. PMU consists of 6 DC-DCs, 10 LDOs, 12-bit multiplex ADC, one linear charging-management unit, Coulombmeter, and self-adaption power distribution control unit etc, automatically monitoring abnormal power conditions like overvoltage, overcurrent, undervoltage and overtemperature, etc.

The linear charging-management unit for Li-Ion battery adjusts the charging current automatically according to the battery's status, including trickle, CC (Constant Current) and CV (Constant Voltage) charging phase, with maximum charging current of 3A. Furthermore, it also supports overcharge protection and timeout protection, etc.

Self-Adaption Power Distribution (APDS) control module is an integrated unit inside PMU, which controls the power distribution and seamless power switching among BAT, VBUS and WALL to guarantee a stable power supply for the whole system. The minimum Standby current can be lower than 30μA. The input voltage of integrated 12-bit, 17-channel Analog-to-Digital converter (AuxADC) ranges from 0V to 3V, is used for detecting the voltage, current and temperature.

7.2 Module Description

7.2.1 DC-DC Module

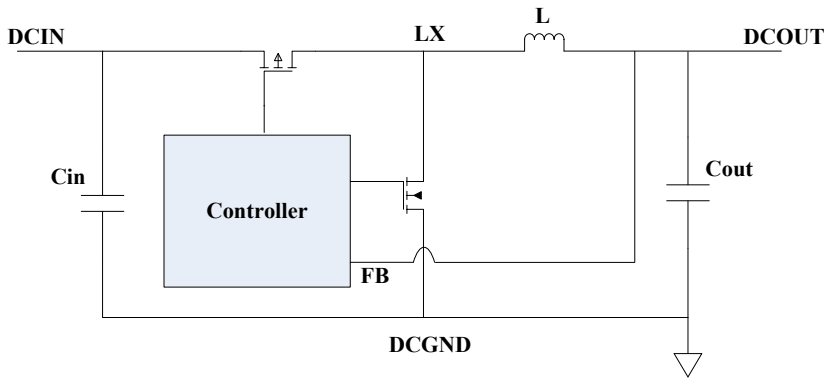


Figure 7-1 ATC2609 Buck DC-DC circuit diagram

ATC2609 integrates 6 Buck DC-DCs: DC-DC0, DC-DC1, DC-DC2, DC-DC3, DC-DC4, SW_DC-DC.

All the 6 Buck DC-DCs are synchronized controlled and integrate internal MOSFET. For normal application, one inductor and two capacitors should be applied outside. The recommended components selection is listed in Table 7-1 below.

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Table 7-1 External components selection for DC-DCs

Buck	Vin (V)	Vout (V)	Adjustable Voltage Step (mV)	Imax (A)	L	Cin (μF)	Cout (μF)
DC-DC0	3.0~5.5	0.6~2.2	6.25	2	1.0μH@DCR<0.03Ohm I>2A	10//0.1	10//0.1
DC-DC1	3.0~5.5	0.6~2.2	6.25	3	1.0μH@DCR<0.03Ohm I>3A	10//0.1	10//0.1
DC-DC2	3.0~5.5	0.6~2.2	6.25	2	1.0μH@DCR<0.03Ohm I>2A	10//0.1	10//0.1
DC-DC3	3.0~5.5	0.6~3.3	25	1.2	1.0μH@DCR<0.03Ohm I>1.2A	10//0.1	10//0.1
DC-DC4	3.0~5.5	0.6~2.2	6.25	2	1.0μH@DCR<0.03Ohm I>2A	10//0.1	10//0.1
SW_DC-DC	-	-	-	3	4.7μH@DCR<0.03Ohm I>3A	10//0.1	10

Note: "10//0.1" in table above means paralleled 10μF and 0.1μF capacitors.

The Efficiency characteristics of these DC-DCs are shown in Figure 7-2

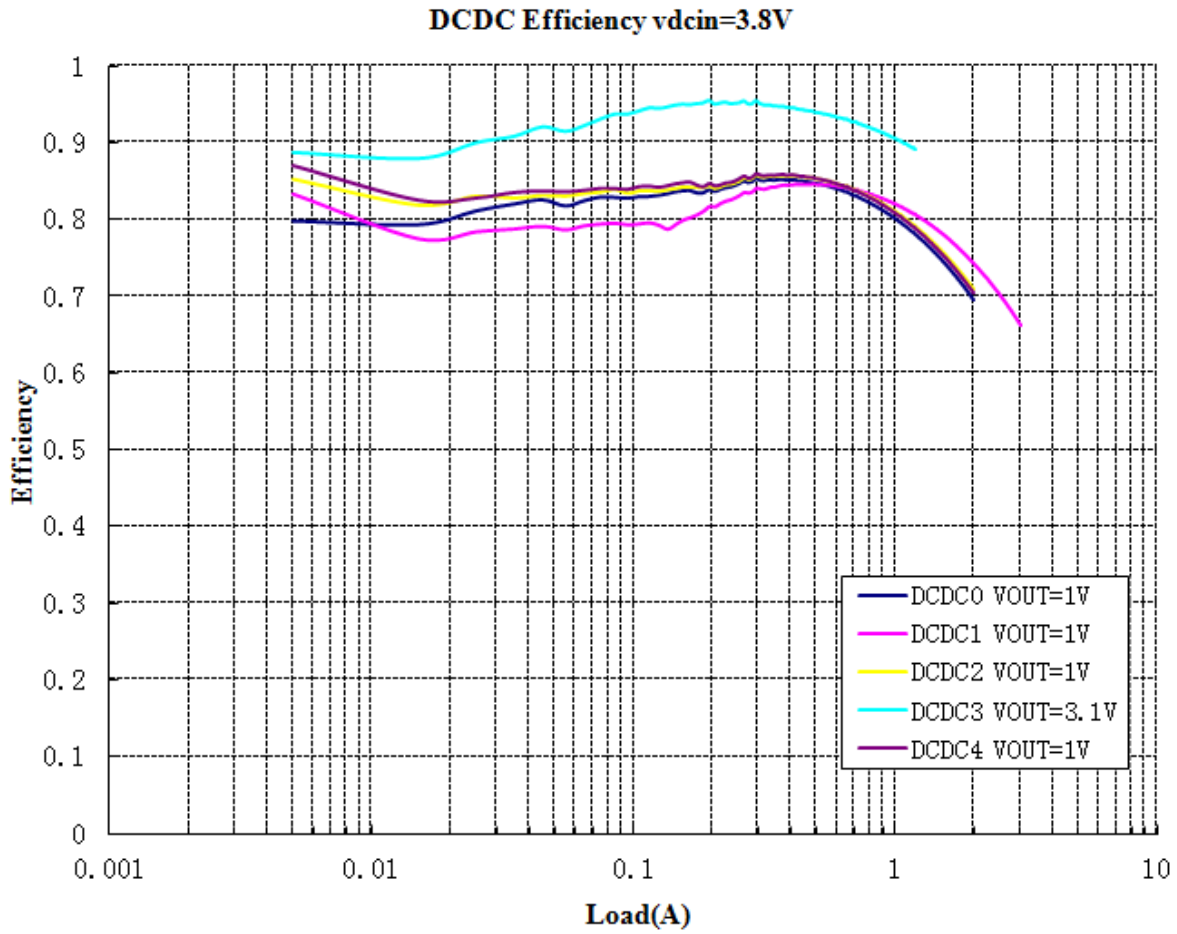


Figure 7-2 ATC2609 Buck DC-DCs Efficiency curve

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.2.2 LDO Module

ATC2609 integrates 10 LDOs, their specifications are listed below in Table 7-2. LDO support output overvoltage, overcurrent and undervoltage protection. Whenever the output voltage exceeds the overvoltage range, LDOs will generate an overvoltage interrupt, besides, the LDOs overvoltage protection can be enabled or disabled through the relevant register. Overcurrent and Undervoltage are the same mechanism.

Notes: LDO9 and LDO10 are used internally for SVCC and RTCVDD separately

Table 7-2 LDO regulators specifications

Regulator	Vin (V)	Vout(V)	Imax(mA)	Cin(μF)	Cout(μF)
LDO0	3.0~5.5	2.3~3.4	500	0.1//2.2	0.1//2.2
LDO1	3.0~5.5	2.3~3.4	500	0.1//2.2	0.1//2.2
LDO2	3.0~5.5	2.3~3.4	500	0.1//2.2	0.1//2.2
LDO3	3.0~5.5	0.7~3.3	50	0.1//1.0	0.1//1.0
LDO4	3.0~5.5	0.7~3.3	200	0.1//1.0	0.1//1.0
LDO6	3.0~5.5	0.85~3.3	200	0.1//1.0	0.1//1.0
LDO7	3.0~5.5	0.7~3.3	200	0.1//1.0	0.1//1.0
LDO8	3.0~5.5	0.7~3.3	200	0.1//1.0	0.1//1.0
LDO9	3.0~5.5	2.6~3.3	25	0.1//1.0	0.1//1.0
LDO10	3.0~5.5	1.8	20	0.1//1.0	0.1//1.0

7.2.3 Charger Module

ATC2609 integrates two constant current and constant voltage chargers, one is switch charger the other is linear charger, they provide battery detection, trickle current charging and it can adjust the charging current according to system power consumption. When an external adaptor is plugged in, the battery's existence is detected by ATC2609 PMU according to the voltage on BAT PIN, once SYSPWR is detected higher than battery voltage (VBAT), the charger will be enabled by software and ATC2609 PMU will manage the charging process automatically. Charging current can be configured through register (max 3A) and the real-time charging current can be read by the ADC charging current register.

The IC internal temperature and battery temperature are monitored throughout the charging process, once the temperature is detected higher or lower than the standard value, an interrupt signal will be sent, then software will take measures and charging process will be paused. The battery's temperature is measured by the circuit shown in Figure 7-3 below.

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

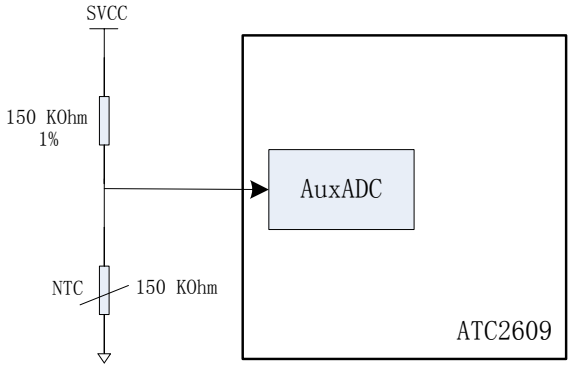


Figure 7-3 ATC2609 Battery Temperature Detecting Diagram

7.2.4 APDS Module

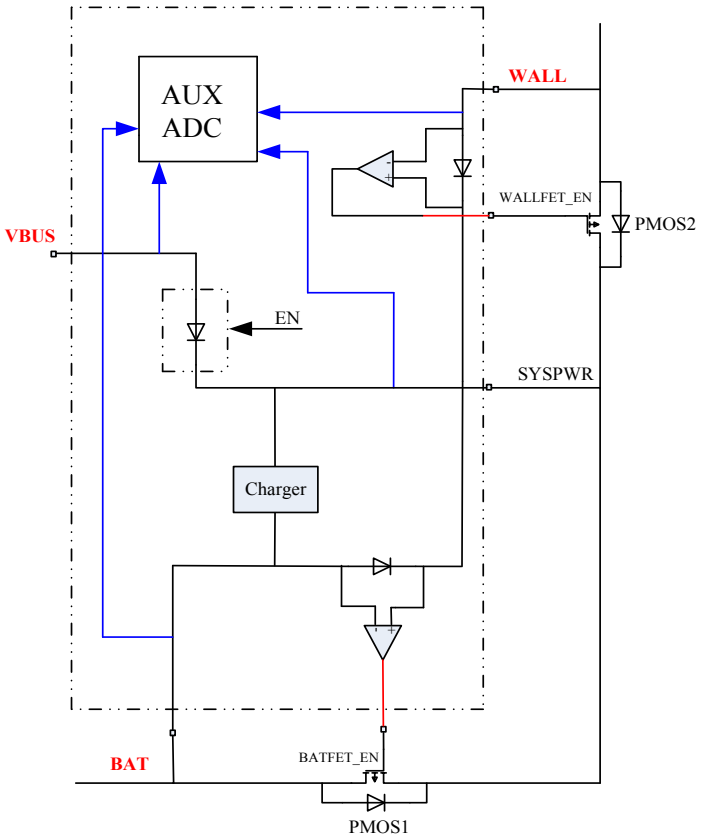


Figure 7-4 APDS Module Diagram

ATC2609 APDS (Adaptive Power Distribute System) block diagram is shown in Figure 7-4 above. SYSPWR is a public power supply node for all the DC-DCs and LDOs. PMU gets power from BAT, VBUS and WALL and then supplies to the public node SYSPWR through a diode respectively in the IC. To prevent current from flowing from VBUS to SYSPWR in OTG application, an enable control pin (EN) is applied to the diode between VBUS and SYSPWR. When this diode is disabled, the path from BUS to SYSPWR will be cut off completely.

PMU needs to supply high power, in order to reduce internal thermal dissipation, two external

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

MOSFET PMOS1 and PMOS2 are applied to bypass big current, see in Figure 7-4 above.
Voltages on BAT, VBUS, WALL and SYSPWR nodes as well as the current flows through each diode are monitored since the system is powered on. Once the output voltage of BAT exceeds the upper or lower settings, PMU will send BAT overvoltage or undervoltage interrupt to INTC module. When the current through BAT path is detected higher than the set value, a BAT overcurrent interrupt will be sent to INTC module, what's more, if this current exceeds overcurrent shut-off value, the power will be forced to shut off to protect IC. If VBUS and WALL are detected overvoltage, undervoltage or overcurrent, the same process will be triggered as BAT does.

7.2.5 Power Modes

According to the application, the following 5 types of power modes are distinguished:

- **S1-Working Mode**: In Working Mode, Master can work normally including its kernel and IOs, that is to say, LDO2 and LDO3 needed by the Master and ATC2609 must work properly. LDO2, LDO3, LDO9, LDO10 and their related control logic circuits should work. Other regulators can be either on or off. This state is called S1.
- **S2-Standby Mode**: Both Master IC's kernel and IOs are shut off in this mode, LDO2 and LDO3 are powered off accordingly, LDO9 and LDO10 is still on, essential information is saved in DDR for fast start-up, DC-DC2 should work normally. The communication between Master and ATC2609 is disabled. We called this state S2.
- **S3-Sleep Mode**: When the device is not used for a long time, the system will enter S3 state, which is a low power state. In this case, DDR will be power down, but SYSPWR still supplies the system. Only LDO9 and LDO10 is on, others are all power off.
- **S3A-Relaxation Mode**: this mode is an intermediate state, its external power is same with S3, but a little different internally. This working mode is used to sustain the function of ADC, after a period of time the battery enters a relaxation state, then the coulometer level can be updated.
- **S4-Deep Sleep Mode**: In this mode, the power consumption is reduced more deeply than standby mode, LDO9 is power down, only LDO10 is on.

Wakeup elements:

The system can be woke up in different conditions, which involves several wake up elements including ONOFF, ALARM, WKIRQ, RESET, REM_CON, USB, WALL, HDSW, IR. In S2 and S3, each of the elements above can wake up the system. In S4, SVCC is shut off, only RTCVDD exists, so only WKIRQ, REM_CON and IR cannot wake up the system, others can wake up the system. Either long or short press on ONOFF button can wake up the system, which can be enabled or disabled by the register. In S1 mode, the system can be configured into S2, S3 or S4 by software, setting the related bits EN_S1, EN_S2, EN_S3, shown in Table 7-3 below.

Table 7-3 Power State changed by Software

Power State	EN_S1	EN_S2	EN_S3	T_ACK
S4	0	0	0	1
S3	0	0	1	1
S3A	0	0	x	0
S2	0	1	x	x
S1	1	x	x	x

Note: When the system need to go into S2 from S1, set EN_S2=1 first, then write 0 to EN_S1, to

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

switch the system from S1 mode to S2.

Overcurrent protection:

If one of the LDOs is overcurrent, and overcurrent interrupt is sent, PWROK will be pulled down first, and then it will enter Standby state by setting EN_S2, EN_S3 and T_ACK.

If overcurrent is detected on BAT, WALL or VBUS, and its overcurrent shut off function is enabled, then it will entering Standby state according to the settings of EN_S2, EN_S3 and T_ACK.

Overtemperature protection:

When the temperature in IC exceeds the settings, and its overtemperature protection is enabled, then the system will enter Standby state by setting EN_S2, EN_S3 and T_ACK automatically.

7.2.6 POR and Power ON/OFF Sequence Module

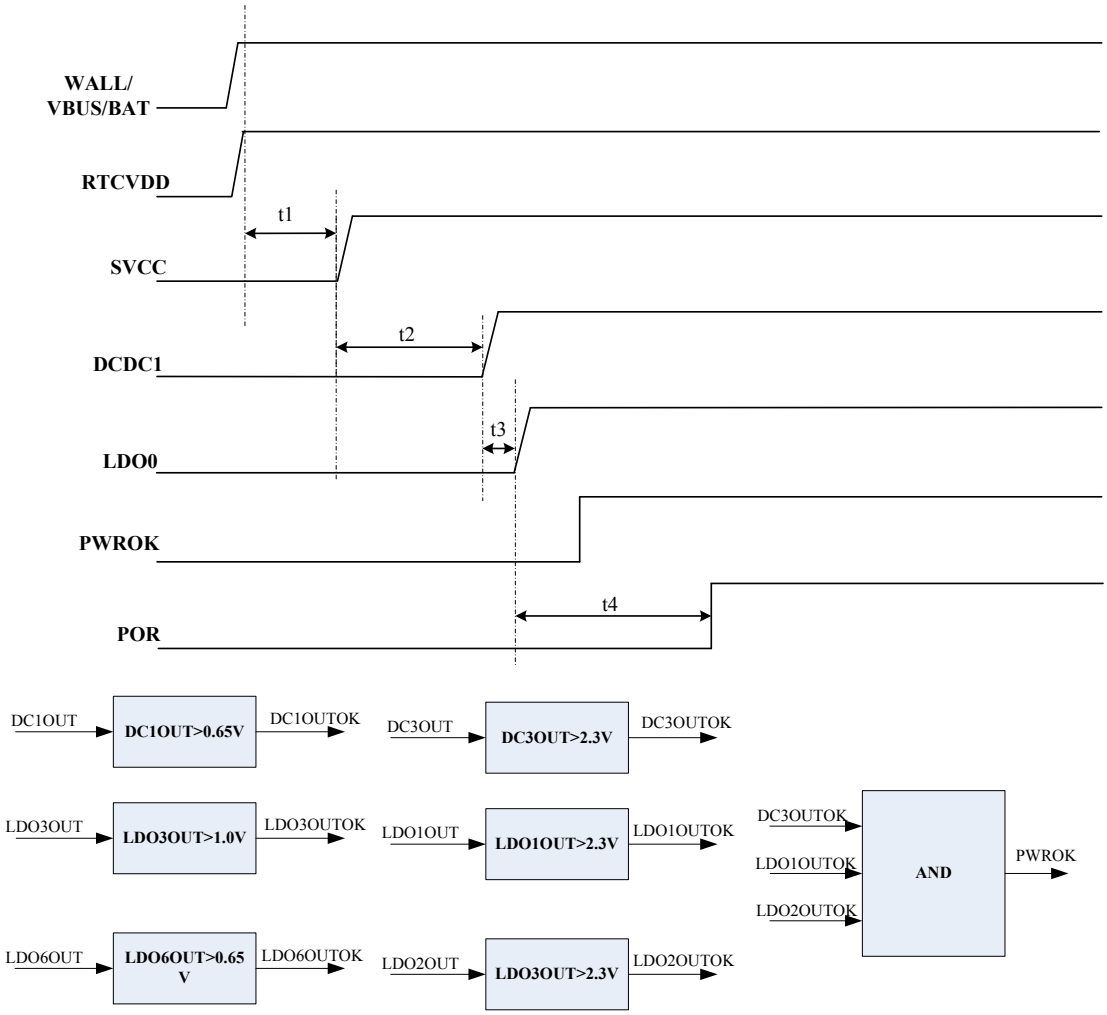


Figure 7-5 Power on Sequence

Figure 7-5 above shows ATC2609 power on sequence, the power of BAT or WALL or VBUS is turned on firstly, RTCVDD and SVCC will be generated closely after that. Then ATC2609's core voltage (1.8V) and Master's core voltage (1.0V) will be applied. The high-voltage supply for ATC2609 and Master will be generated afterwards. At last, when all these power is stable, the POR

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

signal will be sent to Master, which indicates the Master starts to run. The timing parameter is of power on sequence is listed in Table 7-4 below.

Table 7-4 Timing Parameter of Power on Sequence

Parameter	Min	Max
t1	35ms	
t2	56ms	
t3	6ms	48ms
t4	40ms	

If the system is set to power down by software, Master will send commands to ATC2609, on receiving the commands.

7.2.7 ONOFF & Reset Module

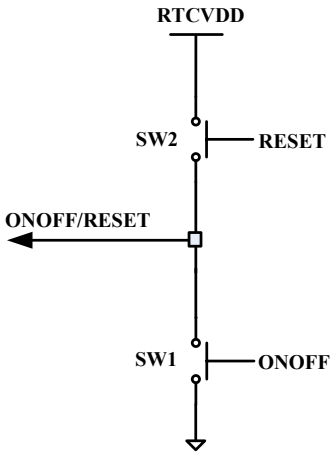


Figure 7-6 ONOFF & Reset Module Diagram

In the PMU, ONOFF and Reset multiplex one PIN (ONOFF/RESET), shown in figure 7-6. Either ONOFF or RESET button is pressed down, SYSRST or SYSONOFF signal will be high and generates a trigger signal to PMU through ONOFF/RESET pin accordingly. If the RESET and ONOFF buttons are pressed down at the same time, all the registers in RTCVDD voltage domain will be reset.

Long press on ONOFF button for more than a setting period (6s, 8s, 10s or 12s) will trigger a same function like P_RESET to reset the whole system.

7.2.8 Coulombmeter

Built-in Coulombmeter supports accurate battery capacity monitor.

7.3 Register List

Table 7-5 PMU Block Address

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Name	Base Address
PMU	0x00

Table 7-6 PMU Controller Registers

Offset	Register Name	Description
0x00	PMU_SYS_CTL0	PMU SYSTEM CONTROL Register0
0x01	PMU_SYS_CTL1	PMU SYSTEM CONTROL Register1
0x02	PMU_SYS_CTL2	PMU SYSTEM CONTROL Register2
0x03	PMU_SYS_CTL3	PMU SYSTEM CONTROL Register3
0x04	PMU_SYS_CTL4	PMU SYSTEM CONTROL Register4
0x05	PMU_SYS_CTL5	PMU SYSTEM CONTROL Register5
0x06	PMU_SYS_CTL6	PMU SYSTEM CONTROL Register6
0x07	PMU_SYS_CTL7	PMU SYSTEM CONTROL Register7
0x08	PMU_SYS_CTL8	PMU SYSTEM CONTROL Register8
0x09	PMU_SYS_CTL9	PMU SYSTEM CONTROL Register9
0x0A	PMU_BAT_CTL0	PMU BAT CONTROL Register0
0x0B	PMU_BAT_CTL1	PMU BAT CONTROL Register1
0x0C	PMU_VBUS_CTL0	PMU VBUS CONTROL Register0
0x0D	PMU_VBUS_CTL1	PMU VBUS CONTROL Register1
0x0E	PMU_WALL_CTL0	PMU WALL CONTROL Register0
0x0F	PMU_WALL_CTL1	PMU WALL CONTROL Register1
0x10	PMU_SYS_PENDING	PMU SYSTEM Pending Register
0x11	PMU_APDS_CTL0	PMU APDS CONTROL Register0
0x12	PMU_APDS_CTL1	PMU APDS CONTROL Register1
0x13	PMU_APDS_CTL2	PMU APDS CONTROL Register2
0x14	PMU_CHARGER_CTL	PMU CHARGER CONTROL Register
0x16	PMU_SWCHG_CTL0	PMU SW_CHARGER CONTROL Register0
0x17	PMU_SWCHG_CTL1	PMU SW_CHARGER CONTROL Register1
0x18	PMU_SWCHG_CTL2	PMU SW_CHARGER CONTROL Register2
0x19	PMU_SWCHG_CTL3	PMU SW_CHARGER CONTROL Register3
0x1A	PMU_SWCHG_CTL4	PMU SW_CHARGER CONTROL Register4
0x1B	PMU_DC_OSC	PMU DC-DC OSC CONTROL Register
0x1C	PMU_DC0_CTL0	PMU DC-DC0 CONTROL Register0
0x23	PMU_DC1_CTL0	PMU DC-DC1 CONTROL Register0
0x2A	PMU_DC2_CTL0	PMU DC-DC2 CONTROL Register0
0x31	PMU_DC3_CTL0	PMU DC-DC3 CONTROL Register0
0x79	PMU_DC4_CTL0	PMU DC-DC4 CONTROL Register0
0x38	PMU_DC_ZR	PMU DC-DC Status Register
0x39	PMU_LDO0_CTL0	PMU LDO0 CONTROL Register0
0x3B	PMU_LDO1_CTL0	PMU LDO1 CONTROL Register0
0x3D	PMU_LDO2_CTL0	PMU LDO2 CONTROL Register0
0x3F	PMU_LDO3_CTL0	PMU LDO3 CONTROL Register0
0x41	PMU_LDO4_CTL0	PMU LDO4 CONTROL Register0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

0x45	PMU_LDO6_CTL0	PMU LDO6 CONTROL Register0
0x47	PMU_LDO7_CTL0	PMU LDO7 CONTROL Register0
0x49	PMU_LDO8_CTL0	PMU LDO8 CONTROL Register0
0x4B	PMU_LDO9_CTL	PMU LDO9 CONTROL Register0
0x4C	PMU_OV_INT_EN	PMU OVER VOLTAGE INT ENABLE Register
0x4D	PMU_OV_STATUS	PMU OVER VOLTAGE Status Register
0x4E	PMU_UV_INT_EN	PMU UNDER VOLTAGE INT ENABLE Register
0x4F	PMU_UV_STATUS	PMU UNDER VOLTAGE Status Register
0x50	PMU_OC_INT_EN	PMU OVER CURRENT INT ENABLE Register
0x51	PMU_OC_STATUS	PMU OVER CURRENT Status Register
0x52	PMU_OT_CTL	PMU OVER TEMPERTURE CONTROL Register
0x53	PMU_CM_CTL0	PMU Coulometer Module CONTROL Register
0x80	PMU_PWR_STATUS	PMU POWER Status Register
0x81	PMU_S2_PWR	PMU S2 POWER CONTROL Register
0x82	CLMT_CTL0	PMU Coulometer Module CONTROL Register
0x83	CLMT_DATA0	PMU Coulometer Module DATA Register0
0x84	CLMT_DATA1	PMU Coulometer Module DATA Register1
0x85	CLMT_DATA2	PMU Coulometer Module DATA Register2
0x86	CLMT_DATA3	PMU Coulometer Module DATA Register3
0x56	PMU_ADC12B_I	PMU BATIADC Register
0x57	PMU_ADC12B_V	PMU BATVADC Register
0x89	CLMT_OCV_TABLE	PMU Coulometer Module OCV TABLE Register
0x8A	CLMT_R_TABLE	PMU Coulometer Module R TABLE Register

7.4 Register Description

7.4.1 PMU_SYS_CTL0

PMU_SYS_CTL0 Register (RTCVDD) (default 0xE055)
Offset = 0x00

Bit(s)	Name	Description	Access	Reset
15	USB_WK_EN	VBUS wake up enable, when exceeds the threshold voltage 1:VBUS can wake up 0:VBUS can't wake up	RW	0x1
14	WALL_WK_EN	WALL wake up enable, when exceeds the threshold voltage 1:WALL can wake up 0:WALL can't wake up	RW	0x1
13	ONOFF_LONG_WK_EN	ONOFF long press wake up enable 1:ONOFF can wake up	RW	0x1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:ONOFF can't wake up		
12	ONOFF_SHORT_WK_EN	ONOFF short press wake up enable 1:ONOFF can wake up 0:ONOFF can't wake up	RW	0x0
11	WKIRQ_WK_EN	WKIRQ wake up enable 1:WKIRQ can wake up 0:WKIRQ can't wake up	RW	0x0
10	RESTART_EN	Restart enable 1:enable 0:default the default value is 0, when it is set to 1 (if WALL or VBUS exists, WALL or VBUS wakeup will be HW disabled), the system will enter Standby mode automatically, then wakes up automatically 2sec later, this bit will be cleared to 0 at the same time.	RW	0x0
9	REM_CON_WK_EN	REM_CON button pressed wake up enable 1:Rem_con can wake up 0:Rem_con can't wake up	RW	0x0
8	ALARM_WK_EN	Alarm wake up enable 1:Alarm can wake up 0:Alarm can't wake up	RW	0x0
7	HDSW_WK_EN	Hard switch wake up enable 0:No 1:Yes	RW	0x0
6	RESET_WK_EN	Reset wake up enable 0:No 1:Yes	RW	0x1
5	IR_WK_EN	IR wake up enable 0:No 1:Yes	RW	0x0
4:3	VBUS_WK_TH	VBUS wake up threshold voltage 00:4.05V 01:4.20V 10:4.35V 11:4.50V	RW	0x2
2:1	WALL_WK_TH	WALL wake up threshold voltage 00:4.05V 01:4.20V 10:4.35V 11:4.50V	RW	0x2
0	ONOFF_MUXKEY_EN	ONOFF multiplex enable 0:Disable (No P_RESET key) 1:Enable (With P_RESET key)	RW	0x1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.2 PMU_SYS_CTL1

PMU_SYS_CTL1 Register (RTCVDD) (default 0x000E)
Offset = 0x01

Bit(s)	Name	Description	Access	Reset
15	USB_WK_FLAG	VBUS wakeup flag 1:VBUS wakeup 0:No VBUS wakeup	R	0x0
14	WALL_WK_FLAG	WALL wakeup flag 1:WALL wakeup 0:No WALL wakeup	R	0x0
13	ONOFF_LONG_WK_FLAG	ONOFF long press wakeup flag 1:ONOFF long press wakeup 0:No ONOFF long press wakeup	R	0x0
12	ONOFF_SHORT_WK_FLAG	ONOFF short press wakeup flag 1:ONOFF short press wakeup 0:No ONOFF short press wakeup	R	0x0
11	WKIRQ_WK_FLAG	WKIRQ wakeup flag 1: WKIRQ wakeup 0: No WKIRQ wakeup	R	0x0
10	RESTART_WK_FLAG	RESTART wakeup flag 1: RESTART wakeup 0: No RESTART wakeup	R	0x0
9	REM_CON_WK_FLAG	REM_CON wakeup flag 1: REM_CON wakeup 0: No REM_CON wakeup	R	0x0
8	ALARM_WK_FLAG	Alarm wakeup flag 1:Alarm wakeup 0: No Alarm wakeup	R	0x0
7	HDSW_WK_FLAG	HDSW wakeup flag 1:HDSW wakeup 0: No HDSW wakeup	R	0x0
6	RESET_WK_FLAG	reset wakeup flag 1:Reset wakeup 0: No reset wakeup	R	0x0
5	IR_WK_FLAG	IR wakeup flag 1:IR wakeup 0: No IR wakeup	R	0x0
4:3	LB_S4	Low power state enter S4 voltage setting 00:2.9V 01:3.0V 10:3.1V 11:3.3V When the system is in S1, S2, S3A, S3 and the	RW	0x1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		relative transition state, if the Battery voltage is lower than settings and there is no VBUS and WALL detected, the system enters S4 directly.		
2	LB_S4_EN	Low Power state enter S4 enable (including enable detection) 0:Disable 1:Enable	RW	0x1
1	ENRTCOSC	Internal 32kHz clock enable 0:disable 1:enable	RW	0x1
0	EN_S1	Enter S1state enable (this bit will be cleared to 0 when leaving S1) 0:Do not enter S1 1:Enter S1	RW	0x0

7.4.3 PMU_SYS_CTL2

PMU_SYS_CTL2 Register (RTCVDD) (default 0x0680)
Offset = 0x02

Bit(s)	Name	Description	Access	Reset
15	ONOFF_PRESS	ONOFF key is pressed or not 0:ONOFF key is not pressed 1:ONOFF key is pressed	R	0x0
14	ONOFF_SHORT_PRESS	ONOFF short press pending 0:No ONOFF short press happen 1: ONOFF short press happen Write 1 clear to 0	RW	0x0
13	ONOFF_LONG_PRESS	ONOFF long press pending 0:No ONOFF long press happen 1:ONOFF long press happen Write 1 clear to 0	RW	0x0
12	ONOFF_LSP_INT_EN	ONOFF key long or short press interrupt enable 0:disable 1:enable	RW	0x0
11:10	ONOFF_PRESS_TIME	ONOFF key press time settings **00:** 60ms < t < 0.5s; judged as short press; t >= 0.5s, judged as long press; **01:** 60ms < t < 1s, judged as short press; t >= 1s, judged as long press;	RW	0x01

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		10: 60ms < t < 2s, judged as short press; t >= 2s, judged as long press; **11:** 60ms < t < 4s, judged as short press; t >= 4s, judged as long press;		
9	ONOFF_RESET_EN	ONOFF long press reset function enable 0:disable 1:enable	RW	0x1
8:7	ONOFF_RESET_TIME_SEL	Long press ONOFF send Reset time selection 00:6s 01:8s 10:10s 11:12s	RW	0x01
6	S2_TIMER_EN	S2 timer enable 0:Disable 1:Enable When S2timer is enabled, once the system enters S2 state, S2timer starts to count, when it counts up the system will enter S3A state.	RW	0x0
5:3	S2TIMER	S2timer 000:6min 001:16min 010:31min 011:61min 100:91min 101:121min 110:151min 111:181min	RW	0x0
2	ONOFF_PRESS_PD	ONOFF key press happen pending 0:No ONOFF key press happen 1:ONOFF key press happen Writing 1 clears to 0	RW	0x0
1	ONOFF_PRESS_INT_EN	ONOFF key press interrupt enable 0:disable 1:enable	RW	0x0
0	PMU_A_EN	PMU simulation acceleration mode enable 0:diasble 1:enable	RW	0x0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.4 PMU_SYS_CTL3

PMU_SYS_CTL3 Register (RTCVDD) (default 0x0000)
Offset = 0x03

Bit(s)	Name	Description	Access	Reset
15	EN_S2	Enter S2 state enable 0:do not enter S2 1:enter S2	RW	0x0
14	EN_S3	Enter S3 state enable 0:do not enter S3 1:enter S3	RW	0x0
13	S3_TIMER_EN	S3 timer enable 0:Disable 1:Enable If S3 timer is enabled, when the system enters S3 state, S3 timer starts to count, when it counts up, the system will enter S4 state.	RW	0x0
12:10	S3TIMER	S3timer 000:6min 001:16min 010:31min 011:61min 100:91min 101:121min 110:151min 111:181min	RW	0x0
9:0	-	Reserved	-	-

7.4.5 PMU_SYS_CTL4

PMU_SYS_CTL4 Register (RTCVDD) (default 0xB000)
Offset = 0x04

Bit(s)	Name	Description	Access	Reset
15:8	-	Reserved	-	-
7:5	AUXIN1	AUXIN1 Multiplexing 000: AUXIN1 001: SGPIO2 (<1MHz) 010: WKUP 011: IR 100: 32kHz clock is sent Others: Reserved	RW	0x0
4:2	AUXIN0	AUXIN0 Multiplexing	RW	0x0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		000: AUXIN0 001: SGPIO1 (<1MHz) 010: WKUP 011: IR 100: 32kHz clock is sent Others: Reserved		
1:0	REMCON	REMCON Multiplexing 00: REMCON 01: SGPIO0 (<1MHz) 10: WKUP 11: IR	RW	0x0

7.4.6 PMU_SYS_CTL5

PMU_SYS_CTL5 Register (RTCVDD) (default 0x0180)
Offset = 0x05

Bit(s)	Name	Description	Access	Reset
15	WKIRQ_PD	WKIRQ pending 0:WKIRQ is not active 1:WKIRQ is active Writing 1 clears to 0	RW	0x0
14:13	WKIRQ_TPYE	WKIRQ types 00:High level active 01:Low level active 10:Rising edge-triggered 11:Falling edge-triggered	RW	0x0
12	WKIRQ_INT_EN	WKIRQ interrupt enable 0: disable 1: enable	RW	0x0
11	REMCON_PD	REMCON pending 0: REMCON is not pressed 1: REMCON is pressed Writing 1 clears to 0	RW	0x0
10	REMCON_INT_EN	Rem_con interrupt enable 0: Disable 1: Enable	RW	0x0
9	REMCON_DECT_EN	Rem_con wakeup detection enable 0: Disable 1:Enable	RW	0x0
8	VBUSWKDTEN	VBUS wakeup detection enable 0: Disable 1:Enable	RW	0x1
7	WALLWKDTEN	WALL wakeup detection enable	RW	0x1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0: Disable 1:Enable		
6:5	IBIAS	IBIAS 00:lower 01:low 10:high 11:higher	RW	0x0
4:0	-	Reserved	-	-

7.4.7 PMU_SYS_CTL6

PMU_SYS_CTL6 Register (RTCVDD) (default 0x0000)
Offset = 0x06

Bit(s)	Name	Description	Access	Reset
15:11	-	Reserved	-	-
10:8	SGPIO_FUN_SEL	SGPIO[2:0] In/Out selection 0:Input 1:Output	RW	0x0
7:3	-	Reserved	-	-
2:0	SGPIO_DATA	SGPIO[2:0] DATA	RW	0x0

7.4.8 PMU_BAT_CTL0

PMU_BAT_CTL0 Register (RTCVDD) (default 0x5680)
Offset = 0x0A

Bit(s)	Name	Description	Access	Reset
15:14	BAT_UV_VOL	BAT Undervoltage interrupt voltage setting 00:3.1V 01:3.3V 10:3.4V 11:3.5V	RW	0x1
13:12	BAT_OV_VOL	BAT overvoltage interrupt voltage setting 00:4.3V 01:4.4V 10:4.5V 11:4.8V	RW	0x1
11:8	BAT_OC_SET	BAT overcurrent interrupt current setting 0000:200mA 0001:300mA 0010:400mA 0011:500mA 0100:600mA	RW	0x6

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0101:700mA 0110:800mA 0111:900mA 1000:1000mA 1001:1200mA 1010:1400mA 1011:1600mA 1100:1800mA 1101:2000mA 1110:2200mA 1111:2500mA The current detected is flowing from BAT to SYSPWR through the diode, overcurrent signal debounce time is 1ms.		
7:6	BAT_OC_SHUTOFF_SET	BAT overcurrent shutoff current setting 00:1000mA 01:2000mA 10:2500mA 11:3000mA Overcurrent signal debounce is 1ms	RW	0x2
5:0	-	Reserved	-	-

7.4.9 PMU_BAT_CTL1

PMU_BAT_CTL1 Register (RTCVDD) (default 0xE000)
Offset = 0x0B

Bit(s)	Name	Description	Access	Reset
15	BAT_OC_EN	BAT overcurrent detection enable 0:disable 1:enable	RW	1
14	BAT_OV_EN	BAT overvoltage detection enable 0:disable 1:enable	RW	1
13	BAT_UV_EN	BAT undervoltage detection enable 0:disable 1:enable	RW	1
12	BAT_OC_INT_EN	BAT overcurrent interrupt enable 0:disable 1:enable	RW	0
11	BAT_OV_INT_EN	BAT overvoltage interrupt enable 0:disable 1:enable	RW	0
10	BAT_UV_INT_EN	BAT undervoltage interrupt enable	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:disable 1:enable		
9	BAT_OC_SHUTOFF_EN	BAT overcurrent cutoff enable 0:disable 1:enable	RW	0
8:0	-	Reserved	-	-

7.4.10 PMU_VBUS_CTL0

PMU_VBUS_CTL0 Register (RTCVDD) (default 0xA680)
Offset = 0x0C

Bit(s)	Name	Description	Access	Reset
15:14	VBUS_UV_VOL	VBUS undervoltage interrupt voltage setting 00:3.8V 01:4.0V 10:4.3V 11:4.5V	RW	0x2
13:12	VBUS_OV_VOL	VBUS overvoltage interrupt voltage setting 00:5.3V 01:5.5V 10:5.6V 11:5.8V	RW	0x2
11:8	VBUS_OC_SET	VBUS overcurrent interrupt current setting 0000:200mA 0001:400mA 0010:600mA 0011:800mA 0100:1000mA 0101:1200mA 0110:1400mA Others: reserved The current under detection is the current flowing from VBUS to SYSPWR through the diode, the overcurrent signal debounce time is 1ms	RW	0x6
7:6	VBUS_OC_SHUTOFF_SET	VBUS overcurrent shutoff current setting 00:500mA 01:1000mA 10:1500mA	RW	0x6

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		11:2000mA The overcurrent signal debounce time is 1ms		
5:0	-	Reserved	-	-

7.4.11 PMU_VBUS_CTL1

PMU_VBUS_CTL1 Register (RTCVDD) (default 0xE000)
Offset = 0x0D

Bit(s)	Name	Description	Access	Reset
15	VBUS_OC_EN	VBUS overcurrent detection enable 0:disable 1:enable	RW	1
14	VBUS_OV_EN	VBUS overvoltage detection enable 0:disable 1:enable	RW	1
13	VBUS_UV_EN	VBUS undervoltage detection enable 0:disable 1:enable	RW	1
12	VBUS_OC_INT_EN	VBUS overcurrent interrupt enable 0:disable 1:enable	RW	0
11	VBUS_OV_INT_EN	VBUS overvoltage interrupt enable 0:disable 1:enable	RW	0
10	VBUS_UV_INT_EN	VBUS undervoltage interrupt enable 0:disable 1:enable	RW	0
9	VBUS_OC_SHUTOFF_EN	VBUS overcurrent shutoff enable 0:disable 1:enable	RW	0
8	VBUS_DETECT_INT_EN	VBUS plug interrupt enable 0:disable 1:enable	RW	0
7:0	-	Reserved	-	-

7.4.12 PMU_WALL_CTL0

PMU_WALL_CTL0 Register (RTCVDD) (default 0xE680)
Offset = 0x0E

Bit(s)	Name	Description	Access	Reset
15:14	WALL_UV_VOL	WALL undervoltage interrupt voltage setting	RW	0x3

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		00:3.8V 01:4.0V 10:4.3V 11:4.5V		
13:12	WALL_OV_VOL	WALL overvoltage interrupt voltage setting 00:5.3V 01:5.5V 10:5.6V 11:5.8V	RW	0x2
11:8	WALL_OC_SET	WALL overcurrent interrupt current setting 0000:200mA 0001:300mA 0010:400mA 0011:500mA 0100:600mA 0101:700mA 0110:800mA 0111:900mA 1000:1000mA 1001:1200mA 1010:1400mA 1011:1600mA 1100:1800mA 1101:2000mA 1110:2200mA 1111:2500mA The current under detection is flowing from WALL to SYSPWR, through the diode, the overcurrent signal debounce time is 1ms	RW	0x6
7:6	WALL_OC_SHUTOFF_SET	WALL overcurrent shutoff current setting 00:1000mA 01:2000mA 10:2500mA 11:3000mA Overcurrent signal debounce time is 1ms	RW	10
5:0	-	Reserved	-	-

7.4.13 PMU_WALL_CTL1

PMU_WALL_CTL1 Register (RTCVDD) (default 0xE000)
Offset = 0x0F

Bit(s)	Name	Description	Access	Reset
15	WALL_OC_EN	WALL overcurrent detection enable	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:disable 1:enable		
14	WALL_OV_EN	WALL overvoltage detection enable 0:disable 1:enable	RW	1
13	WALL_UV_EN	WALL undervoltage detection enable 0:disable 1:enable	RW	1
12	WALL_OC_INT_EN	WALL overcurrent interrupt enable 0:disable 1:enable	RW	0
11	WALL_OV_INT_EN	WALL overvoltage interrupt enable 0:disable 1:enable	RW	0
10	WALL_UV_INT_EN	WALL undervoltage interrupt enable 0:disable 1:enable	RW	0
9	WALL_OC_SHUTOFF_EN	WALL overcurrent shutoff enable 0:disable 1:enable	RW	0
8	WALL_DETECT_INT_EN	WALL plug interrupt enable 0:disable 1:enable	RW	0
7:0	-	Reserved	-	-

7.4.14 PMU_SYS_PENDING

PMU_SYS_PENDING Register (RTCVDD) (default 0x0000)
Offset = 0x10

Bit(s)	Name	Description	Access	Reset
15	BAT_OV_STATUS	BAT overvoltage state flag 0:BAT is not overvoltage 1:BAT is overvoltage	R	0
14	BAT_UV_STATUS	BAT undervoltage state flag 0:BAT is not undervoltage 1:BAT is undervoltage	R	0
13	BAT_OC_STATUS	BAT overcurrent state flag 0:BAT is not overcurrent 1:BAT is overcurrent	R	0
12	VBUS_OV_STATUS	VBUS overvoltage state flag 0:BAT is not overvoltage 1:BAT is overvoltage	R	0
11	VBUS_UV_STATUS	VBUS undervoltage state flag	R	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:BAT is not undervoltage 1:BAT is undervoltage		
10	VBUS_OC_STATUS	VBUS overcurrent state flag 0:BAT is not overcurrent 1:BAT is overcurrent	R	0
9	WALL_OV_STATUS	WALL overvoltage state flag 0:BAT is not overvoltage 1:BAT is overvoltage	R	0
8	WALL_UV_STATUS	WALL undervoltage state flag 0:BAT is not undervoltage 1:BAT is undervoltage	R	0
7	WALL_OC_STATUS	WALL overcurrent state flag 0:BAT is not overcurrent 1:BAT is overcurrent	R	0
6	VBUS_IN_PD	VBUS plug in pending 0:VBUS is not plugged in 1: VBUS is plugged in	R	0
5	VBUS_OUT_PD	VBUS pull out pending 0:VBUS is not pulled out 1: VBUS is pulled out	R	0
4	WALL_IN_PD	WALL is plugged in pending 0:WALL is not plugged in 1: WALL is plugged in	R	0
3	WALL_OUT_PD	WALL pull out pending 0:WALL is not pulled out 1: VBUS is pulled out	R	0
2:1	-	Reserved	-	-
0	STATUS_CLEAR1	Status flag clear bit Writing 1 to this bit will clear PMU_SYS_PENDING[15:3], then this bit will turn to 0 automatically	RW	0

7.4.15 PMU_APDS_CTL0

PMU_APDS_CTL0 Register (RTCVDD) (default 0x15F8)
Offset = 0x11

Bit(s)	Name	Description	Access	Reset
15	VBUS_CONTROL_EN	VBUS voltage and current control 1:Enable 0:Disable When this bit is enabled, the system will automatically adjust the current extracted from VBUS, and according to the value of	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		bit 14, the system will ensure VBUS voltage is higher than the threshold set by bit[11:10] **or** the current extracted from VBUS is lower than bit[13:12] setting. When this bit is disabled ,the power system's current is in prior. If this bit is enabled, bit8 is invalid.		
14	VBUS_CONTROL_SEL	VBUS control mode selection 0: Voltage-limiting 1: Current-limiting	RW	0
13:12	VBUS_CUR_LIMITED	VBUS current-limiting threshold current 00:100mA 01:300mA 10:500mA 11:800mA	RW	1
11:10	VBUS_VOL_LIMITED	VBUS voltage-limiting threshold voltage 00:4.2V 01:4.3V 10:4.4V 11:4.5V	RW	1
9	VBUS_OTG	If VBUS supplies power for external devices, VBUS_OTG should be set to 1, to avoid VBUS supplies power for SYSPWR. 0:Do not close the diode from VBUS to SYSPWR 1:Close the diode from VBUS to SYSPWR, the path between VBUS and SYSPWR is cutoff completely	RW	0
8	VBUS_FST_ON	When SYSPWR is lower than settings, if VBUS is enough high, VBUS will be opened rapidly 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	1
7	VBUS_FST_OFF	When SYSPWR is higher than settings, VBUS will be shut off rapidly 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	1
6	WALL_FST_ON	When SYSPWR is lower than setting, if WALL is high enough, WALL will be opened rapidly	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:disable 1:enable *Note: this bit is strongly suggested to enable.*		
5	WALL_FST_OFF	If SYSPWR is higher than settings, WALL will be shut off rapidly. 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	1
4	BAT_FST_ON	When SYSPWR is lower than settings, if BAT voltage is high enough, BAT will be opened rapidly 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	1
3	BAT_FST_OFF	If SYSPWR is higher than settings, BAT will be off rapidly 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	1
2	VBUS_PD	VBUS 5KOhm pull down resistor enable 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	0
1	WALL_PD	WALL 5KOhm pull down resistor enable 0:disable 1:enable *Note: this bit is strongly suggested to enable.*	RW	0
0	WALL_ID_EN	Diode between WALL and SYSPWR enable 0:Enable 1:Disable (the path between WALL and SYSPWR is shut off completely)	RW	0

7.4.16 PMU_APDS_CTL1

PMU_APDS_CTL1 Register (RTCVDD) (default 0x176A)
Offset = 0x12

Bit(s)	Name	Description	Access	Reset

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

15	WALL_CONTROL_EN	WALL voltage and current control 1:Enable 0:Disable When this bit is enabled, the system will automatically adjust the current extracted from WALL, and according to the value of bit 14, the system will ensure WALL voltage is higher than the threshold set by bit[11:10] **or** the current extracted from WALL is lower than bit[13:12] setting. When this bit is disabled , the power system's current is in prior. If this bit is enabled, bit6 is invalid.	RW	0
14	WALL_CONTROL_SEL	WALL control mode selection 0:Voltage-limiting 1:Current-limiting	RW	0
13:12	WALL_CUR_LIMITED	WALL current-limiting threshold 00:500mA 01:1500mA 10:2000mA 11:3000mA	RW	1
11:10	WALL_VOL_LIMITED	WALL voltage-limiting threshold 00:4.2V 01:4.3V 10:4.4V 11:4.5V	RW	1
9	VBUS_OVP_EN	VBUS overvoltage protection, if VBUS exceeds the threshold set by bit[8:7] for more than 1μs, VBUS power path will be shutoff; When it falls below the protection value for more than 100μs, VBUS power path will be opened. 0:disable 1:enable	RW	1
8:7	VBUS_OVP_SET	VBUS overvoltage protection voltage threshold setting 00:7.0V 01:7.5V 10:8.0V 11:8.5V	RW	0x2
6	WALL_OVP_EN	WALL overvoltage protection, if WALL exceeds the threshold set by	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		bit[8:7] for more than 1μs, WALL power path will be shutoff;When it falls below the protection value for more than 100μs, WALL power path will be opened 0:disable 1:enable		
5:4	WALL_OVP_SET	WALL overvoltage protection voltage threshold setting 00:7.0V 01:7.5V 10:8.0V 11:8.5V	RW	0x2
3:0	-	Reserved	-	-

7.4.17 PMU_APDS_CTL2

PMU_APDS_CTL2 Register (RTCVDD) (default 0x0055)
Offset = 0x13

Bit(s)	Name	Description	Access	Reset
15	VBUS_STD_INDICATE	VBUS overcurrent or overvoltage state indication 1:VBUS power path is in overcurrent or overvoltage state 0:VBUS power path is not in overcurrent or overvoltage state	R	x
14	WALL_STD_INDICATE	overcurrent or overvoltage state indication 1:WALL power path is in overcurrent or overvoltage state 0:WALL power path is not in overcurrent or overvoltage state	R	x
13:0	-	Reserved	-	-

7.4.18 PMU_CHARGER_CTL

PMU_CHARGER_CTL Register (RTCVDD) (default 0x0000)
Offset = 0x14

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14:13	TEMPTH1	IC temperature threshold1 protection during charging	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		00:65°C 01:75°C 10:85°C 11:95°C		
12:11	TEMPTH2	IC temperature threshold2 protection during charging 00:75°C 01:85°C 10:95°C 11:105°C	RW	0
10:9	TEMPTH3	IC temperature threshold3 protection during charging 00:85°C 01:95°C 10:105°C 11:115°C	RW	0
8:0	-	Reserved	-	-

7.4.19 PMU_SWCHG_CTL0

PMU_SWCHG_CTL0 Register (RTCVDD) (default 0x401A)
Offset = 0x16

Bit(s)	Name	Description	Access	Reset
15	SWCHGEN	Enable Charge Circuit 0:disable 1:enable	RW	0
14	ENTKLE	Enable Trickle Charge 0:disable 1:enable	RW	1
13	CHGISTK	Charger trickle charging current configuration 0:100mA 1:200mA	RW	0
12	RSENSEL	Select external resistor of battery charging current sampling 0:20mOhm 1:10mOhm	RW	0
11:8	CHGIS	Charger constant current charging current configuration 0000:100mA 0001:200mA 0010:400mA 0011:600mA 0100:800mA	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0101:1000mA 0110:1200mA 0111:1400mA 1000:1600mA 1001:1800mA 1010:2000mA 1011:2200mA 1100:2400mA 1101:2600mA 1110:2800mA 1111:3000mA The values above is for switch charging threshold, for linear charging, values are half of the values above.		
7	ENCHGTIME	Charger stopping timer enable bit 0:disable 1:enable	RW	0
6:5	TKLT	Trickle Timer 00:30min 01:40min 10:50min 11:60min	RW	0
4:3	CHGT	CC/CV Charger Timer 00:4hour 01:6hour 10:8hour 11:12hour	RW	0x3
2	ENCHGFCOFF	When bit1 and this bit are enabled at the same time, the battery voltage will be detected every bit0 period, if its value exceeds 4.24V, the charging process will be terminated. 0:disable 1:enable	RW	0
1	ENCHGATDT	Auto detection charging termination 0:disable 1:enable	RW	1
0	DTSEL	Detecting charging termination Time cycle config 1:every 20s 0:every 3min	RW	0

7.4.20 PMU_SWCHG_CTL1

PMU_SWCHG_CTL1 Register (RTCVDD) (default 0x202A)
Offset = 0x17

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15</td><td>ENBATDT</td><td>Battery detection
0:disable
1:enable</td><td>RW</td><td>0</td></tr>
<tr><td>14</td><td>ENATDIS</td><td>When CHGPWROK=0, charger auto cutoff enable
0:disable
1:enable</td><td>RW</td><td>0</td></tr>
<tr><td>13</td><td>ENCURRISE</td><td>Charging current auto increase or decrease enable
0:disable
1:enable</td><td>RW</td><td>1</td></tr>
<tr><td>12:11</td><td>CURRISET</td><td>Time step of increasing/decreasing current in Constant Current charging
00:0.5s
01:1s
10:2s
11:4s</td><td>RW</td><td>0</td></tr>
<tr><td>10</td><td>CV_SET_L</td><td>Constant Voltage charging, voltage setting (set by this bit together with bit8)
<table>
<tr><th>Bit8</th><th>Bit10</th><th>CV_SET</th><th>Note</th></tr>
<tr><td>0</td><td>0</td><td>4.20V</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>4.25V</td><td>In linear/switch charging, the voltage set is 4.30V/4.25V</td></tr>
<tr><td>1</td><td>0</td><td>4.35V</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>4.40V</td><td>-</td></tr>
</table>
If the constant voltage is set to 4.2V, when the battery voltage is near 4.2V, the charging current will decrease, charging time will extend.
In order to decrease the charging time, the battery constant voltage is set to 4.3V, this will accelerate the charging time</td><td>RW</td><td>0</td></tr>
<tr><td>9</td><td>STOPV</td><td>Charging terminate voltage setting
<table>
<tr><th>Bit8</th><th>Bit9</th><th>STOP Voltage</th></tr>
<tr><td>0</td><td>0</td><td>4.16V</td></tr>
<tr><td>0</td><td>1</td><td>4.18V</td></tr>
<tr><td>1</td><td>0</td><td>4.31V</td></tr>
<tr><td>1</td><td>1</td><td>4.33V</td></tr>
</table>
In charging, if the battery voltage is higher than the STOPV value, then the charging process will be hardware stopped every 3min and delay 1s to detect the battery voltage, if the voltage is higher than or equals STOPV, then CHGEND will be set to 1</td><td>RW</td><td>0</td></tr>
<tr><td>8</td><td>CV_SET_H</td><td>Constant charging voltage setting (set by this bit and bit10)</td><td>RW</td><td>0</td></tr>
</table>

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		<table><tr><th>Bit8</th><th>Bit10</th><th>STOP Voltage</th><th>Note</th></tr><tr><td>0</td><td>0</td><td>4.20V</td><td></td></tr><tr><td>0</td><td>1</td><td>4.25V</td><td>In liner/switch charging, the voltage set is 4.30V/4.25V</td></tr><tr><td>1</td><td>0</td><td>4.35V</td><td></td></tr><tr><td>1</td><td>1</td><td>4.40V</td><td></td></tr></table>		
7:6	CHGPWRSET	The voltage difference larger SYSPWR than BAT, if actual difference is less than that, begin to stop charging. 00:0.060V 01:0.160V 10:0.264V 11:0.373V	RW	0
5	ENSAMP	If SYSPWR is not more bit[7:6] than BAT, the charing current will be decreased in Constant Voltage charing phase. 0:disable 1:enable	RW	1
4	ENCHGTEMP	Automatically adjust the charging current in accordance with the variation of temperature 0:Disable 1:Enable	RW	0
3:2	SYSSTEADYSET	Set SYSPWR steady voltage 11: higher 10: high 01: low 00: lower	RW	0x2
1	ENSYN	Enable SYN regulation detect 0: disable 1: enable	RW	1
0	-	Reserved	-	-

7.4.21 PMU_SWCHG_CTL2

PMU_SWCHG_CTL2 Register (RTCVDD) (default 0x0005)
Offset = 0x18

Bit(s)	Name	Description	Access	Reset
15:13	FSL[2:0]	OSC frequency setting (kHz) 000:547 001:600 010:670 011:724	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		100:980 101:1200 110:1340 111:1450		
12	TMEN2	Input offset of OP2 in Constant Current loop adjust enable 0:Disable 1:Enable	RW	0
11	OSRW2	Adjusting mode of input offset OP2 in Constant Current loop 0: automatically 1: manually	RW	0
10	TMEN	Input offset of OP in Constant Current loop adjust enable 0:Disable 1:Enable	RW	0
9	-	Reserved	-	-
8	OSRW	Adjusting mode of input offset OP in Constant Current loop 0: automatically 1: manually	RW	0
7	OSTIME	Setting the adjusting time of OP input offset in Constant Current loop 0: trim once at power on only 1:trim once every 10min	RW	0
6:5	-	Reserved	-	-
4	EN_OCP	Charging overcurrent protection enable 0:Disable 1:Enable	RW	0
3	ILIMIT	Setting the current limit 0:2.5A 1:3.47A	RW	0
2:0	-	Reserved	-	-

7.4.22 PMU_SWCHG_CTL3

PMU_SWCHG_CTL3 Register (RTCVDD) (default 0x4AAA)
Offset = 0x19

Bit(s)	Name	Description	Access	Reset
15	MODSEL	Setting DC-DC charger working modes 0:linear charging mode 1:switch charging mode	RW	0
14	-	Reserved	-	-

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

13:7	TRIMSET2	OP2 trim code manually set 0000000: more positive …… 1111111: more negative	RW	0x55
6:0	TRIMSET	OP trim code manually set 0000000: more positive …… 1111111: more negative	RW	0x2A

7.4.23 PMU_SWCHG_CTL4

PMU_SWCHG_CTL4 Register (RTCVDD) (default 0x0000)
Offset = 0x1A

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14	CHGPWR_RTC	Flag bit of power voltage relative to BAT 0:SYSPWR<BAT+ΔV 1:SYSPWR>BAT+ΔV	R	x
13	CHGOV001_RTCD	Flag bit of Ichg (charging current) 0: Ichg<1%Ichg_reg 1: Ichg>1%Ichg_reg	R	x
12:11	CHGPHASE<1 :0>	Charging state flag 00: reserved 01: trickle charging phase 10: CC charging phase 11: CV charging phase	R	x
10	CHGEND	Charging finished flag 0:on charging 1:charging finished	R	x
9	CHGTIMEEND	Charging time finished flag 0:CC/CV Timer/Trickle timer doesn’t count up 1:CC/CV Timer/Trickle timer counts up	R	x
8	BATEXT	BAT existance flag 0:no BAT 1:BAT	R	x
7	DTOVER	Battery detection finished flag 0:under detection 1:detection finished	R	x
6:0	OSTRIMOUT	Revised result of OP in CC loop	R	x

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.24 PMU_DC_OSC

PMU_DC_OSC Register (RTCVDD) (default 0xAA0C)
Offset = 0x1b

Bit(s)	Name	Description	Access	Reset
15:9	-	Reserved	-	-
8	EN_DC4L	DC4 Enable (bit0 will be cleared to 0 when entering S3A/S3/S4) 1:enable 0:disable	RW	0
7	EN_DC3L	DC3 Enable (bit0 will be cleared to 0 when entering S3A/S3/S4) 1:enable 0:disable	RW	0
6	EN_DC2L	DC2 Enable (bit0 will be cleared to 0 when entering S3A/S3/S4) 1:enable 0:disable	RW	0
5	EN_DC1L	DC1 Enable (bit0 will be cleared to 0 when entering S3A/S3/S4) 1:enable 0:disable	RW	0
4	EN_DC0L	DC0 Enable (bit0 will be cleared to 0 when entering S3A/S3/S4) 1:enable 0:disable	RW	0
3	RG_OSC_DEL	OSC delay selection 1: DC-DC PMOS turn on time interval 150ns 0: DC-DC PMOS turn on time interval 5ns	RW	1
2:0	FSL	OSC frequency adjust 000~010: smaller 011:2.0MHz 100~111:bigger	RW	0x4

7.4.25 PMU_DC0_CTL0

PMU_DC0_CTL0 Register (RTCVDD) (default 0x4000)
Offset = 0x1C

Bit(s)	Name	Description	Access	Reset
15:8	DC_VOL	DC0 Voltage setting (TRES) Code: 0000,000~1111,111 / Voltage(V): 0.6~2.19375 / Step(mV): 6.25	RW	0x40

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		Four important voltage settings: 1100,0000:1.8V 1001,0000:1.5V 0110,0000:1.2V 0100,0000:1.0V		
7:0	-	Reserved	-	-

7.4.26 PMU_DC1_CTL0

PMU_DC1_CTL0 Register (RTCVDD) (default 0x4000)

Offset = 0x23

Bit(s)	Name	Description	Access	Reset
15:8	DC_VOL	DC1 Voltage setting (TRES) **Code** | **Voltage** | **Step** 0000'0000~1111'1111 | 0.6~2.19375 | 6.25mV Four important voltage settings: 1.8V:1100,0000 1.5V:1001,0000 1.2V: 0110,0000 1.0V: 0100,0000	RW	0x40
7:0	-	Reserved	-	-

7.4.27 PMU_DC2_CTL0

PMU_DC2_CTL0 Register (RTCVDD) (default 0x4000)

Offset = 0x2A

Bit(s)	Name	Description	Access	Reset
15:8	DC_VOL	DC2 Voltage setting (TRES) **Code** | **Voltage** | **Step** 0000'0000~1111'1111 | 0.6~2.19375 | 6.25mV Four important voltage settings: 1100,0000:1.8V 1001,0000:1.5V 0110,0000:1.2V 0100,0000:1.0V	RW	0x40
7:0	-	Reserved	-	-

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.28 PMU_DC3_CTL0

PMU_DC3_CTL0 Register (RTCVDD) (default 0x4000)
Offset = 0x31

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15:8</td><td>DC_VOL</td><td>DC3 Voltage setting (TRES)<table><tr><th>Code</th><th>Voltage</th><th>Step</th></tr><tr><td>0000’0000~0111’1111</td><td>0.6~1.39375</td><td>6.25mV</td></tr><tr><td>1000’0000~1110’1000</td><td>1.4~4.0</td><td>25mV</td></tr></table>Four important voltage settings:
3.1V:1100,0100
1.8V:1001,0000
1.5V:1000,0100
1.2V: 0110,0000
1.0V: 0100,0000</td><td>RW</td><td>0x40</td></tr>
<tr><td>7:0</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table>

7.4.29 PMU_DC4_CTL0

PMU_DC4_CTL0 Register (RTCVDD) (default 0x4000)
Offset = 0x79

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15:8</td><td>DC_VOL</td><td>DC4 Voltage setting (TRES)<table><tr><th>Code</th><th>Voltage</th><th>Step</th></tr><tr><td>0000’0000~1111’1111</td><td>0.6~2.19375</td><td>6.25mV</td></tr></table>1100,0000:1.8V
1001,0000:1.5V
0110,0000:1.2V
0100,0000:1.0V</td><td>RW</td><td>0x40</td></tr>
<tr><td>7:0</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table>

7.4.30 PMU_DC_ZR

PMU_DC_ZR Register (RTCVDD) (default 0x0000)
Offset = 0x38

Bit(s)	Name	Description	Access	Reset
15:12	ZR3	Auto zero-crossing calibration state	R	0
11:8	ZR2	Auto zero-crossing calibration state	R	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7:4	ZR1	Auto zero-crossing calibration state	R	0
3:0	ZR0	Auto zero-crossing calibration state	R	0

7.4.31 PMU_LDO0_CTL0

PMU_LDO0_CTL0 Register (RTCVDD) (default 0x00A0)
Offset = 0x39

Bit(s)	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:2	LDO0_VOL	Others: 3.4V 1011: 3.4V 1010: 3.3V 1001: 3.2V 1000: 3.1V 0111: 3.0V 0110: 2.9V 0101: 2.8V 0100: 2.7V 0011: 2.6V 0010: 2.5V 0001: 2.4V 0000: 2.3V	RW	0x8
1	LDO0_SW_EN	LDO0 switch function Enable (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable *Note: in order to realize the switch function, the LDO0 enable bit must be disabled.* *When the system enters Standby mode, the power needed to be shut down, at the time LDO function is disabled, the switch function should be disabled, too*	RW	0
0	LDO0_EN	LDO0 enable control (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable	RW	0

7.4.32 PMU_LDO1_CTL0

PMU_LDO1_CTL0 Register (RTCVDD) (default 0x00A0)

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Offset = 0x3B

Bit(s)	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:2	LDO1_VOL	Other: 3.4V 1011: 3.4V 1010: 3.3V 1001: 3.2V 1000: 3.1V 0111: 3.0V 0110: 2.9V 0101: 2.8V 0100: 2.7V 0011: 2.6V 0010: 2.5V 0001: 2.4V 0000: 2.3V	RW	0x8
1	LDO1_SW_EN	LDO1 switch function enable: (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable *Note: in order to realize the switch function, the LDO1 enable bit must be disabled.* *When the system enters Standby mode, the power needed to be shut down, at the time LDO function is disabled, the switch function should be disabled, too*	RW	0
0	LDO1_EN	LDO1 enable control (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable	RW	0

7.4.33 PMU_LDO2_CTL0

PMU_LDO2_CTL Register (RTCVDD) (default 0x00A0)
Offset = 0x3D

Bit(s)	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:2	LDO2_VOL	Others: 3.4V 1011: 3.4V 1010: 3.3V 1001: 3.2V	RW	0x8

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1000: 3.1V 0111: 3.0V 0110: 2.9V 0101: 2.8V 0100: 2.7V 0011: 2.6V 0010: 2.5V 0001: 2.4V 0000: 2.3V		
1	LDO2_SW_EN	LDO2 switch function Enable (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable *Note: in order to realize the switch function, the LDO2 enable bit must be disabled.* *When the system enters Standby mode, the power needed to be shut down, at the time LDO function is disabled, the switch function should be disabled, too*	RW	0
0	LDO2_EN	LDO2 Enable control (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable	RW	0

7.4.34 PMU_LDO3_CTL0

PMU_LDO3_CTL0 Register (RTCVDD) (default 0x0096)
Offset = 0x3F

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>LDO3_VOL_SEL</td><td>Choosing LDO output voltage range
1 : 2.1V~3.3V
0 : 0.7V~2.2V
When switching this bit, LDO voltage will fall down for a while, the LDO should not be switched in normal working mode.</td><td>RW</td><td>0</td></tr>
<tr><td>4:1</td><td>LDO3_VOL</td><td><table><tr><th>LDO3_VOL</th><th>bit[5]=0</th><th>bit[5]=1</th></tr><tr><td>1111</td><td>2.2V</td><td>3.3V</td></tr><tr><td>1110</td><td>2.1V</td><td>3.3V</td></tr><tr><td>1101</td><td>2.0V</td><td>3.3V</td></tr></table></td><td>RW</td><td>0xB</td></tr>
</table>

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1100 1.9V 3.3V 1011 1.8V 3.2V 1010 1.7V 3.1V 1001 1.6V 3.0V 1000 1.5V 2.9V 0111 1.4V 2.8V 0110 1.3V 2.7V 0101 1.2V 2.6V 0100 1.1V 2.5V 0011 1.0V 2.4V 0010 0.9V 2.3V 0001 0.8V 2.2V 0000 0.7V 2.1V		
0	LDO3_EN	LDO3 Enable control (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable	RW	0

7.4.35 PMU_LDO4_CTL0

PMU_LDO4_CTL0 Register (RTCVDD) (default 0x0096)
Offset = 0x41

Bit(s)	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5	LDO4_VOL_SEL	LDO output voltage range selection 1: 2.1V~3.3V 0: 0.7V~2.2V When the range is switched, LDO voltage will fall down for a short while. When LDO is turned on, the voltage range should not be switched in normal working mode.	RW	0
4:1	LDO4_VOL	**LDO4_VOL bit[5]=0 bit[5]=1** 1111 2.2V 3.3V 1110 2.1V 3.3V 1101 2.0V 3.3V 1100 1.9V 3.3V 1011 1.8V 3.2V 1010 1.7V 3.1V 1001 1.6V 3.0V 1000 1.5V 2.9V	RW	0xB

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0111	1.4V	2.8V		
		0110	1.3V	2.7V		
		0101	1.2V	2.6V		
		0100	1.1V	2.5V		
		0011	1.0V	2.4V		
		0010	0.9V	2.3V		
		0001	0.8V	2.2V		
		0000	0.7V	2.1V		
0	LDO4_EN	LDO4 enable control (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable			RW	0

7.4.36 PMU_LDO6_CTL0

PMU_LDO6_CTL0 Register (RTCVDD) (default 0x0086)
Offset = 0x45

Bit(s)	Name	Description			Access	Reset
15:6	-	Reserved			-	-
5	LDO6_VOL_SEL	LDO output voltage range selection 1 : 2.1V~3.3V 0 : 0.85V~2.2V Switching this bit, LDO voltage will fall down for a short time, when the LDO is switched on and working in normal mode, the voltage range should not be switched.			RW	0
4:1	LDO6_VOL	**LDO6_VOL**	**bit[5]=0**	**bit[5]=1**	RW	0x3
		1111	2.20V	3.2V		
		1110	1.25V	3.2V		
		1101	1.20V	3.2V		
		1100	1.15V	3.2V		
		1011	1.10V	3.2V		
		1010	1.05V	3.1V		
		1001	1.05V	3.0V		
		1000	1.05V	2.9V		
		0111	1.05V	2.8V		
		0110	1.05V	2.7V		
		0101	1.05V	2.6V		
		0100	1.05V	2.5V		
		0011	1.00V	2.4V		
		0010	0.95V	2.3V		

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0001	0.90V	2.2V		
		0000	0.85V	2.1V		
0	LDO6_EN	LDO6 enable control: (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable			RW	0

7.4.37 PMU_LDO7_CTL0

PMU_LDO7_CTL0 Register (RTCVDD) (default 0x0096)
Offset = 0x47

Bit(s)	Name	Description			Access	Reset
15:6	-	Reserved			-	-
5	LDO7_VOL_SEL	LDO output voltage range selection 1 : 2.1V~3.3V 0 : 0.7V~2.2V LDO output voltage will fall down for a short while when switching the range, after LDO is turned on and working in normal mode, the voltage range should not be switched.			RW	0
4:1	LDO7_VOL	**LDO7_VOL**	**bit[5]=0**	**bit[5]=1**	RW	0xB
		1111:	2.2V	3.3V		
		1110:	2.1V	3.3V		
		1101:	2.0V	3.3V		
		1100:	1.9V	3.3V		
		1011:	1.8V	3.2V		
		1010:	1.7V	3.1V		
		1001:	1.6V	3.0V		
		1000:	1.5V	2.9V		
		0111:	1.4V	2.8V		
		0110:	1.3V	2.7V		
		0101:	1.2V	2.6V		
		0100:	1.1V	2.5V		
		0011:	1.0V	2.4V		
		0010:	0.9V	2.3V		
		0001:	0.8V	2.2V		
		0000:	0.7V	2.1V		
0	LDO7_EN	LDO7 Enable control (FSM will clear bit[0] to 0 when entering S3A/S3/S4) 0:disable 1:enable			RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.38 PMU_LDO8_CTL0

PMU_LDO8_CTL0 Register (RTCVDD) (default 0x0096)
Offset = 0x49

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>LDO8_VOL_SEL</td><td>LDO output voltage range selection
1 : 2.1V~3.3V
0 : 0.7V~2.2V
LDO output voltage will fall down for a short while when switching the range, after LDO is turned on and working in normal mode, the voltage range should not be switched.</td><td>RW</td><td>0</td></tr>
<tr><td>4:1</td><td>LDO8_VOL</td><td><table><tr><th>LDO8_VOL</th><th>bit[5]=0</th><th>bit[5]=1</th></tr><tr><td>1111</td><td>2.2V</td><td>3.3V</td></tr><tr><td>1110</td><td>2.1V</td><td>3.3V</td></tr><tr><td>1101</td><td>2.0V</td><td>3.3V</td></tr><tr><td>1100</td><td>1.9V</td><td>3.3V</td></tr><tr><td>1011</td><td>1.8V</td><td>3.2V</td></tr><tr><td>1010</td><td>1.7V</td><td>3.1V</td></tr><tr><td>1001</td><td>1.6V</td><td>3.0V</td></tr><tr><td>1000</td><td>1.5V</td><td>2.9V</td></tr><tr><td>0111</td><td>1.4V</td><td>2.8V</td></tr><tr><td>0110</td><td>1.3V</td><td>2.7V</td></tr><tr><td>0101</td><td>1.2V</td><td>2.6V</td></tr><tr><td>0100</td><td>1.1V</td><td>2.5V</td></tr><tr><td>0011</td><td>1.0V</td><td>2.4V</td></tr><tr><td>0010</td><td>0.9V</td><td>2.3V</td></tr><tr><td>0001</td><td>0.8V</td><td>2.2V</td></tr><tr><td>0000</td><td>0.7V</td><td>2.1V</td></tr></table></td><td>RW</td><td>0xB</td></tr>
<tr><td>0</td><td>LDO8_EN</td><td>LDO8 enable control
(FSM will clear bit[0] to 0 when entering S3A/S3/S4)
0:disable
1:enable</td><td>RW</td><td>0</td></tr>
</table>

7.4.39 PMU_LDO9_CTL

PMU_LDO9_CTL Register (RTCVDD) (default 0xB000)
Offset = 0x4B

Bit(s)	Name	Description	Access	Reset
15:13	LDO9_VOL	LDO9(SVCC) Voltage setting	RW	0x5

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		000:2.6V 001:2.7V 010:2.8V 011:2.9V 100:3.0V 101:3.1V 110:3.2V 111:3.3V		
12	SVCC_LOW_EN	SVCC low voltage protection enable 0:Disable 1:Enable	RW	1
11:7	-	Reserved	-	-
6:0	OSTRIMOUT2	Constant current loop OP2 calibration result	R	x

7.4.40 PMU_OV_STATUS

PMU_OV_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x4D

Bit(s)	Name	Description	Access	Reset
15	DC-DC0_OV_STATUS	DC-DC0 output overvoltage state flag 0:DC-DC0 output not overvoltage 1:DC-DC0 output overvoltage	R	0
14	DC-DC1_OV_STATUS	DC-DC1 output overvoltage state flag 0:DC-DC1 output not overvoltage 1:DC-DC1 output overvoltage	R	0
13	DC-DC2_OV_STATUS	DC-DC2 output overvoltage state flag 0:DC-DC2 output not overvoltage 1:DC-DC2 output overvoltage	R	0
12	DC-DC3_OV_STATUS	DC-DC3 output overvoltage state flag 0:DC-DC3 output not overvoltage 1:DC-DC3 output overvoltage	R	0
11	LDO0_OV_STATUS	LDO0 output overvoltage state flag 0:LDO0 output not overvoltage 1:LDO0 output overvoltage	R	0
10	LDO1_OV_STATUS	LDO1 output overvoltage state flag 0:LDO1 output not overvoltage 1:LDO1 output overvoltage	R	0
9	LDO2_OV_STATUS	LDO2 output overvoltage state flag 0:LDO2 output not overvoltage 1:LDO2 output overvoltage	R	0
8	LDO3_OV_STATUS	LDO3 output overvoltage state flag 0:LDO3 output not overvoltage	R	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1:LDO3 output overvoltage		
7	LDO4_OV_STATUS	LDO4 output overvoltage state flag 0:LDO4 output not overvoltage 1:LDO4 output overvoltage	R	0
6	-	Reserved	-	-
5	LDO6_OV_STATUS	LDO6 output overvoltage state flag 0:LDO6 output not overvoltage 1:LDO6 output overvoltage	R	0
4	LDO7_OV_STATUS	LDO7 output overvoltage state flag 0:LDO7 output not overvoltage 1:LDO7 output overvoltage	R	0
3	LDO8_OV_STATUS	LDO8 output overvoltage state flag 0:LDO8 output not overvoltage 1:LDO8 output overvoltage	R	0
2	DC-DC4_OV_STATUS	DC-DC4 output overvoltage state flag 0:DC-DC4 output not overvoltage 1:DC-DC4 output overvoltage	R	0
1	-	Reserved	-	-
0	STATUS_CLEAR2	Status indication clear bit When writing 1 to this bit, the bit[15:2] will be cleared, and this bit will turn to 0 automatically	RW	0

7.4.41 PMU_UV_INT_EN

PMU_UV_INT_EN Register (RTCVDD) (default 0xFFFC)

Offset = 0x4E

Bit(s)	Name	Description	Access	Reset
15	DC-DC0_UV_EN	DC-DC0 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
14	DC-DC1_UV_EN	DC-DC1 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
13	DC-DC2_UV_EN	DC-DC2 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
12	DC-DC3_UV_EN	DC-DC3 output undervoltage interrupt enable 0:Disable	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1:Enable		
11	LDO0_UV_EN	LDO0 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
10	LDO1_UV_EN	LDO1 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
9	LDO2_UV_EN	LDO2 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
8	LDO3_UV_EN	LDO3 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
7	LDO4_UV_EN	LDO4 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
6	-	Reserved	-	-
5	LDO6_UV_EN	LDO6 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
4	LDO7_UV_EN	LDO7 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
3	LDO8_UV_EN	LDO8 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
2	DC-DC4_UV_INT_EN	DC-DC4 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
1-0	-	Reserved	-	-

7.4.42 PMU_UV_STATUS

PMU_UV_STATUS Register (RTCVDD) (default 0x0000)

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Offset = 0x4F

Bit(s)	Name	Description	Access	Reset
15	DC-DC0_UV_STATUS	DC-DC0 output undervoltage state flag 0:DC-DC0 output is not undervoltage 1:DC-DC0 output is undervoltage	R	0
14	DC-DC1_UV_STATUS	DC-DC1 output undervoltage state flag 0:DC-DC1 output is not undervoltage 1:DC-DC1 output is undervoltage	R	0
13	DC-DC2_UV_STATUS	DC-DC2 output undervoltage state flag 0:DC-DC2 output is not undervoltage 1:DC-DC2 output is undervoltage	R	0
12	DC-DC3_UV_STATUS	DC-DC3 output undervoltage state flag 0:DC-DC3 output is not undervoltage 1:DC-DC3 output is undervoltage	R	0
11	LDO0_UV_STATUS	LDO0 output undervoltage state flag 0:LDO0 output is not undervoltage 1:LDO0 output is undervoltage	R	0
10	LDO1_UV_STATUS	LDO1 output undervoltage state flag 0:LDO1 output is not undervoltage 1:LDO1 output is undervoltage	R	0
9	LDO2_UV_STATUS	LDO2 output undervoltage state flag 0:LDO2 output is not undervoltage 1:LDO2 output is undervoltage	R	0
8	LDO3_UV_STATUS	LDO3 output undervoltage state flag 0:LDO3 output is not undervoltage 1:LDO3 output is undervoltage	R	0
7	LDO4_UV_STATUS	LDO4 output undervoltage state flag 0:LDO4 output is not undervoltage 1:LDO4 output is undervoltage	R	0
6	-	Reserved	-	-
5	LDO6_UV_STATUS	LDO6 output undervoltage state flag 0:LDO6 output is not undervoltage 1:LDO6 output is undervoltage	R	0
4	LDO7_UV_STATUS	LDO7 output undervoltage state flag 0:LDO7 output is not undervoltage 1:LDO7 output is undervoltage	R	0
3	LDO8_UV_STATUS	LDO8 output undervoltage state flag 0:LDO8 output is not undervoltage 1:LDO8 output is undervoltage	R	0
2	DC-DC4_UV_STATUS	DC-DC4output undervoltage state flag 0:DC-DC4 output is not undervoltage 1:DC-DC4 output is undervoltage	R	0
1	-	Reserved	-	-
0	STATUS_CLEAR4	Status flag clear bit	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		When writing 1 to this bit, the bit[15:2] will be cleared, and this bit will turn to 0 automatically		

7.4.43 PMU_OC_INT_EN

PMU_OC_INT_EN Register (RTCVDD) (default 0x0FF8)
Offset = 0x50

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	LDO0_OC_INT_EN	LDO0 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
10	LDO1_OC_INT_EN	LDO1 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
9	LDO2_OC_INT_EN	LDO2 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
8	LDO3_OC_INT_EN	LDO3 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
7	LDO4_OC_INT_EN	LDO4 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
6	-	Reserved	-	-
5	LDO6_OC_INT_EN	LDO6 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
4	LDO7_OC_INT_EN	LDO7 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
3	LDO8_OC_INT_EN	LDO8 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

2:0	-	Reserved	-	-

7.4.44 PMU_OC_STATUS

PMU_OC_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x51

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	LDO0_OC_STATUS	LDO0 output overcurrent state flag 0:LDO0 output is not overcurrent 1:LDO0 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
10	LDO1_OC_STATUS	LDO1 output overcurrent state flag 0:LDO1 output is not overcurrent 1:LDO1 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
9	LDO2_OC_STATUS	LDO2 output overcurrent state flag 0:LDO2 output is not overcurrent 1:LDO2 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
8	LDO3_OC_STATUS	LDO3 output overcurrent state flag 0:LDO3 output is not overcurrent 1:LDO3 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
7	LDO4_OC_STATUS	LDO4 output overcurrent state flag 0:LDO4 output is not overcurrent 1:LDO4 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
6	-	Reserved	-	-
5	LDO6_OC_STATUS	LDO6 output overcurrent state flag 0:LDO6 output is not overcurrent 1:LDO6 output is overcurrent When LDO is overcurrent, this LDO	R	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		will be HW shutdown, and this bit will turn to 1.		
4	LDO7_OC_STATUS	LDO7 output overcurrent state flag 0:LDO7 output is not overcurrent 1:LDO7 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
3	LDO8_OC_STATUS	LDO8 output overcurrent state flag 0:LDO8 output is not overcurrent 1:LDO8 output is overcurrent When LDO is overcurrent, this LDO will be HW shutdown, and this bit will turn to 1.	R	0
2:1	-	Reserved	-	-
0	STATUS_CLEAR3	Status flag clear bit When writing 1 to this bit, the bit[15:2] will be cleared, and this bit will turn to 0 automatically	RW	0

7.4.45 PMU_OT_CTL

PMU_OT_CTL Register (RTCVDD) (default 0x3300)
Offset = 0x52

Bit(s)	Name	Description	Access	Reset
15	OT_STATUS	IC overtemperature status flag 0:not overtemperature 1: overtemperature Write 1 clear to 0	RW	0
14:13	OT_SET	IC overtemperature temperature interrupt setting 00:60°C 01:70°C 10:80°C 11:90°C	RW	1
12	OT_INT_EN	IC overtemperature interrupt enable 0:disable 1:enable	RW	1
11	OT_SHUTOFF_EN	IC overtemperature shut off enable 0:disable 1:enable	RW	0
10:9	OT_SHUTOFF_SET	IC overtemperature shut off temperature setting	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		00:90°C 01:100°C 10:110°C 11:120°C		
8	OT_EN	IC overtemperature detection enable 0:disable 1:enable	RW	1
7-0	-	Reserved	-	-

7.4.46 PMU_CM_CTL0

PMU_CM_CTL0 Register (RTCVDD) (default 0xF000)
Offset = 0x53

Bit(s)	Name	Description	Access	Reset
15	ENCM	Enable coulomb meter's pre-amplifier 1:enable 0:disable	RW	1
14	ENCHOP	Enable pre-amplifier's primary offset reduction function 1:enable 0:disable	RW	1
13	AUTOGACTL_EN	Enable automatic gain control of the pre-amplifier. 1: gain = automatically selected 0: gain = fixed set	RW	1
12:0	-	Reserved	-	-

7.4.47 PMU_PWR_STATUS

PMU_PWR_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x80

Bit(s)	Name	Description	Access	Reset
15	DC-DC0_PWR_OK	DC-DC0 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
14	DC-DC1_PWR_OK	DC-DC1 power output status indication 0:no output or voltage is lower than normal value at present	R	x

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1:output voltage is OK at present		
13	DC-DC2_PWR_OK	DC-DC2 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
12	DC-DC3_PWR_OK	DC-DC3 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
11	DC-DC4_PWR_OK	DC-DC4 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
10	LDO0_PWR_OK	LDO0 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
9	LDO1_PWR_OK	LDO1 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
8	LDO2_PWR_OK	LDO2 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
7	LDO3_PWR_OK	LDO3 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
6	LDO4_PWR_OK	LDO4 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
5	-	Reserved	-	-
4	LDO6_PWR_OK	LDO6 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
3	LDO7_PWR_OK	LDO7 power output status indication 0:no output or voltage is lower than normal value at present	R	x

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1:output voltage is OK at present		
2	LDO8_PWR_OK	LDO8 power output status indication 0:no output or voltage is lower than normal value at present 1:output voltage is OK at present	R	x
1:0	PWR_ON_SCALING	When entering S1 from Standby, time interval of every power step 00:1ms 01:2ms 10:4ms 11:8ms	RW	0

7.4.48 PMU_S2_PWR

PMU_PWR_STATUS Register (RTCVDD) (default 0x2000)
Offset = 0x81

Bit(s)	Name	Description	Access	Reset
15	S2_DC-DC0_PWR_EN	Whether DC-DC0 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
14	S2_DC-DC1_PWR_EN	Whether DC-DC1 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
13	S2_DC-DC2_PWR_EN	Whether DC-DC2 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	1
12	S2_DC-DC3_PWR_EN	Whether DC-DC3 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
11	S2_DC-DC4_PWR_EN	Whether DC-DC4 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
10	S2_LDO0_PWR_EN	Whether LDO0 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
9	S2_LDO1_PWR_EN	Whether LDO1 is forced to shut down in S2	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0:forced to shutdown 1:remain the power state in S1		
8:7	-	Reserved	-	-
6	S2_LDO4_PWR_EN	Whether LDO4 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
5	-	Reserved	-	-
4	S2_LDO6_PWR_EN	Whether LDO6 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
3	S2_LDO7_PWR_EN	Whether LDO7 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
2	S2_LDO8_PWR_EN	Whether LDO8 is forced to shut down in S2 0:forced to shutdown 1:remain the power state in S1	RW	0
1	-	Reserved	-	-
0	PWR_OFF_SCH	0:power supplies power off at the same time 1:power supplies power off according to a reversed sequence of power on	RW	0

7.4.49 CLMT_CTL0

CLMT_CTL0 Register (RTCVDD) (default 0x8001)
Offset = 0x82

Bit(s)	Name	Description	Access	Reset
15:14	TIMER	Setting the time of Qmax should stay in Standby mode before being updated 00: 1h 01: 3h 10: 5h 11: 7h	RW	0x2
13:2	U_STOP	Lowest battery voltage for system operation	RW	0
1	INIT_DATA_EN	Coulombmeter system information initialization enable 1:Enable (info is initialized) 0:Disable (indicating the info is not initialized) When the software is powered up, value of this bit	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		should be read first, if it is 0, before setting this bit to 1, CLMT_CTL[13:2], CLMT_DATA0, CLMT_OCV_TABLE, CLMT_R_TABLE should be set first, then 1sec later, the output of Coulombmeter becomes valid		
0	CLMT_EN	Coulombmeter 1:Enable 0:Disable	RW	1

7.4.50 CLMT_DATA0

CLMT_DATA0 Register (RTCVDD) (default 0x0000)
Offset = 0x83

Bit(s)	Name	Description	Access	Reset
15:0	Q_MAX	Total amount of Li-Ion battery	RW	0

7.4.51 CLMT_DATA1

CLMT_DATA1 Register (RTCVDD) (default 0x0000)
Offset = 0x84

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14:8	SOCR	Actual battery power remained in percentage (percentage step:1%) 0000000: 0% … 1100100: 100% 1100101: Reserved … 1111111: Reserved	R	0
7	-	Reserved	-	-
6:0	SOCA	Usable battery power remained in percentage (percentage step:1%) 0000000: 0% … 1100100: 100% 1100101: Reserved … 1111111: Reserved	R	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

7.4.52 CLMT_DATA2

CLMT_DATA2 Register (RTCVDD) (default 0x0000)
Offset = 0x85

Bit(s)	Name	Description	Access	Reset
15:0	QR	Actual battery power remained	R	0

7.4.53 CLMT_DATA3

CLMT_DATA3 Register (RTCVDD) (default 0x0000)
Offset = 0x86

Bit(s)	Name	Description	Access	Reset
15:0	QA	Usable battery power remained	R	0

7.4.54 PMU_ADC12B_I

PMU_ADC12B_I Register (RTCVDD) (default 0x0000)
Offset = 0x56

Bit(s)	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13:0	DATA_ICM	Value of CM detection current	R	x

7.4.55 PMU_ADC12B_V

PMU_ADC12B_V Register (RTCVDD) (default 0x0000)
Offset = 0x57

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	DATA_VCM	Value of CM detection voltage	R	x

7.4.56 CLMT_OCV_TABLE

CLMT_OCV_TABLE Register (RTCVDD) (default 0x0000)
Offset = 0x89

Bit(s)	Name	Description	Access	Reset
15:12	OCV_SEL	Setting up the OCV&SOC contrast table Select the electricity quantity percentage SOC, then writing bit[11:0] in SOC of the relative voltage OF OCV	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0000: 0% 0001: 4% 0010: 8% 0011: 12% 0100: 16% 0101: 20% 0110: 28% 0111: 36% 1000: 44% 1001: 52% 1010: 60% 1011: 68% 1100: 76% 1101: 84% 1110: 92% 1111: 100%		
11:0	OCV_N	The electricity quantity is n% (n is decided by bit[15:12]), the relative OCV battery voltage(mV) *Note: 0000000000 is invalid, can't be written in to registers*	RW	0

7.4.57 CLMT_R_TABLE

CLMT_R_TABLE Register (RTCVDD) (default 0x0000)
Offset = 0x8A

Bit(s)	Name	Description	Access	Reset
15:12	R_SEL	Setting up the battery inner resister R&SOC contrast table: Choose the electricity quantity percentage SOC, then writing the SOC relative battery inner resister into bit[10:0] 0000: 0% 0001: 4% 0010: 8% 0011: 12% 0100: 16% 0101: 20% 0110: 28% 0111: 36% 1000: 44% 1001: 52% 1010: 60% 1011: 68%	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1100: 76% 1101: 84% 1110: 92% 1111: 100%		
11	-	Reserved	-	-
10:0	R_N	The electricity quantity is n% (n is decided by bit[15:12]), the relative inner battery resistor(mOhm) *Note: 0000000000 is invalid, can't be written in to registers*	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

8 Auxiliary ADC

8.1 Module Description

ATC2609 integrates a 12-bit, 16-channel Analog-to-Digital Converter (ADC), which converts one of the 16 analog inputs to 12-bit digital data, the application of each bit is listed below:

Table 8-1 AUXADC functional specifications

ADC_0	**ADC_1**	**ADC_2**	**ADC_3**	**ADC_4**	**ADC_5**	**ADC_6**	**ADC_7**
IREF	ICHG	VBUS	WALLI	BATI	REM_CON	ICTEMP	SVCC
ADC_8	**ADC_9**	**ADC_10**	**ADC_11**	**ADC_12**	**ADC_13**	**ADC_14**	**ADC_15**
Reserved	SYSPWRV	WALLV	VBUSV	Reserved	Reserved	AUXADC1	AUXADC0

WALL, SYSPWR and VBUS will pass a 2.5 voltage divider before sent to ADC, so the formula for WALL, SYSPWR, VBUS voltage (V) that relates their ADC output (DATA) can be described by:

$$V = DATA * LSB * 2.5$$

While BAT will pass a 2 voltage divider before sent to ADC, so the relationship between BAT voltage and its ADC output is:

$$V = DATA * LSB * 2$$

In addition, ADC also detects the current from VBUS to SYSPWR, current from BAT to SYSPWR, charger's charging current, SVCC voltage, battery temperature and etc. The full current range of BATI, WALLI, ICHG and VBUSI ADCs are all 4000mA, thus the current can be expressed as follows, where DATA is the ADC digital output:

$$I = DATA * LSBI = DATA * 4000 / 4096(mA)$$

ICTEM ADC value is sensitive to manufacturing process, the deviation value will be written into PMU_AUXADC_CTL1 register by software, and then software can get the calibrated temperature data ICTEMPADC_ADJ from the register PMU_ICTEMPADC . The relationship between IC Temperature (TEMP) and ICTEMP's ADC data can be expressed as follows:

$$TEMP = 0.051 * (DATA + \mathrm{ICTEMPADC\_ADJ} - 1333)(^{\circ}C)$$

For the REM_CON, the voltage of each button can be calculated as follow:

$$Vrem\_con = (DATA / 4096) * SVCC$$

Where DATA is from the register PMU_REMCONADC.

AUXADC0~1 are for general use.

8.2 Register List

Table 8-2 AUXADC Block Address

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Name	Base Address
AUXADC	0x0000

Table 8-3 AUXADC Controller Registers

Offset	Register Name	Description
0x59	PMU_AUXADC_CTL0	PMU AuxADC CONTROL Register0
0x5A	PMU_AUXADC_CTL1	PMU AuxADC CONTROL Register1
0x5B	PMU_BATVADC	PMU BATVADC Register
0x5C	PMU_BATIADC	PMU BATIADC Register
0x5D	PMU_WALLVADC	PMU WALLVADC Register
0x5E	PMU_WALLIADC	PMU WALLIADC Register
0x5F	PMU_VBUSVADC	PMU VBUSVADC Register
0x60	PMU_VBUSIADC	PMU VBUSIADC Register
0x61	PMU_SYSPWRADC	PMU SYSPWRADC Register
0x62	PMU_REMCONADC	PMU RemConADC Register
0x63	PMU_SVCCADC	PMU SVCCADC Register
0x64	PMU_CHGIADC	PMU CHGIADC Register
0x65	PMU_IREFADC	PMU IREFADC Register
0x67	PMU_ICTEMPADC	PMU ICTEMPADC Register
0x68	PMU_AUXADC0	PMU AuxADC0 Register
0x69	PMU_AUXADC1	PMU AuxADC1 Register
0x6C	PMU_ICTEMPADC_ADJ	PMU ICTEMPADC ADJUST Register

8.3 Register Description

8.3.1 PMU_AUXADC_CTL0

PMU_AuxADC_CTL0 Register (RTCVDD) (default 0xFFFF)

Offset = 0x59

Bit(s)	Name	Description	Access	Reset
15	AUXADC0_EN	AUXADC0 ADC enable 0: disable 1: enable	RW	1
14	AUXADC1_EN	AUXADC1 ADC enable 0: disable 1: enable	RW	1
13:12	-	Reserved	-	-
11	VBUSVADC_EN	VBUS VOLATGE ADC enable 0: disable 1: enable	RW	1
10	WALLVADC_EN	WALL VOLATGE ADC enable	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		0: disable 1: enable		
9	SYSPWRADC_EN	SYSPWR VOLATGE ADC enable 0: disable 1: enable	RW	1
8	-	Reserved	-	-
7	SVCC_ADC_EN	SVCC ADC enable 0: disable 1: enable	RW	1
6	ICTEMP_ADC	TEMP ADC enable 0: disable 1: enable	RW	1
5	REMCON_ADC_EN	REMCON ADC enable 0: disable 1: enable	RW	1
4	BATIADC_EN	BAT CURRENT ADC enable 0: disable 1: enable	RW	1
3	WALLIADC_EN	WALL CURRENT ADC enable 0: disable 1: enable	RW	1
2	VBUSIADC_EN	VBUS CURRENT ADC enable 0: disable 1: enable	RW	1
1	CHGIADC_EN	Charger current ADC enable 0: disable 1: enable	RW	1
0	IREFADC_EN	CURRENT REF ADC enable 0: disable 1: enable	RW	1

8.3.2 PMU_AUXADC_CTL1

PMU_AuxADC_CTL1 Register (RTCVDD) (default 0x0100)

Offset = 0x5A

Bit(s)	Name	Description	Access	Reset
15:9	-	Reserved	-	-
8	PMU_ADC_ENABLE	PMU_ADC enable 0:disable 1:enable	RW	1
7	DATA_AVERAGE_FILTER	Data average Filter for 16 mux ADC: 0:disable 1:enable	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

6:2	-	Reserved	-	-
1	SELECT REFERENCE	Select ADC reference: 0: reference from internal circuit 1: reference source from external circuit trough 3 pins, their value are 22.5, 1.5, 0.75 separately. Or load 1μF capacitor on this pin	RW	0
0	-	Reserved	-	-

8.3.3 PMU_BATVADC

PMU_BATADC Register (RTCVDD) (default 0x0000)
Offset = 0x5B

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	BATVADC	BATVADC data	R	x

8.3.4 PMU_BATIADC

PMU_BATIADC Register (RTCVDD) (default 0x0000)
Offset = 0x5C

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	BATIADC	BATIADC data	R	x

8.3.5 PMU_WALLVADC

PMU_WALLADC Register (RTCVDD) (default 0x0000)
Offset = 0x5D

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	WALLVADC	WALLVADC data	R	x

8.3.6 PMU_WALLIADC

PMU_WALLIADC Register (RTCVDD) (default 0x0000)
Offset = 0x5E

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

11:0	WALLIADC	WALLIADC data	R	x

8.3.7 PMU_VBUSVADC

PMU_VBUSADC Register (RTCVDD) (default 0x0000)
Offset = 0x5F

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	VBUSVADC	VBUSVADC data	R	x

8.3.8 PMU_VBUSIADC

PMU_VBUSIADC Register (RTCVDD) (default 0x0000)
Offset = 0x60

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	VBUSIADC	VBUSIADC data	R	x

8.3.9 PMU_SYSPWRADC

PMU_SYSPWRADC Register (RTCVDD) (default 0x0000)
Offset = 0x61

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	SYSPWRADC	SYSPWRADC data	R	x

8.3.10 PMU_REMCONADC

PMU_REMCONADC Register (RTCVDD) (default 0x0000)
Offset = 0x62

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	REMCONADC	REMCON ADC data	R	x

8.3.11 PMU_SVCCADC

PMU_SVCCADC Register (RTCVDD) (default 0x0000)
Offset = 0x63

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	SVCCADC	SVCC ADC data	R	x

8.3.12 PMU_CHGIADC

PMU_CHGIADC Register (RTCVDD) (default 0x0000)
Offset = 0x64

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	CHGIADC	CHGIADC data	R	x

8.3.13 PMU_IREFADC

PMU_IREFADC Register (RTCVDD) (default 0x0000)
Offset = 0x65

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	IREFADC	IREFADC data	R	x

8.3.14 PMU_ICTEMPADC

PMU_ICTEMPADC Register (RTCVDD) (default 0x0000)
Offset = 0x67

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	ICTEMPADC	ICTEMPADC ADC data	R	x

8.3.15 PMU_AUXADC0

PMU_AuxADC0 Register (RTCVDD) (default 0x0000)
Offset = 0x68

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:0	AUXADC0	AuxADC0 data	R	x

8.3.16 PMU_AUXADC1

PMU_AuxADC1 Register (RTCVDD) (default 0x0000)

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Offset = 0x69

Bit(s)	Name	Description	Access	Reset
15:12	RESERVED	RESERVED	R	0
11:0	AUXADC1	AUXADC1 data	R	x

8.3.17 PMU_ICTEMPADC_ADJ

PMU_ICTEMPADC_ADJ Register (RTCVDD) (default 0x0000)

Offset = 0x6C

Bit(s)	Name	Description	Access	Reset
15:8	-	Reserved	-	-
7:0	ICTEMPADC_ADJ	ICTEMPADC correction bit	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

9 Clock Management Unit

9.1 Universal Clock

9.1.1 Register List

Table 9-1 CMU Register Address

Name	Base Address
CMU_CONTROL_REGISTER	0xC0

Table 9-2 CMU Registers

Offset	Register Name	Description
0x01	CMU_DEVRST	Device Reset Control Register

9.1.2 Register Description

9.1.2.1 CMU_DEVRST

Device Reset Control Register
Offset = 0x01

Bit(s)	Name	Description	Access	Reset
15:9	-	Reserved	-	-
8	AUDIO_CLK_EN	SCLK to Audio Clock Enable Control bit: 0:Disable 1:Enable	RW	0
7:3	-	Reserved	-	-
2	INTS_RST	INTS block reset	RW	1
1	MFP_RST	MFP/GPIO control block reset	RW	1
0	AUDIO_RST	Audio block reset	RW	1

Note: write 0 to reset the block.

9.2 Real Time Clock

RTC module provides system timing and alarm functions, it supports power-off and power-on by alarm. Its clock is based on 32.768 kHz oscillator, which can be provided by a built-in or external oscillator, and the external OSC is used by default.

At the system power on the internal OSC is used, then there is a process of selecting clock source, if an oscillatory waveform is detected at LOSC, the detect circuit will delay about 1ms and then set

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

RTC_CTL[3] to 1, and external OSC is selected. If no waveform is detected at LOSC, the detect circuit will delay about 3ms and set RTC_CTL[3] to 0, internal OSC will be selected.

Whether the system is in Standby or normal working mode, if the system chooses the external LOSC but the external LOSC stopped working, RTCVDD_OK will be pulled down and then the whole system will be reset. Powered on next time, the system will use internal OSC by default.

9.2.1 Module Description

32kHz Oscillator

An external 32.768 kHz crystal oscillator should be supplied to ATC2609 system to get an accurate clock for Real Time Clock (RTC) and an alarm function capable of waking up the system. If the requirement for 32.768 kHz clock is not too accurate, the system will choose the built-in oscillator instead of the external 32.768 kHz oscillator.

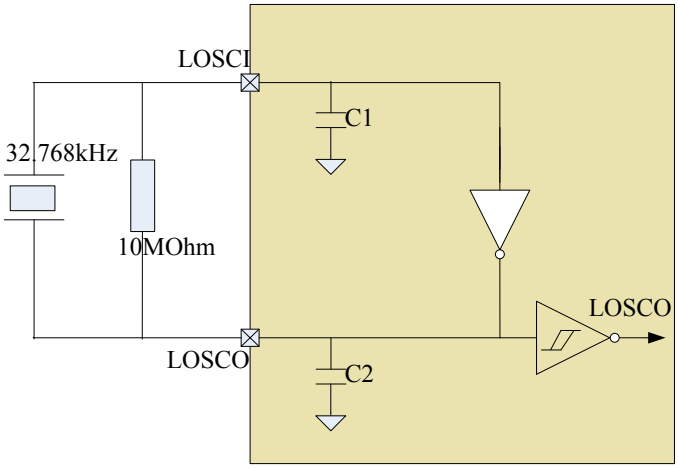


Figure 9-3 LOSC block diagram

Calendar

When RTCE=1, RTC_H, RTC_MS and RTC_YMD clock is based on LOSC_CLK, Master can only read the registers to get the current time in this case. When RTCE=0, the registers can be written to set the current time.

Alarm

When RTCE=ALIE=1, if RTC_HALM=RTC_H, RTC_MSALM=RTC_MS and RTC_YMDALM = RTC_YMD, an Alarm IRQ will be generated, which can be cleared by setting ALIP to 1.

9.2.2 Register List

Table 9-1 RTC Block Address

Name	Base Address
RTC	0x0000

Table 9-2 RTC Controller Registers

Offset	Register Name	Description

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

0x6E	RTC_CTL	RTC control register
0x6F	RTC_MSALM	RTC ALARM Minute second register
0x70	RTC_HALM	RTC ALARM Hour register
0x71	RTC_YMDALM	RTC ALARM Year month date register
0x72	RTC_MS	RTC Minute second register
0x73	RTC_H	RTC Hour register
0x74	RTC_DC	RTC day century register
0x75	RTC_YMD	RTC year month date register

9.2.3 Register Description

9.2.3.1 RTC_CTL

Calendar Control Register (RTCVDD) (default 0x5A50)
Offset=0x6E

Bit(s)	Name	Description	Access	Reset
15:14	LGS	Low frequency crystal oscillator GMNIN select bits	RW	1
13:12	LOSC_CP	LOSC Capacitor Select: 00:12pF 01:15pF 10:18pF 11:21pF	RW	1
11	RST	RTC Reset 1: Normal 0: Reset	RW	1
10	VERI	RTC Verify Clock Enable Switch RTC clock to 32kHz 1: Enable 0: Disable	RW	0
9	LEAP	RTC Leap Year bit 1: leap year 0: non-leap year	R	1
8:7	-	Reserved	-	-
6	EOSC	External Crystal OSC enable 1: Enable 0: Disable	RW	1
5	CKSS0	RTC 32kHz clock Source Select 1: External Crystal OSC 0: Built-in OSC	RW	0
4	RTCE	RTC Enable 1: Enable 0: Disable	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

3	EXT_LOSC_STATE	External LOSC State: 0:external LOSC stop Oscillating 1:external LOSC is Oscillating	R	x
2	-	Reserved	-	-
1	ALIE	Alarm IRQ Enable 1: Enable 0: Disable	RW	0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	RW	0

Note:

1. *Bit[5] CKSS0: only when RTCVDD is completely powered off, will CKSS0 be reset.*
2. *Calendar and Alarm module need precise low frequency clock, so an external crystal OSC is applied in application.*
3. *Bit[13:12] LOSC_CP: LOSC circuit matching capacitor selection should refer to the load capacitor of the external crystal OSC, a default value of 01 or 10 is used in general.*
4. *Bit[15:14] LGS: this bit is the LOSC circuit driving ability enhancing bit, the driving strength can be sorted as 2b11>2b10>2b01>2b00, the default value is recommended.*
5. *Bit[3] EXT_LOSC_STATE: the state bit of external starting LOSC oscillating.*

9.2.3.2 RTC_MSALM

Calendar MSALM Register (RTCVDD) (default 0x0000)

Offset=0x6F

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:6	MINAL	Alarm minute setting 0x00 : 0x3B	RW	0
5:0	SECAL	Alarm second setting 0x00 : 0x3B	RW	0

9.2.3.3 RTC_HALM

Calendar HALM Register (RTCVDD) (default 0x0000)

Offset=0x70

Bit(s)	Name	Description	Access	Reset
15:5	-	Reserved	-	-
4:0	HOUEAL	Alarm hour setting 0x00:0x17	RW	0

9.2.3.4 RTC_YMDALM

Calendar YMDALM Register (RTCVDD) (default 0x0000)

Offset=0x71

Bit(s)	Name	Description	Access	Reset
15:9	YEARAL	Alarm year setting 0x00:0x63	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

8:5	MONA	Alarm month setting 0x01:0x0C	RW	0
4:0	DATEAL	Alarm day setting 0x01:0x1F	RW	0

9.2.3.5 RTC_MS

Calendar MS Register (RTCVDD) (default 0x0000)

Offset=0x72

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:6	MIN	Time minute setting 0x00:0x3B	RW	0
5:0	SEC	Time second setting 0x00:0x3B	RW	0

9.2.3.6 RTC_H

Calendar HOUR Register (RTCVDD) (default 0x0000)

Offset=0x73

Bit(s)	Name	Description	Access	Reset
15:5	-	Reserved	-	-
4:0	HOUR	Time hour setting 0x00:0x17	RW	0

9.2.3.7 RTC_DC

Calendar DC Register (RTCVDD) (default 0x0080)

Offset=0x74

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:7	DAY	Time day setting 0x01:0x07	RW	1
6:0	CENT	Time setting 0x00:0x63	RW	0

9.2.3.8 RTC_YMD

Calendar YMD Register (RTCVDD) (default 0x0021)

Offset=0x75

Bit(s)	Name	Description	Access	Reset
15:9	YEAR	Time year setting 0x00:0x63	RW	0
8:5	MON	Time month setting 0x01H:0x0C	RW	1
4:0	DATE	Time day setting 0x01:0x1F	RW	1

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

10 Infrared Remote Controller

10.1 Features

ATC2609 Infrared Remote Controller (IRC) module Support RC5/9012/NEC(8-bit)/RC6 protocol, the sample clock is 32.576kHz. IRC is connected with an Infrared Remote (IR) receiver, only when the received key data is equal to the IRC_WK register's data, including NEC, 9012, RC5 and RC6 mode, can IRC wake up the system by generating a wake up signal to PMU.

10.2 Modules Description

10.2.1 9012 Protocol

The 9012 protocol adopts Pulse Distance Modulation. Each pulse is one Tm (560μs) 38kHz carrier burst, and LSB is transmitted first. Logic 1 takes 4Tm (2.25ms) to transmit, and logic 0 only takes 2Tm (1.12ms). A message is started by 8Tm (4.5ms) AGC burst, used to set the gain of the front IR receivers. Customer code and Command code length is both 8-bit, and they are transmitted twice to ensure the reliability of the transmission. And in the second time, Command code is inverted to Anti-code to verify the received messages.

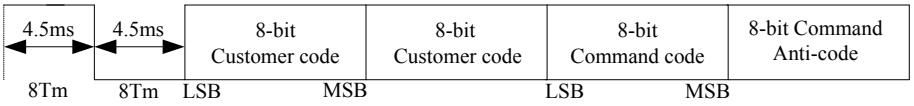


Figure 10-1 9012 Protocol of Frame

Below are some values for reference:

Recommended carrier duty-cycle = 1/4 or 1/3.

Tm = 256/Fosc = 0.56ms (Fosc=455kHz)

Repetition time = 192Tm = 108ms

Carrier frequency = Fosc/12

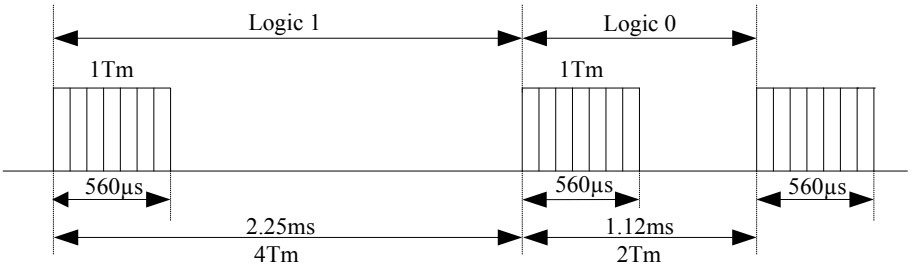


Figure 10-2 9012 Protocol of Logic transmission

When the key on the remote controller remains pressed down, the command will be transmitted only once, even a repeat code is transmitted every 192Tm as long as the key remains pressed down. This repeat code is a 8Tm (4.5ms) AGC pulse followed by a 8Tm (4.5ms) space and a logic 1 and 1Tm

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

(560μs) burst.

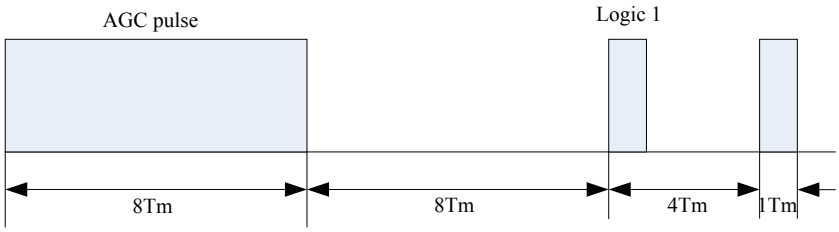


Figure 10-3 9012 Protocol of Repeat Code

10.2.2 NEC Protocol (8-bit)

The NEC protocol adopts Pulse Distance Modulation. Each pulse is one Tm (560μs) 38kHz carrier burst, and LSB is transmitted first. Logic 1 takes 4Tm (2.25ms) to transmit, logic 0 only takes 2Tm (1.12ms). A message is started by 16Tm (9ms) AGC burst, which was used to set the gain of the front IR receivers. This AGC burst is followed by 8Tm (4.5ms) space, and then the Customer and Command code. Customer and Command codes are both 8-bit, they are transmitted twice for reliability; the second customer and command code are inverted to Anti-code to verify the received message. The whole transmission time is constant because every bit is repeated with its inverted length.

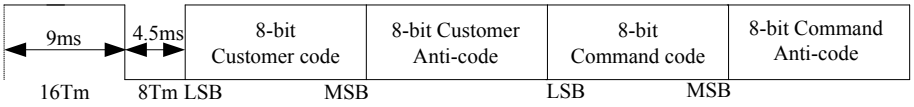


Figure 10-4 NEC Protocol of Frame

Below are some values for reference:

Recommended carrier duty-cycle: 1/4 or 1/3

Tm = 256/Fosc = 0.56ms (Fosc=455kHz)

Repetition time = 192Tm = 108ms

Carrier frequency = Fosc/12

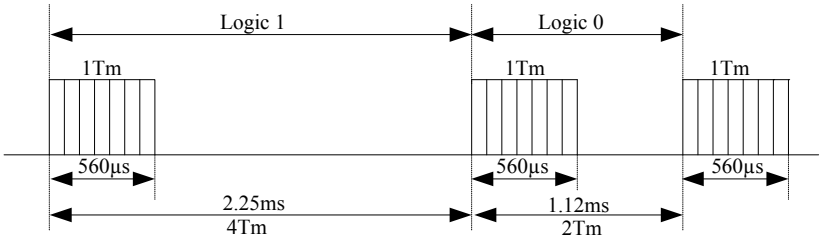


Figure 10-5 NEC Protocol of Logic transmission

When the key on the remote controller remains pressed down, the command will be transmitted only once, even a repeat code is transmitted every 192Tm as long as the key remains pressed down. This repeat code is a 16Tm (9ms) AGC pulse followed by a 4Tm (2.25ms) space and a Tm (560μs) burst.

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

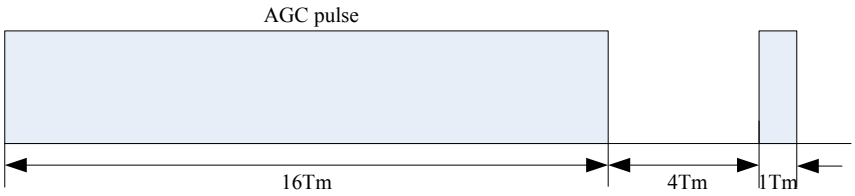


Figure 10-6 NEC Protocol Repeat Code

10.2.3 RC5 Protocol

The RC5 protocol adopts Bi-phase Modulation (or Manchester coding) of 38kHz IR carrier frequency. Transmission time of each bit is 1.8ms in this protocol, in which half of the transmission time is for the 38kHz carrier and the other half being idle. Logic 0 is a burst in the first half of the transmission time, logic 1 is a burst of the second half of the transmission time; see in Figure 10-7 below. The pulse/pause ratio of the 38kHz carrier frequency is 1/3 or 1/4, which reduced the power consumption.

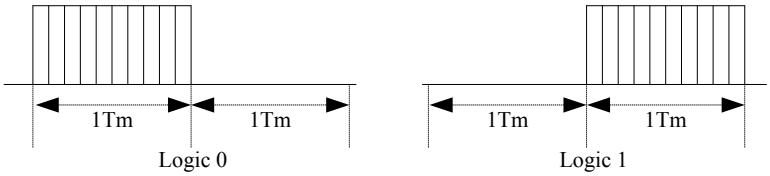


Figure 10-7 RC5 Protocol Logic

Below are some values for reference:

1 bit-time = 3*256 /Fosc= 1.688ms (Fosc=455kHz)

Tm= 1 bit-time/2=0.844ms

Repetition time= 4*16*2Tm=108ms

Carrier frequency = Fosc/12

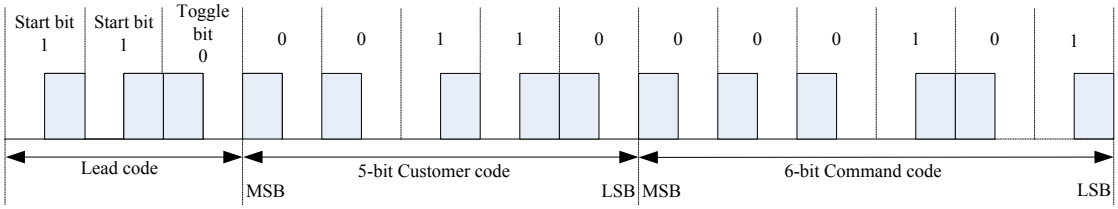


Figure 10-8 RC5 Protocol Frame

The first two pulses are start pulses, both are logic 1. Half of the transmission time will be elapsed before the receiver recognizes the real start of the message. The third bit is a toggle bit, this bit is inverted every time a key is released and pressed again. This is how the receiver distinguishes whether the key remains pressed down or repeatedly pressed. The next 5-bit Customer code represents the IR device's address, with MSB sent first. The following 6-bit command code is sent with MSB first, too. One message is 14 bits in total, which adds up to time duration of 28Tm. Sometimes a message may be shorter because the first half of the start bit S1 is idle, and if the last bit of the message is logic 0 the last half bit of the message is idle too. As long as a key remains down the message will be repeated every 128Tm (108ms). The toggle bit will remain the same logic during these repeated

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

messages. And this auto repeat feature can be configured by the receiver software.

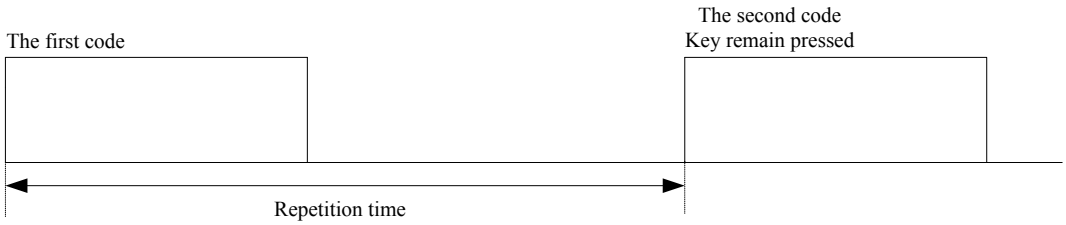


Figure 10-9 RC5 Protocol of Repetition time

10.2.4 RC6 Protocol

The RC6 Protocol of mode 0 is supported only. RC-6 signals are modulated on a 36 kHz Infrared Red carrier. The duty cycle of this carrier is recommended between 25% and 50%. Transmission data is modulated using Manchester coding. This means that each bit (or symbol) will have both a mark and space in the output signal. If the symbol is 1, the first half of the bit time is a mark and the second half is a space. If the symbol is 0, the first half of the bit time is a space and the second half is a mark.
The main timing unit is 1T, which is 16 times the carrier period (1/36kHz * 16 = 444μs)
1T =1*16 / 36kHz = 444μs
1Bit = 2T = 888μs
Total transmission time (22 Bits) = 23.1ms(message) + 2.7ms (no signal)
Repetition time = 240T = 106.7ms

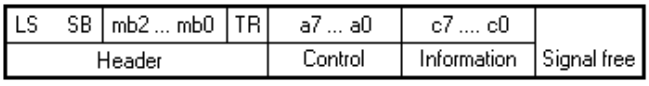


Figure 10-10 RC6 Protocol

The RC6 Protocol frame can be separated into four fields: Header, Control, Information and Signal free field. The signal free field is not used.

Header Field:

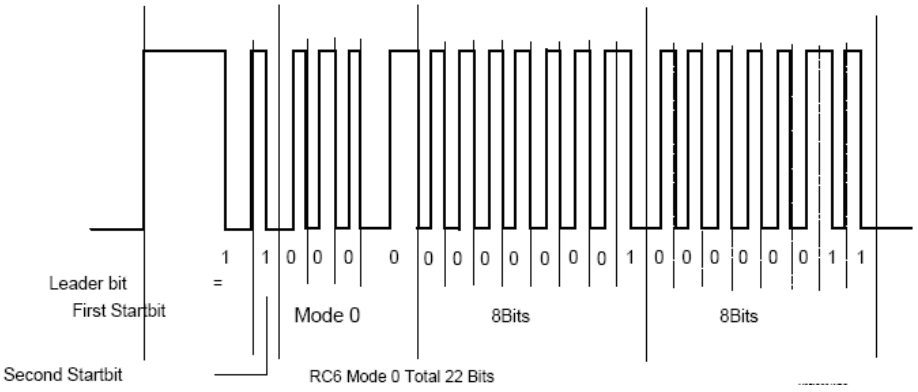


Figure 10-11 RC6 Protocol of Signal Frame

This leader bit is the start bit used to set the gain of the IR receiver unit, which has a mark time of 6T (2.666ms) and a space time of 2T (0.889ms).

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

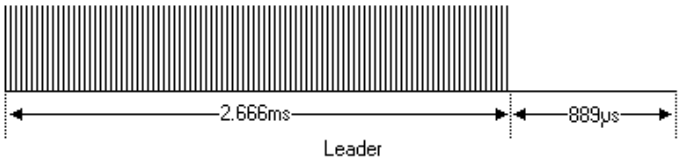


Figure 10-12 RC6 Protocol of Leader Bit

The normal bit, 0 and 1 are encoded by the position of the mark and space in the bit time, in which mark time is1T (0.444ms) and space time is1T (0.444ms).

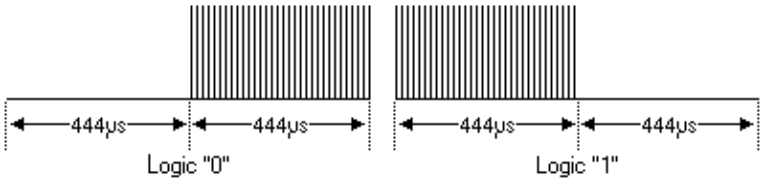


Figure 10-13 RC6 Protocol of Normal Bit

The trailer bit TR has a mark time of 2T (0.889ms) and a space time of 2T (0.889ms). Same, 0 and 1 are encoded by the position of the mark and space in the bit time. This bit functions like the traditional toggle bit, which will be inverted whenever a key is released. This bit separates a long key-press from a double key-press.

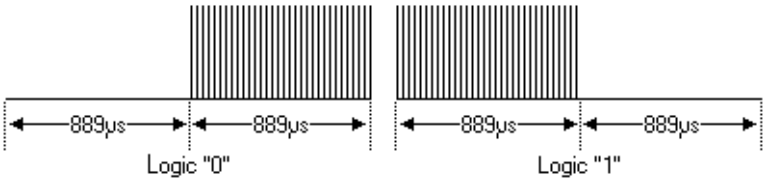


Figure 10-14 RC6 Protocol of Trailer Bit

Control field:

This field holds 8 bits which are used as address byte. This means that a total of 256 different devices can be controlled using mode 0 of RC-6. The MSB is transmitted first.

Information field:

The information field holds 8 bits which are used as command byte. This means that each device can have up to 256 different commands. The MSB is transmitted first.

10.3 Register List

Table 10-1 IRC Block Address

Name	Base Address
IRC	0x0000

Table 10-2 IRC Controller Registers

Offset	Register Name	Description
0x90	IRC_CTL	Infrared remote control register
0x91	IRC_STAT	Infrared remote status register
0x92	IRC_CC	Infrared remote control customer code register
0x93	IRC_KDC	Infrared remote control KEY data code register
0x94	IRC_WK	Infrared remote control wake up KEY data code register

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

0x95	IRC_RCC	Infrared remote control Receive Customer Code register

10.4 Register Description

10.4.1 IRC_CTL

Infrared remote control register (RTCVDD) (default 0x0000)

Offset = 0x90

Bit(s)	Name	Description	Access	Reset
15:4	-	Reserved	-	-
3	IRE	IRC enable 0: disable 1: enable	RW	0
2	IIE	IRC IRQ enable 0: disable 1:enable	RW	0
1:0	ICMS	IRC code mode select 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: RC6 code	RW	0

10.4.2 IRC_STAT

Infrared remote control register (RTCVDD) (default 0x0000)

Offset = 0x91

Bit(s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6	UCMP	User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct user code the next time. 0: user code match 1: user code don't match	RW	0
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct key data code the next time 0: key data code match 1: key data code don't match	RW	0
4	RCD	Repeated code detected, write 1 to this bit will clear it, otherwise don't change 0: no repeat code	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		1: detect repeat code		
3	-	Reserved	-	-
2	IIP	IRC IRQ pending bit, write 1 to this bit will clear it 0: no IRQ pending 1: IRQ pending The precondition of generating interrupt is all the received code is right, including user code and key, and, if the user code and key value is not correct, the repeat code following this frame won't generate interrupt.	RW	0
1	-	Reserved	-	-
0	IREP	IRC receive error pending 0: receive OK 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0

10.4.3 IRC_CC

Infrared remote control customer code register (RTCVDD) (default 0x0000)

Offset = 0x92

Bit(s)	Name	Description	Access	Reset
15:0	ICCC	Infrared remote control customer code **In RC5 mode:** Bit[4:0] is the customer code **In 9012 and NEC mode:** Bit[15:0] is the customer code, **In RC6 mode:** Bit 7:0 is the customer code. If the received customer code does not comply with this register value, error occurs.	RW	0

10.4.4 IRC_KDC

Infrared remote control KEY data code register (RTCVDD) (default 0x0000)

Offset = 0x93

Bit(s)	Name	Description	Access	Reset
15:0	IKDC	IRC key data code **In RC5 mode:** Bit 5:0 is the Key data	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		In 9012 and NEC mode: Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data **In RC6 mode:** Bit 7:0 is the Key data; If key data is received, the register will be updated; If repeat code is received, the register will not update.		

10.4.5 IRC_WK

Infrared remote control wake up KEY data code register (RTCVDD) (default 0x0000)
Offset = 0x94

Bit(s)	Name	Description	Access	Reset
15:0	IKDC	IRC wake up key data code **In RC5 mode:** Bit[5:0] is the wake up Key data **In 9012 and NEC mode:** Bit[15:0] is the wake up key data; Bit[7:0] is the Key data; Bit[15:8] is the Key anti-data **In RC6 mode:** Bit 7:0 is the wake up key data. If the received key value is same with this register, wake up signal will be generated and sent to PMU, an interrupt signal will be generated at the same time.	RW	0

10.4.6 IRC_RCC

Receive customer code register (RTCVDD) (default 0x0000)
Offset = 0x95

Bit(s)	Name	Description	Access	Reset
15:0	ICCC	Received customer code **In RC5 mode:** Bit[4:0] is the customer code **In 9012 and NEC mode:** Bit[15:0] is the customer code **In RC6 mode:** Bit[7:0] is the customer code	R	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

11 Interrupt Controller

11.1 Features

Interrupt Controller (INTC) module can receive and handle 16 Interrupt signals sent through pin EXTIRQ. Table 11-1 lists all the interrupt sources. Details about these interrupts can be found in relevant sections. Please refer to the register INTS_PD to get interrupt that has happened, besides, any of these 16 interrupts can be masked by setting register INTS_MSK.

Table 11-1 Interrupt Sources list

Interrupt Number	Sources	Type
0	AUDIO	High Level
1	OV	High Level
2	OC	High Level
3	OT	High Level
4	UV	High Level
5	ALARM	High Level
6	ONOFF	High Level
7	WKUP	High Level
8	IR	High Level
9	REMCON	High Level
10	POWERIN	High Level
11:15	Reserved	-

Note: OV-overvoltage, OC-overcurrent, OT-overtemperature, UV-Undervoltage, WKUP-Wakeup.

11.2 Block Diagram

Figure 11-1 given below shows the architecture of the interrupt controller:

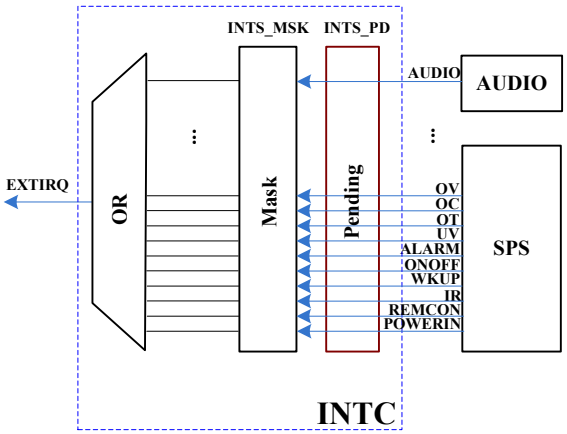


Figure 11-1 Interrupt Controller Block Diagram

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

11.3 Register List

Table 11-2 Interrupt source Block Base Address

Name	Base Address
INTS_REGISTER	0xC8

Table 11-3 Interrupt source Block Configuration Registers List

Offset	Register Name	Description
0x00	INTS_PD	Interrupt Pending register
0x01	INTS_MSK	Interrupt Mask register

11.4 Register Description

11.4.1 INTS_PD

CPU can access the status of interrupt sources by read this register. Interrupt Pending bit can not be cleared by writing 1, it is not cleared until device pending is cleared.

offset = 0x00

Bit	Name	Description	Access	Reset
15:11	-	Reserved	-	-
10:0	INTS_PD	Interrupt Pending bit. Interrupt name "n" accords to Interrupt Sources Table. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	R	INTS_PD[n]

11.4.2 INTS_MSK

CPU can enable or disable by write this register. 0: Interrupt is disabled. 1: Interrupt is enabled.

offset = 0x01

Bits	Name	Description	Access	Reset
15:11	-	Reserved	-	-
10	POWERIN	POWER IN Interrupt Mask Bit	RW	0
9	REMCON	REMOTE CONTROL Interrupt Mask Bit	RW	0
8	IR	IR Interrupt Mask Bit	RW	0
7	WKUP	WKUP Interrupt Mask Bit	RW	0
6	ONOFF	ONOFF Interrupt Mask Bit	RW	0
5	ALARM	ALARM Interrupt Mask Bit	RW	0
4	UV	UN-VOLTAGE Interrupt Mask Bit	RW	0
3	OT	OVER TEMPERATURE Interrupt Mask Bit	RW	0
2	OC	OVER CURRENT Interrupt Mask Bit	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

1	OV	OVER VOLTAGE Interrupt Mask Bit	RW	0
0	AUDIO	AUDIO Interrupt Mask Bit	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

12 General Purpose I/O

12.1 Features

This chapter will describe the multiplexing of the whole system and the GPIO function. There are 6 GPIOs in ATC2609 to provide more flexible application. The 6 GPIOs have independent inputs and outputs, and the multiplexing is software controlled and can be configured for different applications. The GPIOs support different driving capacities.

There are 3 SGPIOs in SVCC power domain. Related registers are PMU_SYS_CTL4 and PMU_SYS_CTL6 in Power Management Unit chapter.

12.2 Registers List

Table 12-1 GPIO/MFP Registers Block base Address

Name	Base Address
MFP_REGISTER	0xD0

Table 12-2 GPIO/MFP Registers Offset Address

Offset	Register Name	Description
0x00	MFP_CTL	Multiplexing Control
0x01	PAD_VSEL	PAD Voltage Selection
0x02	GPIO_OUTEN	GPIO Output Enable
0x03	GPIO_INEN	GPIO Input Enable
0x04	GPIO_DAT	GPIO Data
0x05	PAD_DRV	PAD Drive Capacity Select
0x06	PAD_EN	PAD enable control

12.3 Register Description

12.3.1 MFP_CTL

Multiplexing Control Register
Offset=0x00

Bits	Name	Description	Access	Reset
15:9	-	Reserved	-	-

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

8:7	I2S_MCLK1_LRCLK1_DOUT	I2S_MCLK1, I2S_LRCLK1, I2S_DOUT Multiplexing 00: I2S_MCLK1, I2S_LRCLK1 and I2S_DOUT 01: GPIO3, GPIO4 and GPIO5 10: SPCK, SPDA, and I2S_DOUT (SPCK and SPDA 1MOhm pull-down are enabled automatically) 11: PCM2_DATAIN, PCM2_DATAOUT, PCM0_DATAOUT	RW	0
6:5	I2S_MCLK0_LRCLK0	I2S_MCLK0 and I2S_LRCLK0 Multiplexing 00: I2S_MCLK0 and I2S_LRCLK0 01: GPIO0 and GPIO1 10: Reserved 11: PCM_CLK, PCM_SYNC	RW	0
4:3	I2S_DIN	I2S_DIN Multiplexing 00: I2S_DIN 01: GPIO2 10: I2S_DOUT 11: PCM0_DATAIN	RW	0
2	FMINLR	FMINL and FMINR multiplexing 0: FMINL and FMINR 1: PCM1_DATAOUT, PCM1_DATAIN This pad is multiplexed by analog and digital circuit.	RW	0
1:0	MICINLR	MICINLR multiplexing 00: MICINL and MICINR 01: MICINLN and MICINLP (or MICINRN and MICINRP) 10: DMICCLK and DMICDAT 11:Reserved	RW	0

Note1: When bit[1:0] is set to 10, MICINLN&MICINLP must be disabled, otherwise, DMIC PAD and MICINLN&MICINLP PAD will conflict with each other.
Note2: When bit[1:0] is set to 01, Choosing (MICINLN and MICINLP) or (MICINRN and MICINRP) is determined by MICEN & ADCEN.

12.3.2 PAD_VSEL

PAD Voltage Selection

Offset=0x01

Bits	Name	Description	Access	Reset
15:4	-	Reserved	-	-
3	I2S_MCLK0_LRCLK0	PAD Supply Voltage Select: 1:3.1V 0:1.8V	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

2	I2S_MCLK1_LRCLK1	PAD Supply Voltage Select: 1:3.1V 0:1.8V	RW	0
1	I2S_DIN_DOUT	PAD Supply Voltage Select: 1:3.1V 0:1.8V	RW	0
0	FMINLR	PAD Supply Voltage Select: 1:3.1V 0:1.8V	RW	0

12.3.3 GPIO_OUTEN

GPIO Output Enable Register

Offset=0x02

Bits	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:0	GPIO_OUTEN	GPIO[5:0] Output Enable. 0: Disable 1: Enable	RW	0

12.3.4 GPIO_INEN

GPIO Input Enable Register

Offset=0x03

Bits	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:0	GPIO_INEN	GPIO[5:0] Input Enable. 0: Disable 1: Enable	RW	0

12.3.5 GPIO_DAT

GPIO Data Register

Offset=0x04

Bits	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:0	GPIO_DAT	GPIO[5:0] Input/Output Data.	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

12.3.6 PAD_DRV

Pad Driving Capacity
Offset=0x05

Bits	Name	Description	Access	Reset
15	-	Reserved	-	-
14	DMICCLK_DRV	PAD DMICCLK Drive Capacity 0: Level 1 1: Level 2	RW	0
13	EXTIRQ_DRV	PAD EXTIRQ Drive Capacity 0: Level 1 1: Level 2	RW	0
12	TWSI_CLK_DATA_DRV	PAD TWSI_CLK&TWSI_DATA Drive Capacity 0: Level 1 1: Level 2	RW	0
11:10	I2S_MCLK1_DRV	PAD I2S_MCLK1 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0
9:8	I2S_LRCLK1_DRV	PAD I2S_LRCLK1 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0
7:6	I2S_MCLK0_DRV	PAD I2S_MCLK0 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0
5:4	I2S_LRCLK0_DRV	PAD I2S_LRCLK0 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0
3:2	I2S_DOUT_DRV	PAD I2S_DOUT Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0
1:0	I2S_DIN_DRV	PAD I2S_DIN Drive Capacity 0:Level 1 1:Level 3	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

		2:Level 5 3:reserved		

12.3.7 PAD_EN

PAD enable control

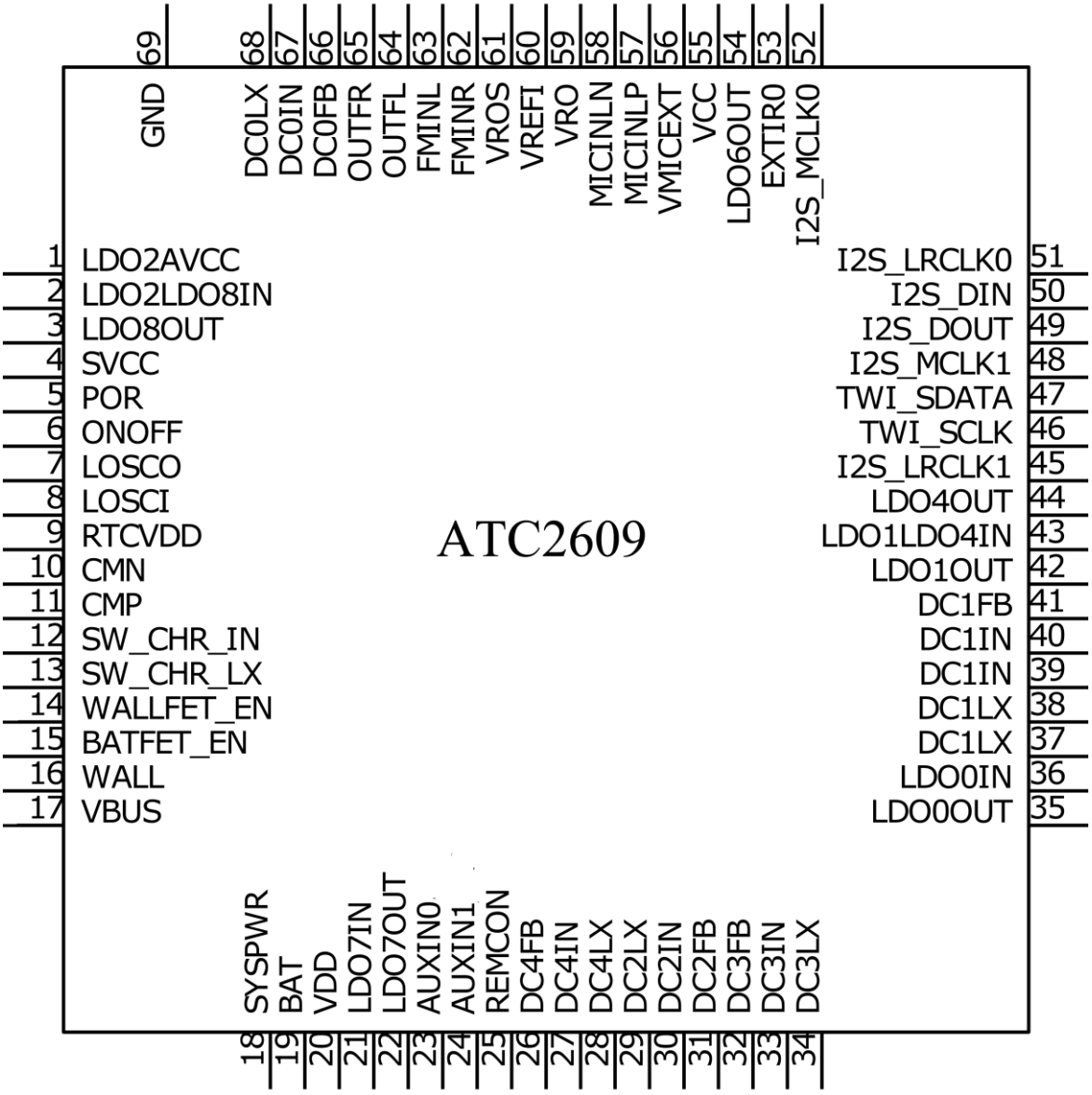
Offset=0x06

Bits	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6	PAD_EN6	1: P_I2S_MCLK0 pad enable 0: P_I2S_MCLK0 pad disable	RW	0
5	PAD_EN5	1: P_I2S_LRCLK0 pad enable 0: P_I2S_LRCLK0 pad disable	RW	0
4	PAD_EN4	1: P_I2S_DIN pad enable 0: P_I2S_DIN pad disable	RW	0
3	PAD_EN3	1: P_I2S_MCLK1 pad enable 0: P_I2S_MCLK1 pad disable	RW	0
2	PAD_EN2	1: P_I2S_LRCLK1 pad enable 0: P_I2S_LRCLK1 pad disable	RW	0
1	PAD_EN1	1: P_I2S_DOUT pad enable 0: P_I2S_DOUT pad disable	RW	0
0	PAD_EN0	1: P_EXTIRQ pad enable 0: P_EXTIRQ pad disable	RW	0

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

13 Pin Description

13.1 ATC2609 Pin Assignment



Note: This is a schematic figure for ATC2609, Pin 69 is e-pad under the IC

Figure 13-1 ATC2609 schematic pin assignment

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

13.2 ATC2609 Pin Definition

Table 13-1 ATC2609 Pin Descriptions

Pin No.	PIN Name	Function Name	I/O	Description
1	LDO2AVCC	LDO2AVCC	Power	Output of LDO2, also for analog IO
2	LDO2LDO8IN	LDO2 LDO8IN	Power	Input of LDO2 and LDO8
3	LDO8OUT	LDO8OUT	Power	Output of LDO8
4	SVCC	SVCC	Power	Power for Standby mode
5	POR	POR	AO	Power on reset to Master
6	ONOFF	ONOFF	A	ONOFF key input/reset signal
7	LOSCO	LOSCO	AO	32.768kHz crystal oscillator output
8	LOSCI	LOSCI	AI	32.768kHz crystal oscillator input
9	RTCVDD	RTCVDD	Power	VDD for RTC power domain
10	CMN	CMN	A	Coulombmeter input
11	CMP	CMP	A	Coulombmeter input
12	SW_CHR_IN	SW_CHR_IN	AI	Input of switch charger
13	SW_CHR_LX	SW_CHR_LX	A	Output of switch charger
14	WALLFET_EN	WALLFET_EN	A	Enable signal of external MOSFET connected to WALL
15	BATFET_EN	BATFET_EN	A	Enable signal of external MOSFET connected to BAT
16	WALL	WALL	Power	Wall adapter power
17	VBUS	VBUS	Power	USB power
18	SYSPWR	SYSPWR	Power	System power
19	BAT	BAT	Power	Battery power
20	VDD	VDD	Power	VDD for logic
21	LDO7IN	LDO7IN	Power	LDO7 input
22	LDO7OUT	LDO7OUT	Power	LDO7 output
23	AUXIN0	AUXIN0	A	General ADC input0
		SGPIO1		SGPIO1
		WKUP		Wake up signal
		IR		Infrared signal
		32K_OUT		32kHz output
24	AUXIN1	AUXIN1	A	General ADC input1
		SGPIO2		SGPIO2
		WKUP		Wake up signal
		IR		Infrared signal
		32K_OUT		32kHz output
25	REMCON	REMCON	A	Remote control signal
		SGPIO0		SGPIO0
		WKUP		Wake up signal
		IR		Infrared signal
26	DC4FB	DC4FB	A	DC-DC4 output
27	DC4IN	DC4IN	A	DC-DC4 input
28	DC4LX	DC4LX	A	DC-DC4 inductor connection
29	DC2LX	DC2LX	A	DC-DC2 inductor connection
30	DC2IN	DC2IN	A	DC-DC2 input
31	DC2FB	DC2FB	A	DC-DC2 output
32	DC3FB	DC3FB	A	DC-DC3 output
33	DC3IN	DC3IN	A	DC-DC3 input

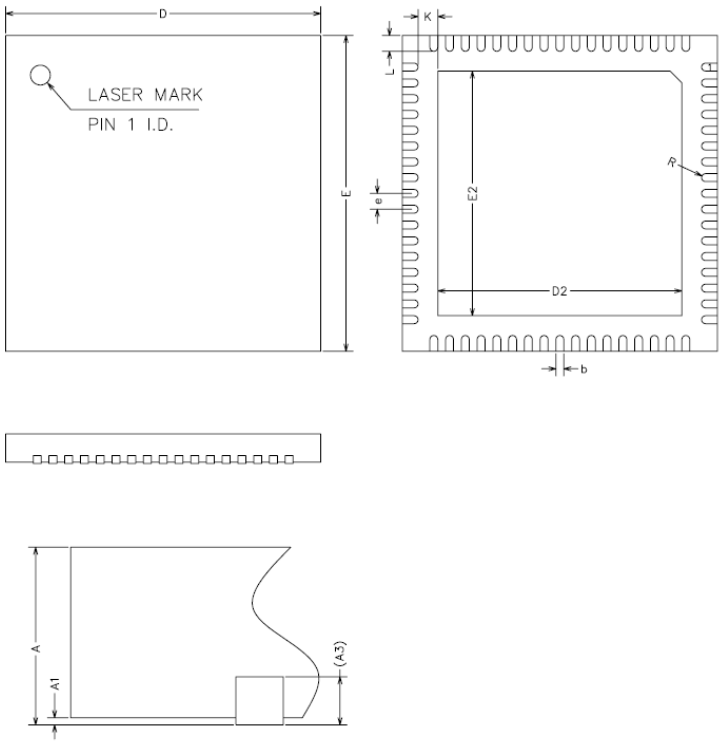
Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

34	DC3LX	DC3LX	A	DC-DC3 inductor connection
35	LDO0OUT	LDO0OUT	A	LDO0 output
36	LDO0IN	LDO0IN	A	LDO0 input
37	DC1LX	DC1LX	A	DC-DC1 inductor connection
38	DC1LX	DC1LX	A	DC-DC1 inductor connection
39	DC1IN	DC1IN	A	DC-DC1 input
40	DC1IN	DC1IN	A	DC-DC1 input
41	DC1OUT	DC1OUT	A	DC-DC1 output
42	LDO1OUT	LDO1OUT	A	LDO1 output
43	LDO1LDO4IN	LDO1LDO4IN	A	LDO1 and LDO4 input
44	LDO4OUT	LDO4OUT	A	LDO4 output
45	I2S_LRCLK1	I2S_LRCLK1	IO	I2S LR clock1
		GPIO4		General purpose input/output 4
		PCM2_DATAOUT		PCM2 data output
46	TWSI_CLK	TWSI_CLK	IO	TWSI clock
47	TWSI_SDATA	TWSI_SDATA	IO	TWSI data
48	I2S_MCLK1	I2S_MCLK1	IO	I2S master clock
		GPIO3		General purpose input/output 3
		PCM2_DATAIN		PCM2 data input
49	I2S_DOUT	I2S_DOUT	IO	I2S data output
		GPIO5		General purpose input/output 5
		PCM0_DATAOUT		PCM0 data output
50	I2S_DIN	I2S_DIN	IO	I2S data input
		I2S_DOUT		I2S data output
		GPIO2		General purpose input/output 2
		PCM0_DATAIN		PCM0 data input
51	I2S_LRCLK0	I2S_LRCLK0	IO	I2S LR clock0
		GPIO1		General purpose input/output 1
		PCM_SYNC		PCM sync
52	I2S_MCLK0	I2S_MCLK0	IO	I2S master clock
		GPIO0		General purpose input/output 0
		PCM_CLK		PCM clock
53	EXTIRQ	EXTIRQ	IO	IRQ output signal
54	LDO6OUT	LDO6OUT	A	LDO6 output signal
55	VCC	VCC	A	VCC
56	VMICEXT	VMICEXT	A	External MIC bias
57	MICINLP	MICINLP	AI	Differential mono MIC Positive channel input
		DMICDAT		DMIC data
58	MICINLN	MICINLN	AI	Differential mono MIC Negative channel input
		DMICCLK		DMIC clock
59	VRO	VRO	A	VR output
60	VREF	VREF	A	Reference voltage
61	VROS	VROS	A	VRO sense
62	FMINR	FMINR	AI	FM right channel input
		PCM1_DATAIN		PCM1 data input
63	FMINL	FMINL	AI	FM left channel input
		PCM1_DATAOUT		PCM1 data output
64	OUTFL	OUTFL	AO	Front left channel output
65	OUTFR	OUTFR	AO	Front right channel output
66	DC0FB	DC0FB	A	DC-DC0 output
67	DC0IN	DC0IN	A	DC-DC0 input
68	DC0LX	DC0LX	A	DC-DC0 inductor connection
69	e-PAD	GND	Power	Ground

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

14 Package and Ordering Information

14.1 Package Drawing



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.10	6.20	6.30
E2	6.10	6.20	6.30
e	0.30	0.40	0.50
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

Figure 14-1 ATC2609 Package Drawing

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Appendix

Acronyms and Terms

AMIC	Analog Microphone
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BT	Bluetooth
CC	Constant Current
CV	Constant Voltage
DC-DC/DC-DC	DC to DC Converter
DMIC	Digital Microphone
DAC	Digital-to-Analog Converter
GPIO	General Purpose Input/Output
HW	Hardware
IR	Infrared
I/O	Input/Output
I2S	Inter-IC Sound
LSB	Least Significant Bit
Li-Ion	Lithium Ion (battery type)
LDO	Low Dropout Regulator
MIC	Microphone
MSB	Most Significant Bit
OS	Operation System
OSC	Oscillator
PA	Power Amplifier
PMIC	Power Management Integrated Circuit
PMU	Power Management Unit
PCM	Pulse Code Modulation
PDM	Pulse Distance Modulation
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
RTC	Real-Time Clock
SCY	Sampling Cycle
SD	Secure Digital memory card
SW	Software
SoC	System on Chip
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver Transmitter

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.

Actions (Zhuhai) Technology Co., Ltd.
Address: No. 1, Ke Ji Si Road, Technology Innovation Coast of Hi-Tech Zone, Zhuhai, Guangdong, China
Tel: +86-756-3392353
Fax: +86-756-3392251
Post Code: 519085
http://www.actions-semi.com
Business Email: mmp-sales@actions-semi.com
Technical Service Email: mmp-cs@actions-semi.com

Copyright© 2015 Actions (Zhuhai) Technology Co., Ltd. All rights reserved.