Hardware Development Guide of Module Product

Product Model No: MF210V2

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Revision History

Version No.	Revised on	Reason for Revision
2.0	2013-8-23	

Applicable to: R&D engineers using MF210V2 for second development

Proposal: Before reading this document, it is recommended to understand the following knowledge and skills.

SEQ	Knowledge and skills	Reference material
1	3GPP basic AT commands	3GPP TS 27.007
2		
3		

Follow-up document: After read this document, you may need the following information.

SEQ	Reference material	Information
1	Software Development Guide of Module Product MF210V2.pdf	
2	ZTEWelink MF210V2 Module Specification.pdf	
3		

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1 About This Document

1.1 Application Scope

This document is applicable as the hardware development guide of HSUPA PCI Express Mini Card MF210V2. It is only applicable for the hardware application and development of MF210V2 product.

1.2 Purpose

This document provides design and development fundamentals for users of MF210V2. By reading this document, the user can have an overall knowledge of MF210V2 and a clear understanding of the technical parameters. With this document, the user can successfully fulfill the application and development of wireless 3G Internet product or MID equipment.

Besides the product features and technical parameters, this document also provides the service function implementation flow, driver installation and firmware upgrade information, to provide the user with a complete and detailed design reference.

1.3 Instructions

As the wireless module will need to be upgraded and improved constantly in the further, part of the content can't make sure and is instead of TBD at present. This part of the document will be updated in subsequent versions.

1.4 Abbreviations

Table 1–1 Abbreviation List

Abbreviation	Full Name
ESD	Elextro-Static discharge
EGSM	Enhanced Full Rate
GMSK	Gaussian Minimum Shift Keying
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
I/O	Input/Output
LED	Light Emitting Diode
PCS	Personal Cellular System
PCL	Power Control Level
PCS	Personal Communication System

QPSK	Quadrate Phase Shift Keying
SPI	Serial Peripheral Interface
WCDMA	Wideband Code Division Multi Access
UMTS	Universal Mobile Telecommunication System
BER	Bit Error Rate
EMC	Electromagnetic Compatibility
ACLR	Adjacent Channel Leakage power Ratio
ACS	Adjacent Channel Selectivity
AFC	Automatic Frequency Control
AGC	Automatic Gain Contol
AMR	Adaptive Multi Rate
ASD	Acceleration Spectral Density
ATM	Asynchronous Transfer Mode
BLER	Block Error Ratio
CN	Core Network
CW	Continuous Wave (un-modulated signal)
DL	DownLink
DPCH	Dedicated Physical Channel
DPCH_Ec	Average energy per PN chip for DPCH. DPCH
EVM	Error Vector Magnitude
FDD	Frequency Division Duplexing
SIM	Subscriber Identification Module
SMS	Short Message Service
USB	Universal Serial Bus

2 Product Overview

MF210V2 is one HSPA wireless Internet module with PCI Express Mini Card interface. It is applicable, but not limited, to realize the embedded functions of internet access on the notepad as a figure illustrating the product itself. The functions of MF210V2 are described as below.

- It can support UMTS/HSDPA/HSUPA 850(900)/1900/2100MHz frequency band, and GSM/GPRS/EDGE 850/900/1800/1900MHz frequency band.
- It can provide the GSM/GPRS/EDGE and UMTS/HSDPA/HSUPA high-speed data access service under the mobile environment.
- Support SMS and GPS/AGPS.
- It provides major PIN interfaces such as the power interface, SPI interface, UIM card interface (3.0V/1.8V), USB2.0 interface, UART interface and GPIO interface.

Figure 2–1 Product Illustration

2.1 Technical Parameters

Table 2–1 is a list of the major technical parameters and features supported by MF210V2.

Table 2–1 Major Technical Parameters

Name	Parameter Item	Specifications
Mechanical Feature	Dimensions	51mm * 30mm * 4.7mm
	Weight	About 12g
	Form Factor	PCI Express Mini Card
Solution	Chipset supplier	Qualcomm
Baseband	Chipset	Qualcomm
	Processor	ARM 9
	Processor speed (Apps)	MSM6290:High-performance ARM926EJ-STM running at up to 297.6 MHz for 7.2 Mbps HSDPA
	USIM/SIM	Standard 6 PIN SIM card interface 3V SIM card and 1.8V SIM card

Name	Parameter Item	Specifications	
	Memory(SDRAM/ NAND)	32MByte/128MByte	
	USB Version	USB 2.0 HIGH SPEED	
	Interface	PCI EXPRESS MINI CARD	
	Maximum power consumption	2.2W (The maximum power consumption of MF210V2 refers to the average value measured under the maximum transmission power)	
	Power supply	DC 3. 3V	
	Working current[1]	Peak current	≤2.3 A
		Average normal working current	≤560mA
		Average normal working current (without services)	≤150mA
		Standby current	about 4.6mA
	LED pin	Support	
RF	Chipset	Qualcomm	
	GSM Band	EDGE/GPRS/GSM: 1900/1800/900/850MHz	
	UMTS Band	HSUPA/HSDPA/WCDMA: 2100/1900/850(900)MHz;	
	RxDiv Band	2100/1900/850(900)MHz	
	Max. transmitter power	UMTS2100/1900/850(900): Power Class 3 (+24dBm +1/-3dBm) GSM/GPRS 850MHz/900MHz: Power Class 4 (+33dBm ±2dBm) GSM/GPRS 1800MHz/1900MHz: Power Class 1 (+30dBm ±2dBm) EDGE 850MHz/900MHz: Power Class E2 (+27dBm ±3dBm) EDGE 1800MHz/1900MHz: Power Class E2 (+26dBm -4/+3dBm)	
	Receiving sensitivity	WCDMA2100: ≤-106.7dBm WCDMA1900/850: ≤-104.7dBm WCDMA900: ≤-103.7dBm GSM850/900/1800/1900: ≤-102dBm	
	Rx Diversity (optional)	2100/1900/AWS/850/900MHz;	
	Equalization	Support	
	Main Antenna interface	Support	
	Receive Diversity (GPS) Antenna interface	Support GPS and diversity antenna, but they are not supported simultaneously. ZTEWelink does not provide the antenna, and the antenna is provided by the third party. They are swiched by AT command.	
Technical Standard	GSM/EDGE/ WCDMA	GSM CS: UL 9.6kbps/DL 9.6kbps GPRS: Multi-slot Class 10 EDGE: Multi-slot Class 10 WCDMA CS: UL 64kbps/DL 64kbps WCDMA PS: UL 384kbps/DL 384kbps	
	HSDPA/HSUPA	HSDPA: DL 7.2Mb/s(Category 8) HSUPA: UL 5.76Mb/s(Category 6)	

Name	Parameter Item	Specifications
	Protocol	<HSUPA/HSDPA/WCDMA/EDGE/GPRS/GSM>
	3GPP Release	R99,R5,R6
	OS	Windows XP (SP2 and later)
		Windows Vista (32bit)
		Windows Vista (64bit)
		Windows 7
		Linux
		Android
	GPRS Class	Class B
Environment	Operating Temperature	-25 to 60° C
	Storage Temperature	-40 to 85° C
	Humidity	5%~ 95%
Application	RAS	Support
	SMS	Support
	MMS	Optional
	STK	Optional
	USSD	Support
	Phonebook	Support
	NETWORK LOCK	Support
	SIM READER	Optional
	Language	English by default
	Update	Optional

Note: 1. In the working current, the peak current, average normal working current, average normal working current (without services) are all the maximum value measured under the maximum power consumption.

2.2 Bearing Services & Working Frequency

2.2.1 Bearing Services

- Bears PS services under the WCDMA mode: The maximum downlink transmission rate is 384Kbit/s, and the maximum uplink transmission rate is 384Kbit/s.
- Bears CS services under the WCDMA mode: Data service of 64Kbit/s.
- HSDPA supports a maximum downlink transmission rate of 7.2Mbit/s.
- HSUPA supports a maximum uplink transmission rate of 5.76Mbit/s.
- Supports the EDGE CLASS12/GPRS CLASS10 bearer service of PS domain.

2.2.2 Working Frequency Band

Table 2–2 describes the working frequency band of MF210V2 from the two aspects of GSM and UMTS.

Table 2–2 Working Frequency Band

Working Frequency Band	Uplink Frequency Band	Downlink Frequency Band
UMTS850	824 MHz — 849 MHz	869 MHz — 894 MHz
UMTS900	880 MHz — 915 MHz	925 MHz — 960 MHz
UMTS1900	1850 MHz — 1910 MHz	1930 MHz — 1990 MHz
UMTS2100	1920 MHz — 1980 MHz	2110 MHz — 2170 MHz
GSM850	824 MHz — 849MHz	869 MHz — 894 MHz
GSM900	890 MHz — 915MHz	935 MHz — 960MHz
GSM1800	1710 MHz — 1785MHz	1805 MHz — 1880MHz
GSM1900	1850 MHz — 1910MHz	1930 MHz — 1990MHz

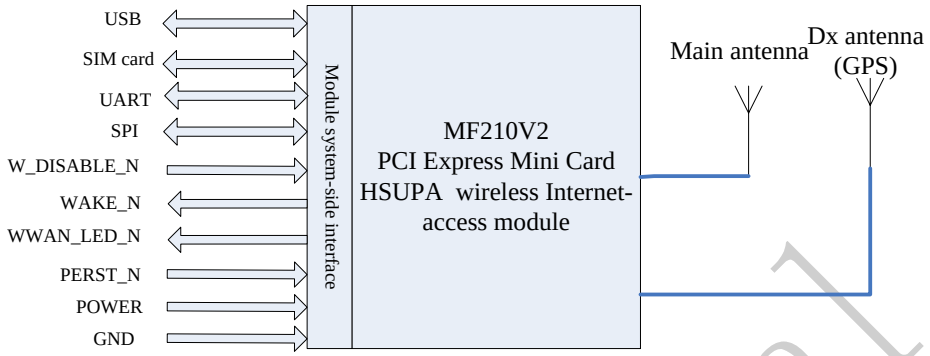
2.3 Application Frame

Figure 2–2 Application Frame

2.4 System Connection Diagram

When MF210V2 is connected to the system board, the following signal groups are involved: USB signal, SIM card signal, SPI interface signal, WAKE_N wakeup (PC) signal, working status indicator signal WWAN_LED_N, RF switch control signal W_DISABLE_N, whole-set reset signal PERST_N, power and grounding. Meanwhile, MF210V2 also provides the main antenna, and the Dx antenna. Figure 2–3 is a system connection diagram.

Figure 2–3 System Connection Diagram



3 Mechanic Features

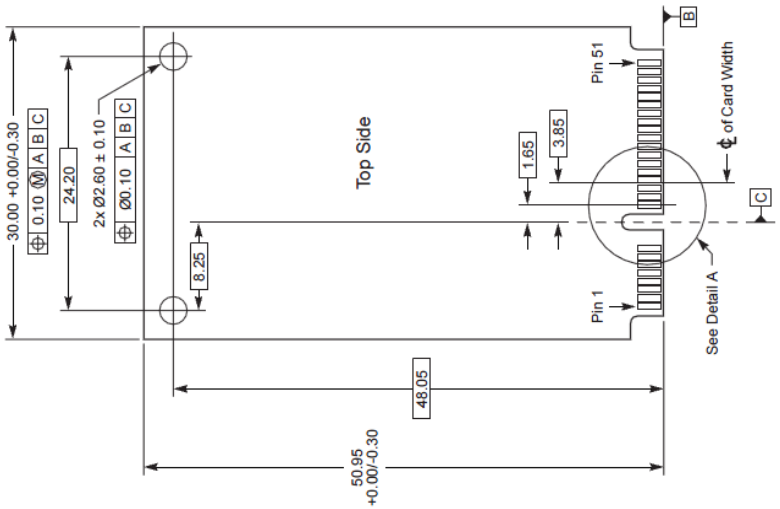
3.1 Dimensions

MF210V2 employs the standard PCI Express Mini Card interface type, with its dimensions designed according to F2 type (compared with the F1 type, devices are forbidden to lay out on the BOTTOM side). Figure 3-1 illustrates the dimensions and slot compatibility of PCI Express Mini Card.

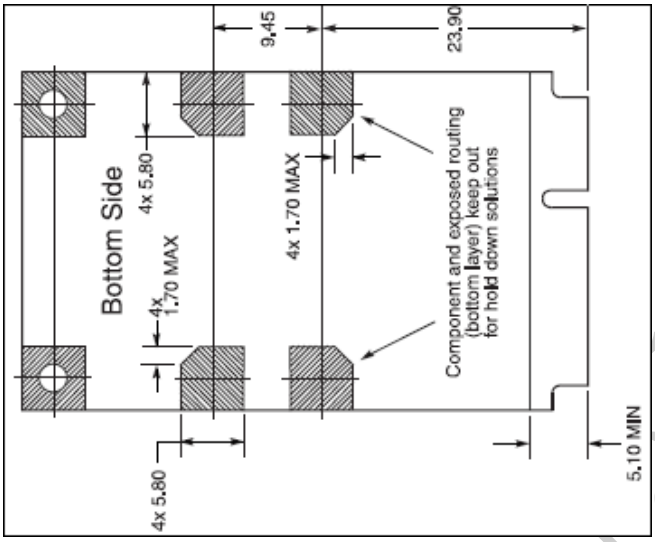
Table 3–1 PCI Express Mini Card Dimensions & Slot Compatibility

Card Type		Full−Mini−Only Socket	Half−Mini−Only Socket	Dual−Use Socket	Dual Head-to-Head Socket	
		Connector A	Connector A	Connector A	Connector A	Connector B
F1	Full-Mini	Yes	No	No	No	No
F2	Full-Mini with bottom-side keep outs	Yes	No	Yes	Yes	No
F3	Half-Mini	No	Yes	Yes	Yes	No
F4	Half-Mini with bottom-side keep outs	No	Yes	Yes	Yes	Yes

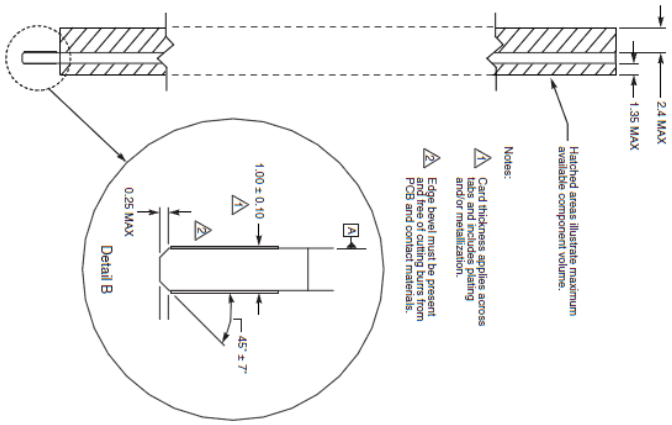
Figure 3–1 PCI Express Mini Card Dimensions



(a)



(b)



(c)

Note: Figure(a) illustrates the dimensions on TOP face. Figure(b) illustrates the dimensions on BOTTOM face. Figure(c) illustrates the thickness.

3.2 Antenna Interface

MF210V2 has three RF antenna interfaces: the main antenna interface (with “MAIN” indication on PCB), Rx (GPS) antenna (Dx and GPS are alternative, but are not supported at the same time) interface (with “AUX” indication on PCB), as shown in Figure 3–2. The antennal interface employs the U.FL-R-SMT(10) RF console by HRS Corporation, as shown in Figure 3–3. For the specified cables on the RF interface, it is recommended to use U.FL_LP_088 of HRS Corporation, as shown in Figure 3–4.

Figure 3–2 Antennal Interface Diagram (With Dx)

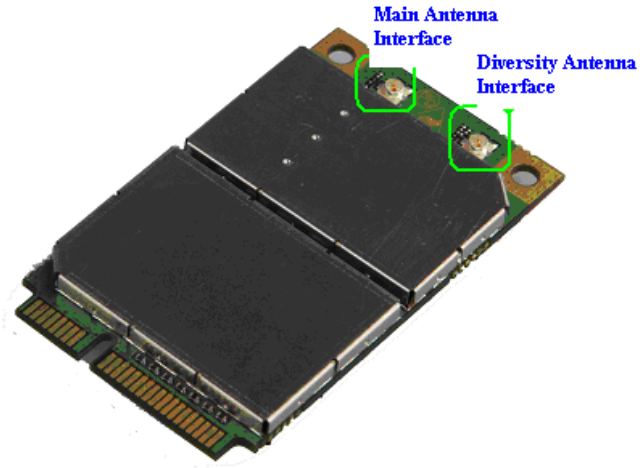


Figure 3–3 RF Interface Testing Console (U.FL-R-SMT(10) of HRS Corporation)

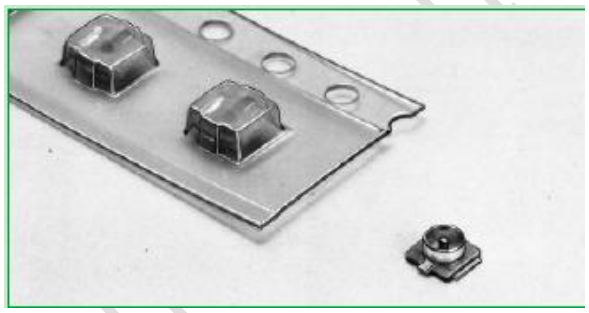
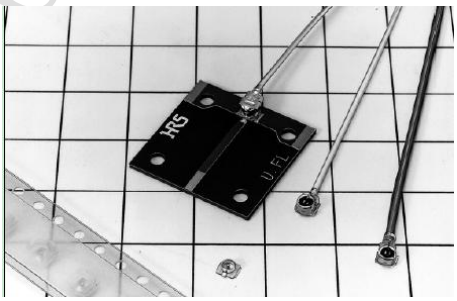


Figure 3–4 Testing Cable



3.3 Heat-dissipation Design

The heat-dissipation design of MF210V2 strictly complies with *PCI Express Mini Card Electromechanical Specification Revision 1.2, October 26 2007*. The heat sources are evenly distributed, and MF210V2 has a very excellent heat-dissipation design. To ensure that the product performance is fully played out, it is recommended to design the main board as follows:

- Locate MF210V2 far away from the switch power and high-speed signal cable as much as possible. Well protect the wiring of the interference sources.
- The antenna, and the coaxial cable connecting the network cable and the antenna, cannot be located close the interference sources.
- Do not locate MF210V2 close to devices with large heat dissipation, such as CPU, south bridge, etc. The high temperature will affect the RF performance.

4 Description of PINs

4.1 Definition of PIN Signals

The interfaces of MF210V2 are designed according to PCI Express Mini Card Electromechanical Specification Revision 1.2, October 26 2007. Figure 4–1 illustrates the PIN sequence, and Table 4–1 describes the detailed PIN definitions.

Figure 4–1 PIN Distribution Diagram

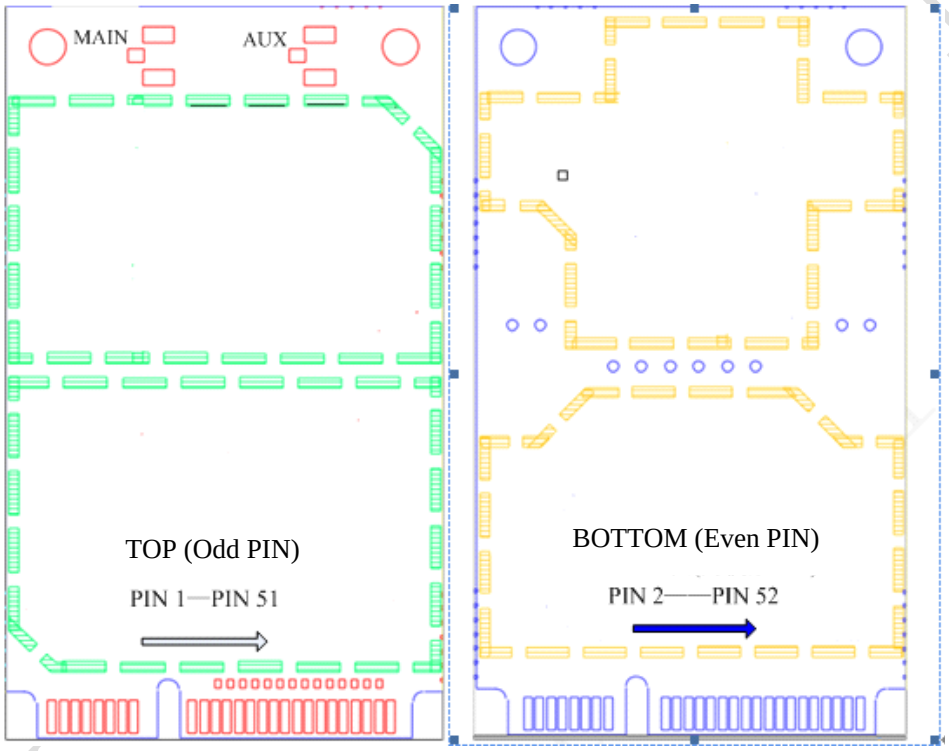


Table 4–1 PIN Definitions

PIN	Protocol Signal	MF210V2 Signal	Pin Reuse	Pin Voltage (Pad group)	Pin I/O	PU/ PD	Description of Pins
1	WAKE#	WAKE_N	Reserved	--	O	--	The default is wakeup signal, and can be reused as another signal by 0 ohm resistance
2	3.3Vaux	VDD_3V3	--	3.3V	I	--	Power pin, Input range of power pin. (3.0-3.8V)
3	COEX1	SPI_SDI	Reserved	--	I	--	The default is SPI data signal, and can be reused as another signal by 0 ohm resistance
4	GND	GND	--	--	--	--	GND pin

PIN	Protocol Signal	MF210V2 Signal	Pin Reuse	Pin Voltage (Pad group)	Pin I/O	PU/ PD	Description of Pins
5	COEX2	SPI_SDO	Reserved	--	O	--	SPI data signal (optional), and can be reused as another signal by 0 ohm resistance
6	1.5V	SPI_CS	--	--	O	--	SPI segment signal
7	CLKREQ#	SPI_CLK	Reserved	--	--	--	SPI synchronization clock (optional), and can be reused as another signal by 0 ohm resistance
8	U(S)IM_PWR	VREG_UIM	--	P2	O	--	USIM Power
9	GND	GND	--	--	--	--	GND pin
10	U(S)IM_DATA	UIM_DATA	--	P2	I/O	--	USIM data signal
11	REFCLK-	UART1_RX	--	--	I	--	UART port receive data
12	U(S)IM_CLK	UIM_CLK	--	P2	O	--	USIM clock signal
13	REFCLK+	UART1_TX	--	--	O	--	UART port transmit data
14	U(S)IM_RESET	UIM_RST	--	P2	O	--	USIM resetting signal
15	GND	GND	--	--	--	--	GND pin
16	U(S)IM_VPP	UART1_DSR	--	P1	O	--	Data is ready
17	Reserved(U(S)IM_C8)	UART1_RI	--	--	I	--	Ringtone indicator
18	GND	GND	--	--	--	--	GND pin
19	Reserved(U(S)IM_C4)	N/C	--	--	--	--	--
20	W_DISABLE#	W_DISABLE_N	--	P1	I	PU	RF pin, This pin can be configured for RF or equipment control.
21	GND	GND	--	--	--	--	GND pin
22	PERST#	PON_RESET_N	--	P1	I	PU	Module's reset signal, valid upon low level, pull-up inside the module
23	PERn0	UART1_CTS	--	--	I/O	--	UART port, clear to send
24	+3.3Vaux	VDD_3V3	--	3.3V	I		Input range of power pin. (3.0-3.8V)
25	PERp0	UART1_RFR	--	--	O	--	UART port, preparing to receive
26	GND	GND	--	--	--	--	GND pin
27	GND	GND	--	--	--	--	GND pin
28	+1.5V	N/C	--	--	--	--	--
29	GND	GND	--	--	--	--	GND pin
30	SMB_CLK	Reserved	--	--	--	--	--
31	PETn0	UART1_DTR	--	--	I	--	UART1 data terminal ready
32	SMB_DATA	Reserved	--	--	--	--	--

PIN	Protocol Signal	MF210V2 Signal	Pin Reuse	Pin Voltage (Pad group)	Pin I/O	PU/ PD	Description of Pins
33	PETp0	UART1_DCD	--	--	I	--	UART1 carrier wave detection
34	GND	GND	--	--	--	--	GND pin
35	GND	GND	--	--	--	--	GND pin
36	USB_D-	USB_DM	--	--	I/O	--	USB differential signal
37	GND	GND	--	--	--	--	GND pin
38	USB_D+	USB_DP	--	--	I/O	--	USB differential signal
39	+3.3Vaux	VDD_3V3	--	3.3V	I	--	Input range of power pin. (3.0-3.8V)
40	GND	GND	--	--	--	--	--
41	+3.3Vaux	VDD_3V3	--	3.3V	I		Input range of power pin. (3.0-3.8V)
42	LED_WWAN#	LED_WWAN_N	--	--	O	--	LED pin, Work status indication
43	GND	GND	--	--	--	--	GND pin
44	LED_WLAN#	N/C	--	--	--	--	--
45	Reserved	Reserved	--	--	--	--	--
46	LED_WPAN#	SLIC_INT	--	2.6V	O	--	exclusive use for routing adaptation
47	Reserved	Reserved	--	--	--	--	--
48	+1.5V	SLIC_RESTE	--	2.6V	O	--	exclusive use for routing adaptation
49	Reserved	Reserved	--	--	--	--	--
50	GND	GND	--	--	--	--	GND pin
51	Reserved	Reserved	--	--	--	--	--
52	+3.3Vaux	VDD_3V3	--	3.3V	I	--	Input range of power pin. (3.0-3.8V)

Note: * “N/C” indicates Not Connected. That is, MF210V2 has no internal connection.

4.2 Description of Major PIN Signals

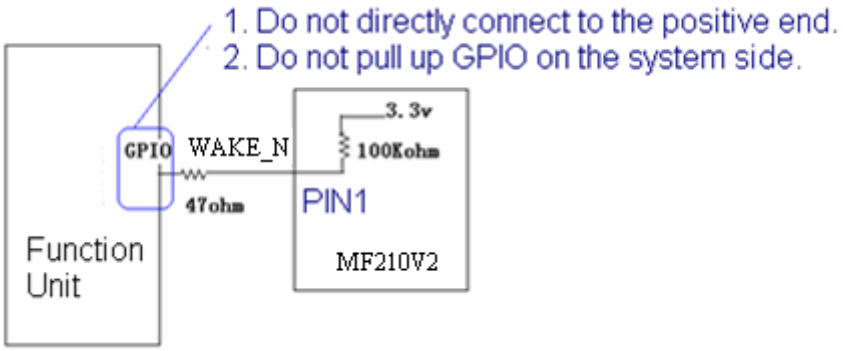
The following section describes the common pins of MF210V2 module, including the functions of each PIN, its default input and output features, and its matched circuits. The user can reasonably design the application circuits on the system board according to the PIN descriptions.

4.2.1 WAKE_N Signal

Figure 4–2 illustrates the reference connection circuit of WAKE_N signal. The WAKE_N signal (PIN No. 1) is an output signal, active low. This signal is a reserved signal for MF210V2 to wake up the system host. MF210V2 pulls up the power level to 3.3.V internally by the 100Kohm resistance. It is recommended to connect the 47ohm resistance to the GPIO PIN on the main chip (If this GPIO PIN is on the system side, it can wake up the host).

Note: Do not directly connect this signal to the positive end of the power supply.

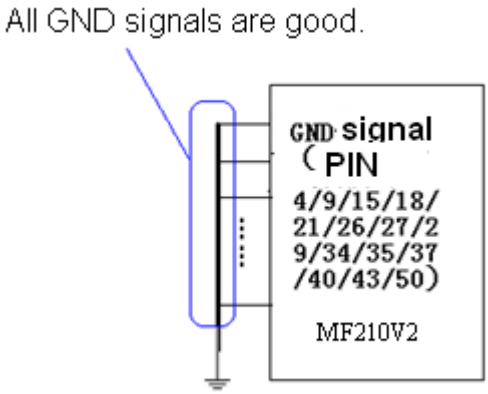
Figure 4–2 Reference Connection Circuit of WAKE# Signal



4.2.2 GND Interface

The GND signal (PIN No: 4/9/15/18/21/26/27/29/34/35/37/40/43/50). This is the power grounding and signal grounding of MF210V2. They need to be all connected to the ground level of system boards. The incomplete connection of GND signals will affect the performance of MF210V2.

Figure 4–3 GND Signal Connection



4.2.3 3.3Vaux Power (Power Interface)

The 3.3Vaux signal (PIN No: 2/24//39/41/52). This is the positive signal of 3.3V power, and is also the input signaling of MF210V2 power. The power supply is recommended to be within the range of 3.0~3.8V. If the network is in poor situation, the antenna will transmit at the maximum power, and the transient maximum peak current can reach as high as 2.3A. So the power supply capacity for peak current on the main board needs to be above 2.3A, and the average peak current needs to be above 0.9A.

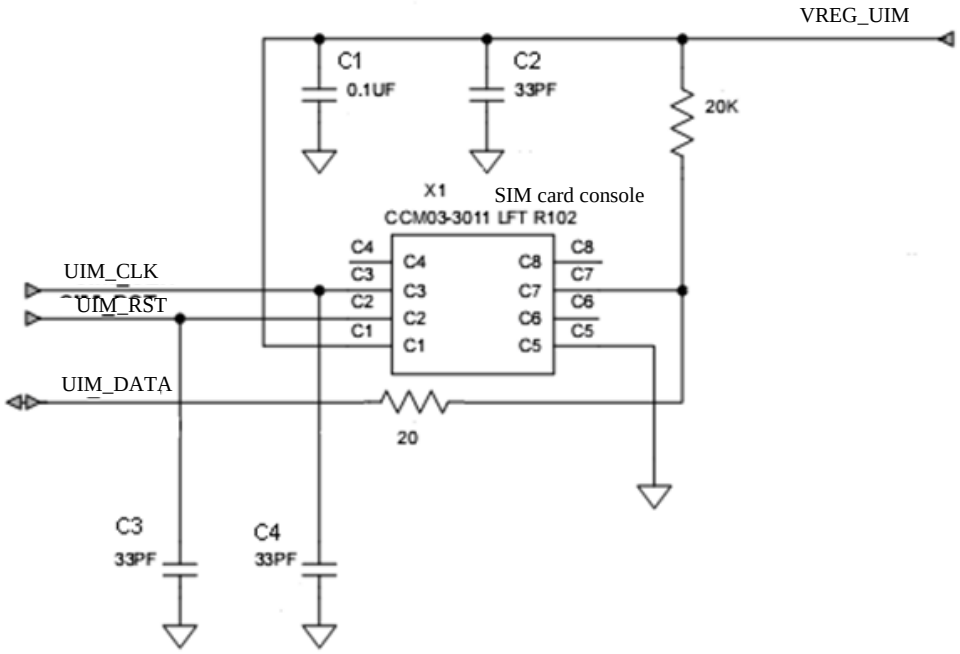
4.2.4 Signal Group of UIM Card

The signal group of UIM card (PIN No: 8/10/12/14/16) is the signal of USIM card. Table 4–2 is a detailed description of each signal. As the USIM card console is placed on the system board side, be sure to add the ESD protection during the design. Figure 4–4 shows the reference circuit design.

Table 4–2 Definition and Description of UIM Card Signal Group

PIN	Protocol Signal	Signal Definition	Signal Description
8	UIM_PWR	VREG_UIM	USIM card power, output by MF210V2
10	UIM_DATA	UIM_DATA	USIM card DATA signal, two-way signal
12	UIM_CLK	UIM_CLK	USIM card clock signal, output by MF210V2
14	UIM_RESET	UIM_RST	USIM card reset signal, output by MF210V2

Figure 4–4 Connection Circuit of U(S)IM Card Signal



NOTE:

The PCB wiring of UIM card should be laid closely around the module as possible as you can, and the ESD component should be put near the UIM card socket.

4.2.5 W_DISABLE_N Signal

The W_DISABLE_N signal (PIN No: 20) is the input signal of MF210V2, active low. Table 4–3 describes its control logic.

Table 4–3 Definition and Description of W_DISABLE# Signal

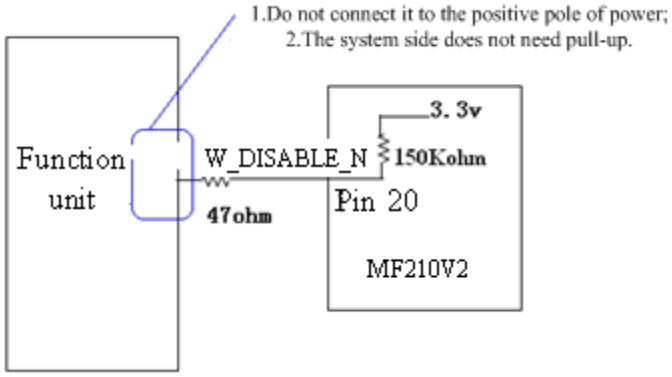
W_DISABLE_N	MF210V2 Status
'1'	RF is enabled.
'0'	RF is disabled.

The W_DISABLE_N signal is pulled up by the 150Kohm resistance to 3.3V inside MF210V2, so the system side does not pull up this circuit any more.

Note: Do not directly connect this signal to the positive end of power supply.

Figure 4–5 illustrates the reference circuit design of W_DISABLE_N signal.

Figure 4–5 Reference Circuit Design of W_DISABLE# Signal



4.2.6 PON_RESET_N Signal

The PON_RESET_N signal (PIN No: 22) is the system reset signal of MF210V2, active low. Table 4–4 illustrates its control logic. Figure 4-6 shows that pull down the reset key (PON_RESET_N) to 100ms will reset the module.

Note: Do not directly connect this signal to the positive end of power supply.

Table 4–4 Definition and Description of PON_RESET_N Signal

PON_RESET_N	MF210V2 Status
'1'	MF210V2 is in the normal working status.
'0' and t≥100ms	RF is in the OFF mode, MF210V2 is reset.

Figure 4–6 Reference Circuit Design of PON_RESET_N Signal

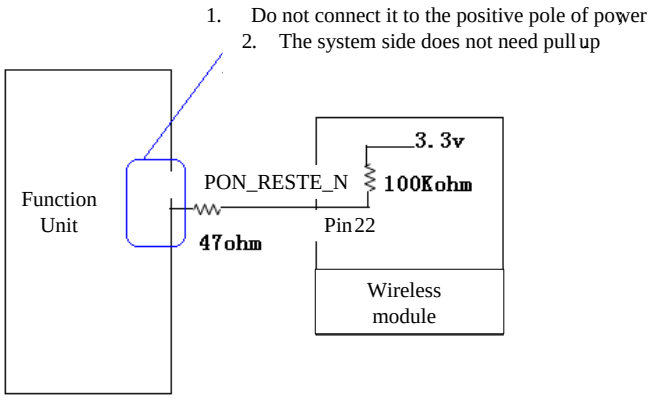
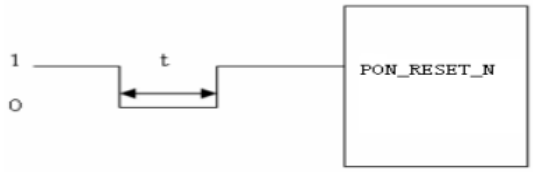


Figure 4–7 Resetting signal



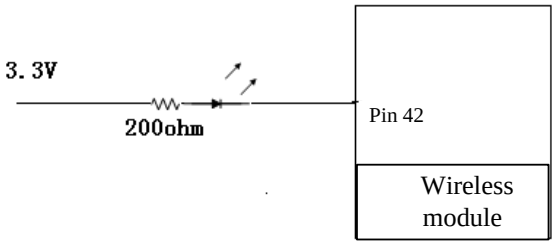
4.2.7 LED_WWAN_ N Signal (Status Indication PIN)

The LED_WWAN_N signal (PIN No: 42) is the signal indicating the current working status of MF210V2, which is generated by MF210V2. The LED indicator is on the system side, and the LED indicator is ON when this signal generates the low power level. Table 4–5 illustrates the indicator status, and Figure 4–8 illustrates the reference circuit design of LED_WWAN_N signal.

Table 4–5 Description of LED_WWAN_N Status

LED_WWAN_N Signal Status	RF Status of MF210V2	Expected Indicator Status
High power level '1', 3.3V	RF is OFF: RF is disabled	The indicator is OFF.
Low power level '0', 0V	RF is ON: RF is enabled, but there is no data transmission.	The indicator is always on.
High power level and low power level alternatively: 0V and 3.3V	RF is ON: there is data transmission.	The indicator is flashing.

Figure 4–8 Reference Design Circuit of WWAN_LED_N



4.2.8 USB Bus Interface

MF210V2 has a high-speed USB2.0 interface, which supports both the full-speed mode and the high-speed mode. It is connected to the system board side through the PCI-E interface, with the PIN No as 36 (USD_DM) and 38 (USB_DP). The USB bus is mainly used in data transmission, software upgrade, DIAG, software LOG snatch and module program detection.

4.2.9 UART Interface

The UART interface is used as MODEM port by default which is occupied by data service.

4.2.9.1 Description of PINs

MF210V2 wireless module supports the full UART interface with flow control function, which complies with the RS-232 interface protocol, and supports the 8-byte serial bus interface or 2-byte serial interface. The module can perform the serial communication and AT instruction interaction with external.

This UART port supports the programmable data width, programmable data stop bit and programmable parity check, and has an independent TX and RX FIFOs (512 bytes for each). For the normal UART application (non-Bluetooth), the maximum baud rate is 230400bps, and the default baud rate is 115200bps. The PINs are defined as shown in Table 4-6.

Table 4–6 Definition of UART Signal

PIN	Signal Name	Description	Function
23	UART1_CTS	UART port CTS clear to send	UART power level is 2.6V.
25	UART1_RFR	UART port RFR preparing to receive	
13	UART1_TX	UART port TX transmit data	
11	UART1_RX	UART port RX receive data	
31	UART1_DTR	DTE is ready	--
17	UART1_RI	Ringtone indicator	--
16	UART1_DSR	Data is ready	--
33	UART1_DCD	Carrier detection	--

4.2.9.2 Electric Feature

During the software interconnection process, there is a method of capturing logs, and it is recommended that this interface be kept during the design and the testing point be reserved. If the module is used together with the application processor, and the PWL matches with 2.6V, the connection mode is as shown in Figure 4-9. The 4-wire or 2-wire mode can be used for connection. The module interface PWL is 1.8V. If it does not match the PWL of AP interface, it is recommended to add the PWL conversion circuit. Otherwise, it might cause unstable com ports because the level is not matched or cause damage to the module because it is at high level for long time.

The connection of MF210V2 UART port and standard RS-232-C interface can be through the chip like class 232. The design involves the transformation of TTL level and EIA level. We recommend to use the chip of NLSX5014MUTAG. If using the 2-byte serial bus

interface, MAX3232 is recommended, and if using the 8-byte serial bus interface, SP3238 or MAX3238 is recommended. The connection mode is as shown in Figure 4-10.

Figure 4–9 Module Serial Port & AP Application Processor

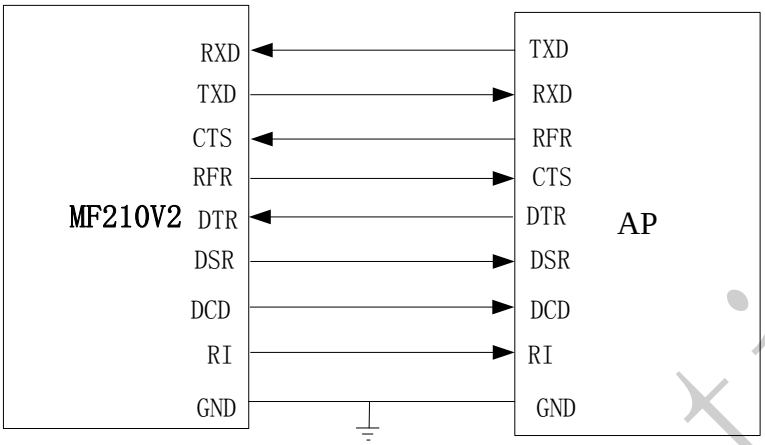
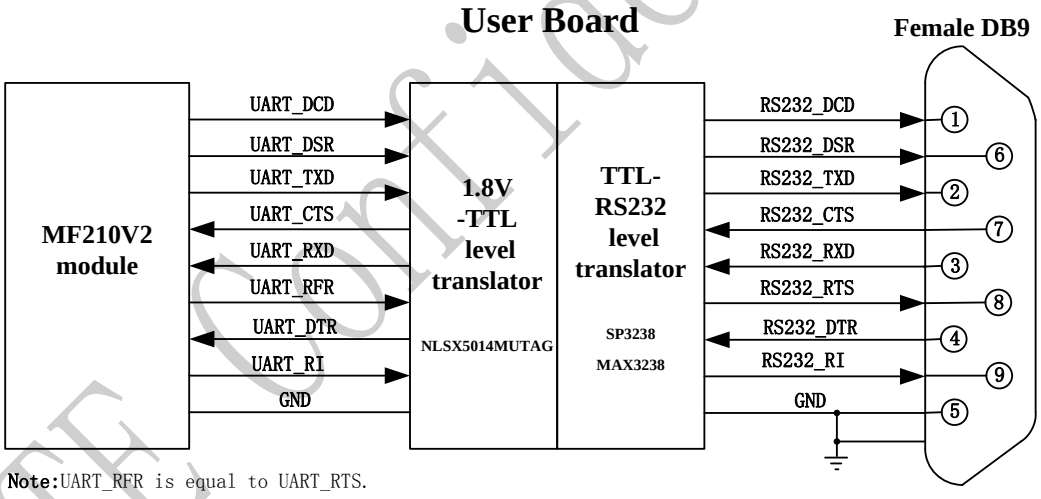


Figure 4–10 The connection of MF210V2 UART and Standard RS-232-C interface



4.2.10 SPI Interface Signal Group

The SPI signal interface is simulated by the GPIO interface, used to control PCI voices. The SPI_CLK clock is 127.2kHz. SPI control signal (pin No: 3/5/6/7). This is an SPI control signal. Table 4-7 describes detailed definition for each signal. The system board side needs to convert the power level of SPI_SDI (SPI control output signal cable on the system board side) into 2.6V, to comply with the high power level VIH input requirements.

Table 4–7 Definition and Description of SPI Control Signal Group

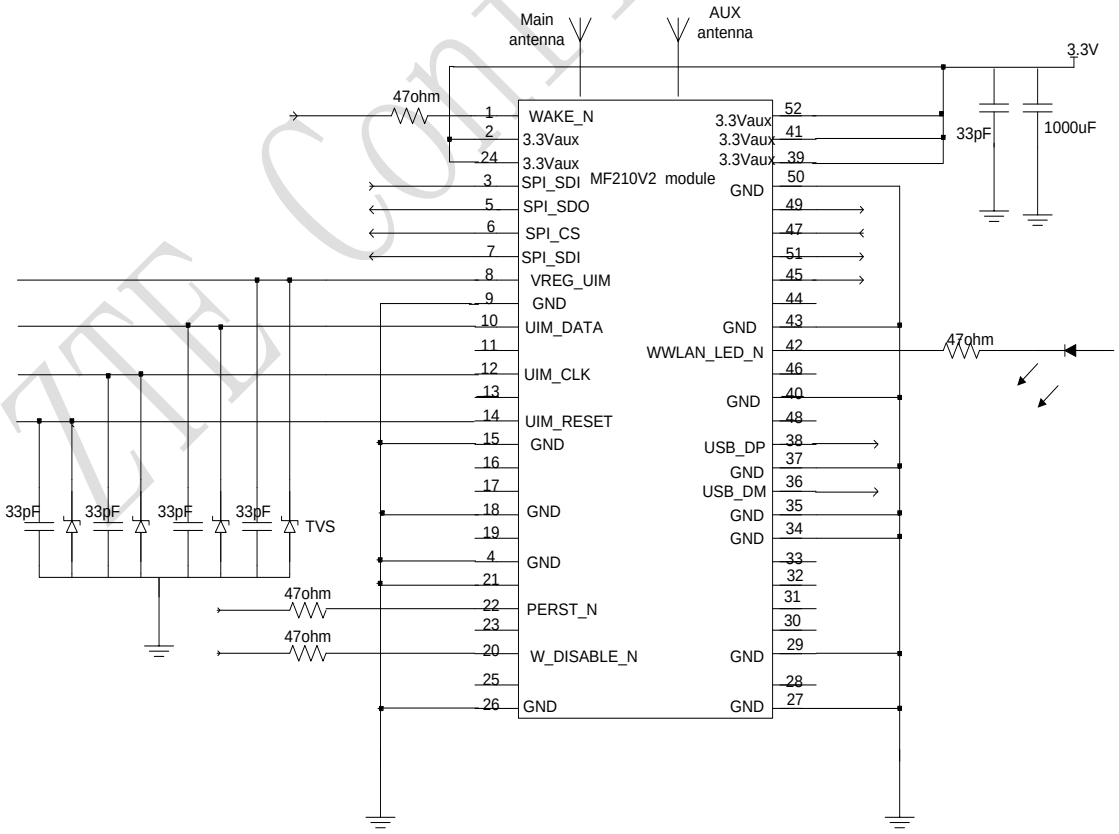
PIN	Signal Definition	Pin I/O	Signal Description
3	SPI_SDI	I	SPI data signal, MF210V2 input, input high power level is VIH, and low power level is VIL. (If this pin is configured as SPI_SDI signal, the reuse signal can't be used)
5	SPI_SDO	O	SPI data signal, MF210V2 output, input high power level is VOH, and low power level is VOL. (If this pin is configured as SPI_SDO signal, the reuse signal can't be used)
6	SPI_CS	O	SPI segment signal, MF210V2 output, input high power level is VOH, and low power level is VOL.
7	SPI_CLK	--	SPI synchronization clock, 100kHz, output by MF210V2, high power level is VOH, and low power level is VOL. (If this pin is configured as SPI_CLK signal, the reuse signal can't be used)

Note: VIH, VIL, VOH, and VOL comply with the power I/O interface power level requirements in 5.2.

4.3 Typical Interface Circuit

Figure 4-11 illustrates the typical interface circuits.

Figure 4–11 Typical Interface Circuit



5 Electric Features

5.1 Operating & Storage Temperature

Table 5–1 Product Temperature Range

Parameter	Minimum	Maximum
Normal Operating temperature	-25°C	+60°C
Extreme Operating temperature	-25°C	+75°C
Storage temperature	-40°C	+85°C

Table 5–2 Testing Results of Product Temperature in Windless Environment

Mode	Environment Temperature	Voltage	Transmission Power	Duration
GPRS Class 10	+60°C	3.8V	Max	≥1 hour
EDGE Class 12	+60°C	3.8V	Max	≥1 hour
WCDMA	+60°C	3.8V	Max	≥1 hour

5.2 Power Level of IO Interface

Table 5–3 Power Level of IO Interface

Parameter	Description	Minimum	Maximum
VIH	High-level input voltage	0.65*VDD_PX V	VDD_PX+0.3 V
VIL	Low-level input voltage	0 V	0.35*VDD_PX V
VOH	High-level output voltage	VDD_PX-0.45 V	VDD_PX V
VOL	Low-level output voltage	0 V	0.45 V

Note:
1. High and low level of input voltage must locate within the ranges specified in the above table.
2. High and low level of external interface signals must match interface level of this product.
3. VDD_PX, X=1 or 2, which indicates the electrical properties of P1 or P2 group pin

Table 5–4 Module Working Condition

Signal	Description	Min	Typical	Max	Unit
VDD_P1	Supply voltage P1 for Pad group1 interfaces	2.5	2.6	2.7	V
VDD_P2	Supply voltage P2 for Pad group2 interfaces	2.7	2.85	3	V

Note:
1. Typical voltage value indicates the default input/output voltage of P1 and P2 pin groups in this product. An external input pin must provide the interface voltage of this value.
2. The design of external circuit interface voltage must match pin voltage.

5.3 Power Supply

5.3.1 Input Power

Table 5–5 Input Power

Parameter	Minimum	Typical	Maximum
Input voltage	3.0V	3.3V	3.8V

5.3.2 Operating Current

Table 5–6 Averaged standby DC power consumption

Mode	Bands	Test value (mA)	Remark
HSDPA/WCDMA	UMTS bands	1.80	Sleep mode
GSM/GPRS/EDGE	GSM bands	4.60	Sleep mode
Note: assumes USB bus is fully suspended during measurements. Under different environments, the testing results might be slightly different. Take the actual situation as the reference.			

Table 5–7 Averaged idle mode DC power consumption

Mode	Bands	Test value (mA)	Remark
HSDPA/WCDMA	UMTS bands	140	Idle mode
GSM/GPRS/EDGE	GSM bands	140	Idle mode
Note: The IDLE mode indicates the power consumption of the module when there is no service. But the module is interactiving with the network such as network registration, and USB is active. The above values are the average of some test samples. Under different environments, the testing results might be slightly different. Take the actual situation as the reference.			

Table 5–8 Averaged DC power consumption in data transmission state

Mode	Bands	Test value (mA)	Remark
HSDPA/HSUDP/HSPA+ (7.2or3.6/5.76/14.4)	Band I (IMT2100)	TBD	The module in state of data transmission.
	Band II (PCS1900)	TBD	
	Band V (850M)	TBD	
	Band VIII (900M)	TBD	
GPRS	GPRS1900	290	The module in state of data transmission.
	GPRS1800	310	
	GPRS900	460	
	GPRS850	450	

EDGE	EDGE1900	340	The module in state of data transmission.
	EDGE1800	360	
	EDGE900	440	
	EDGE850	425	
Note: The above average current is acquired under the maximum transmission power. Under different environments, the testing results might be slightly different. Take the actual situation as the reference.			

5.3.3 Power-on/Resetting Flow

Table 5–9 Power-on/Resetting Period

No	Status	Average	Remark
1	Response time of power-on and power-off	About 6s	From the time of module power-on to port initialization
2	Searching network upon power-on	About 10s	Depending on the actual network situation
Note: 1. The specific power-on/power-off response time depends on the actual software versions. The time of searching network upon power-on differs according to the network quality. The above values are only an example. 2. By default, the module is started up upon power-on.			

5.4 Reliability

Table 5–10 Reliability Feature

Test Standard / Test Item	Test Condition	Test Reference
Random Oscillation	Frequency range: 5-20Hz, PSD:1.0m2/s3; Frequency range: 20-200Hz, -3dB/oct; On the 3 axis, 1 hour for each axis	IEC 68-2-6
Shock Testing	Half sine wave shock Acceleration: 20g Short time: 11ms On 6 axis, one shock on each axis (±x, y and z)	TIA/EIA 603 3.3.5 GB/T 15844.2.4.1

Test Standard / Test Item	Test Condition	Test Reference
Temperature Shock	Low temperature: -40°C ±2°C High temperature: +80°C ±2°C Temperature changing time: less than 30 seconds Testing duration: 2 hours Cycles: 10	IEC 68-2-14 Na
High-temperature Working	Temperature: +60°C Testing duration: 24h	ZTE standard
Low-temperature Working	Temperature: -25°C Testing duration: 24h	ZTE standard
High-temperature and high humidity	Temperature: +55°C Humidity: 95% Duration: 48 hours	ZTE standard
High-temperature Storage	Temperature: 85°C Testing duration: 24h	IEC 68-2-1 Ab
Low-temperature Storage	Temperature: -40°C Testing duration: 24h	IEC 68-2-2 Bb

5.5 Reliability Test Result

Table 5–11 Temperature Testing Result Under Windless Environment

Mode	Ambient Temperature	Voltage	Transmission power	Duration	Results
GPRS Class 10	+25°C	(3.3±9%)V	Max	⩾1 hour	Pass
EDGE Class 12	+25°C	(3.3±9%)V	Max	⩾1 hour	Pass
WCDMA	+25°C	(3.3±9%)V	Max	⩾1 hour	Pass

Table 5–12 Test Results of High/low Temperature Running and Reliability Test

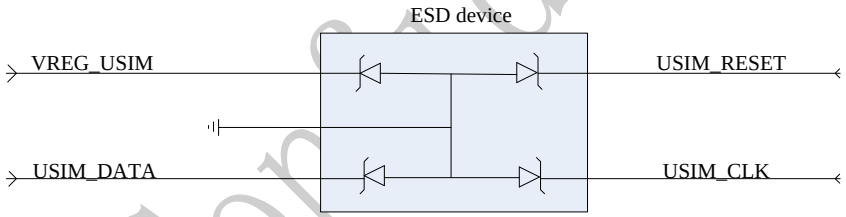
Test Item	Test Conditions and Criteria	Test Items	Results
Random vibration	Refer to table 5-8	RF test and function test	Pass
Impact test	Refer to table 5-8	RF test and function test	Pass
Temperature impact	Refer to table 5-8	RF test and function test	Pass
Running at low temperature	Refer to table 5-8	RF test and function test	Pass

Running at high temperature	Refer to table 5-8	RF test and function test	Pass
Running at the limit of low temperature	Refer to table 5-8	RF test and function test	Pass
Running at the limit of high temperature	Refer to table 5-8	RF test and function test	Pass
Storage at low temperature	Refer to table 5-8	RF test and function test	Pass
Storage at high temperature	Refer to table 5-8	RF test and function test	Pass

5.6 ESD

ESD protection needs to be performed during the usage of MF210V2 module. Figure 5–1 shows the recommended circuit of the USIM card.

Figure 5–1 Recommended Circuit of ESD Protection on USIM Card



6 Radio Frequency Performance Index

6.1 Technical Index of RF in UMTS Mode

6.1.1 Acquiring Radio Frequency Index

The testing of radio frequency index should strictly follow the specified testing specifications of 3GPP. In particular, when carrying out the acceptance test of related indexes, make sure to perform the test in a well-shielded environment.

6.1.2 Maximum Transmission Power

Under the normal testing environment, the maximum transmission power of UMTS2100/ 1900/850(900) should satisfy the requirements in Table 6–1.

Table 6–1 Maximum Transmission Power

Operating Band	Power level	The range of Power Required in the 3GPP Protocol(dBm)	Test value
UMTS850	Class 3	+24dBm +1/-3dBm	22.5dBm
UMTS900	Class 3	+24dBm +1/-3dBm	TBD
UMTS1900	Class 3	+24dBm +1/-3dBm	22.5dBm
UMTS2100	Class 3	+24dBm +1/-3dBm	22.5dBm

6.1.3 Receiving Sensibility

The receiving sensitivity is a key parameter that indicates the receiver performance of module. The receiving sensitivity is the weakest signal that the module at the antenna port can receive. At the same time the BER (Bit Error Rate) must meet the 3GPP TS 34.121protocol requirements in case of the minimum signal. The test value of UMTS2100/1900/850(900) receiving sensibility is shown in the Table 6-2.

Table 6–2 Reference Table of Receiving Sensitivity

Operating Band	Unit	3GPP Protocol Claim	Test value
UMTS850	dBm/3.84 MHz	≤-104.7dBm	-108dBm
UMTS900	dBm/3.84 MHz	≤-103.7dBm	TBD
UMTS1900	dBm/3.84 MHz	≤-104.7dBm	-108dBm
UMTS2100	dBm/3.84 MHz	≤-106.7dBm	-109dBm

6.1.4 Spurious Emission Index

The spurious emission index of UMTS2100/1900/850(900) should comply with the requirements in 3GPP TS 34.121 protocol, as illustrated below. And the test result of module MF210V2 in UMTS mode meets the requirement in Table 6-3.

Table 6–3 Spurious Emission Index

Frequency Band	Resolution Bandwidth	Minimum Requirement
9 kHz ≤ f < 150 kHz	1 kHz	-36 dBm
150 kHz ≤ f < 30 MHz	10 kHz	-36 dBm
30 MHz ≤ f < 1000 MHz	100 kHz	-36 dBm
1 GHz ≤ f < 12.75 GHz	1 MHz	-30 dBm

6.2 Technical Indexes of RF in GPRS/GSM/EDGE Mode

6.2.1 Output Transmission Power

The maximum output transmission power of GSM850/900/1800/1900 (GMSK/8PSK) should comply with the requirements of 3GPP TS 05.05 4.1 protocol, as shown in Table 6–4 indicates the power level of each frequency band in MF210V2.

Table 6–4 Output Transmission Power of GSM850/900/1800/1900 (GMSK)

Operating Band	Power level	The range of Power Required in the 3GPP Protocol(dBm)	Test value
GSM850	Class 4	+33dBm±2dBm	32.5dBm
GSM900	Class 4	+33dBm±2dBm	32.5dBm
GSM1800	Class 1	+30dBm ±2dBm	29.5dBm
GSM1900	Class 1	+30dBm ±2dBm	29.5dBm

6.2.2 Receiving Sensibility

The receiving sensitivity is a key parameter that indicates the receiver performance of module. The receiving sensitivity is the weakest signal that the module at the antenna port can receive. At the same time the BER (Bit Error Rate) must meet the 3GPP TS 05.05 6.2 protocol requirements in case of the minimum signal. The test value of GSM850/900/1800/1900 receiving sensibility is shown in the Table 6-5.

Table 6–5 Reference Table of Receiving Sensitivity

Operating Band	Unit	3GPP Protocol Claim	Test value
GSM850	dBm/3.84 MHz	≤-102dBm	-107dBm
GSM900	dBm/3.84 MHz	≤-102dBm	-107dBm
GSM1800	dBm/3.84 MHz	≤-102dBm	-107dBm
GSM1900	dBm/3.84 MHz	≤-102dBm	-107dBm

6.2.3 Spurious Emission Index

The spurious emission index of GSM850/900/1800/1900 (GMSK) should comply with the requirements of 3GPP TS 4.3.2.1 protocol, as shown in the table below.

The power measured in bandwidth of 9kHz to 1GHz shall be no more than -36 dBm.

The power measured in bandwidth of 1GHz to 12.75GHz shall be no more than -30dBm.

And the test result of module MF210V2 in GPRS/GSM/EDGE mode meets the requirement above.

7 Antenna

The Dx receiving and GPS function of MF210V2 are optional (the user can choose the Dx receiving function that supports the W frequency band or the GPS function). If the Dx receiving function (or GPS) is required, add the Dx (or GPS) antenna on the system equipment. The design of Dx antenna is the same as that of the main antenna, and its efficiency index is allowed to decrease by 10dB.

7.1 Technical Parameters of Main (Auxiliary) Antenna Testing Console

The 3.2 topic illustrates the specifications of the RF testing console, and Table 7–1 illustrates the RF indexes.

Table 7–1 Index of Radio Frequency Testing Console

W2100	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**9612 Tx**	**10562 Rx**	**9750Tx**	**10700 Rx**	**9888 Tx**	**10838 Rx**
		1922.4MHz	**2112.4MHz**	**1950.0 MHz**	**2140.0 MHz**	**1977.6 MHz**	**2167.6 MHz**
	LOG MAGNITUDE (dB)	-4.98	-6.3	-4.4	-6.4	-15.5	-4.3
	SWR (Standing Wave) U	3.59	2.89	4.0	2.83	1.41	4.15
	SWITH CHART (IMPEDANCE) Ω	46.05Ω	25.46Ω	16.27Ω	28.5Ω	41Ω	17.6Ω
		-63.33 jΩ	-30.94 jΩ	-26.45 jΩ	-34.98 jΩ	12.54 jΩ	-32.42 jΩ
W1900	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**9262Tx**	**9662 Rx**	**9400Tx**	**9800 Rx**	**9538 Tx**	**9938 Rx**
		1852.4MHz	**1932.4MHz**	**1880 MHz**	**1960.0 MHz**	**1907.6 MHz**	**1987.6 MHz**
	LOG MAGNITUDE (dB)	-13.84	-13.84	-8.29	-16.8	-11.2	-10.55
	SWR (Standing Wave) U	1.52	1.56	2.25	1.34	1.76	1.85
	SWITH CHART (IMPEDANCE) Ω	33.17Ω	66.87Ω	50.48Ω	62.2Ω	70.85Ω	44.3Ω
		1.3 jΩ	-19.84 jΩ	-41.88 jΩ	-10.83 jΩ	-26.62 jΩ	-28.7 jΩ
W850	S11 main antenna RF	**4132 Tx**	**4357 Rx**	**4182Tx**	**4407 Rx**	**4232Tx**	**4457Rx**

	console (from RF head to beginning =1.7cm) / MHz	**826.4MHz**	**871.4MHz**	**836.4 MHz**	**881.4 MHz**	**846.6 MHz**	**891.6 MHz**
	LOG MAGNITUDE (dB)	-7.5	-6.4	-4.6	-11.4	-10.6	-11.8
	SWR (Standing Wave) U	2.47	2.86	4.09	2.16	2	1.78
	SWITH CHART (IMPEDANCE) Ω	20.65Ω	18.25Ω	15.75Ω	32.27Ω	28.38Ω	32.58Ω
		-6.34 jΩ	-8.9 jΩ	-23.71 jΩ	-20.25 jΩ	11.13 jΩ	-14.71 jΩ
W900	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**2712 Tx**	**2937 Rx**	**2787Tx**	**3012Rx**	**2863 Tx**	**3088 Rx**
		882.4MHz	**927.4MHz**	**897.4 MHz**	**942.4MHz**	**912.6 MHz**	**957.6 MHz**
	LOG MAGNITUDE (dB)	-9.1	-7.6	-4.8	-10	-4.8	-16.4
	SWR (Standing Wave) U	2.1	2.5	3.7	1.9	3.7	1.4
	SWITH CHART (IMPEDANCE) Ω	25.59Ω	23.65Ω	13.45Ω	26.92Ω	15.15Ω	41.15Ω
		10.84 jΩ	-18.27 jΩ	-0.71 jΩ	8.84 jΩ	-16.47 jΩ	-11.92 jΩ

W2100	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**9612 Tx**	**10562 Rx**	**9750Tx**	**10700 Rx**	**9888 Tx**	**10838 Rx**
		1922.4MHz	**2112.4MHz**	**1950.0 MHz**	**2140.0 MHz**	**1977.6 MHz**	**2167.6 MHz**
	LOG MAGNITUDE (dB)	-7.0	-4.8	-7.2	-5	-7.4	-10.1
	SWR (Standing Wave) U	2.58	3.75	2.55	3.6	2.48	1.92
	SWITH CHART (IMPEDANCE) Ω	94Ω	13Ω	125.4Ω	14.08Ω	104.64Ω	25.9Ω
		51.1 jΩ	-5.66 jΩ	-14.2 jΩ	-6.33 jΩ	-40.04 jΩ	-1.13 jΩ
W1900	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**9262Tx**	**9662 Rx**	**9400Tx**	**9800 Rx**	**9538 Tx**	**9938 Rx**
		1852.4MHz	**1932.4MHz**	**1880 MHz**	**1960.0 MHz**	**1907.6 MHz**	**1987.6 MHz**

	LOG MAGNITUDE (dB)	-6.9	-4.4	-6.7	-11.8	-6.6	-3.2
	SWR (Standing Wave) U	2.66	3.99	2.72	1.69	2.75	5.48
	SWITH CHART (IMPEDANCE) Ω	131.8Ω	12.56Ω	74.92Ω	38.57Ω	24.92Ω	9.15Ω
		-10.53 jΩ	2.04 jΩ	-58.68 jΩ	-20.21 jΩ	-27.6 jΩ	4.196 jΩ
W850	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**4132 Tx**	**4357 Rx**	**4182Tx**	**4407 Rx**	**4232Tx**	**4457Rx**
		826.4MHz	**871.4MHz**	**836.4 MHz**	**881.4 MHz**	**846.6 MHz**	**891.6 MHz**
	LOG MAGNITUDE (dB)	-1	-4.2	-1.2	-3.7	-1.5	-8.7
	SWR (Standing Wave) U	16.6	4.24	14.4	4.08	11.4	2.2
	SWITH CHART (IMPEDANCE) Ω	3.1Ω	12.55Ω	3.54Ω	14Ω	4.4Ω	26.6Ω
		-8.9 jΩ	-12.15 jΩ	-6.7 jΩ	-28.58 jΩ	-2.2 jΩ	-16.79 jΩ
W900	S11 main antenna RF console (from RF head to beginning =1.7cm) / MHz	**2712 Tx**	**2937 Rx**	**2787Tx**	**3012Rx**	**2863 Tx**	**3088 Rx**
		882.4MHz	**927.4MHz**	**897.4 MHz**	**942.4MHz**	**912.6 MHz**	**957.6 MHz**
	LOG MAGNITUDE (dB)	-1.2	-16.59	-1.21	-9.45	-3.1	-9
	SWR (Standing Wave) U	14.48	1.36	14.36	2.02	5.66	2.13
	SWITH CHART (IMPEDANCE) Ω	3.5Ω	38.28Ω	3.5Ω	30.65Ω	9.1Ω	24.9Ω
		-6.93 jΩ	-5.56 jΩ	-3.16 jΩ	-20.35 jΩ	8.48 jΩ	-8.98 jΩ

7.2 Passive Index (Recommended Value)

The passive index of antenna is different according to the different product type. The following table takes the 3G Internet-access laptop as an example, to illustrate the recommended passive antenna index, as shown in Table 7–2 and Table 7–3.

Table 7–2 Passive Index of Main Antenna (Recommended Value)

Frequency Band	824-960MHz	1710-2170MHz
VSWR in Free Space	<3:1	<3:1
Peak Gain in Free Space	>0dBi	>0dBi
3-D Average Gain in Free Space	-3dBi	-3dBi
Antenna Efficiency	>50%	>50%

Table 7–3 Passive Index of Rx Antenna (Recommended Value)

Frequency Band	824-960MHz	1710-2170MHz
VSWR in Free Space	<3:1	<3:1
Secondary-to-Primary Antenna Isolation, |S21|	<-10dB	< 10dB
Peak Gain in Free Space	>-5dB	> 5dB
3-D Average Gain in Free Space	-7dBi	-7dBi
Antenna Efficiency	>20%	> 20%

7.3 Active Index (Recommended Value)

The active index of antenna is different according to the different wireless Internet-access product. The following parameter takes the 3G Internet-access laptop as an example, to illustrate the recommended active antenna index.

TRP: <W850/W900/W1900/W2100>18dBm;

GSM850>27dBm, GSM900>27dBm; DCS1800>24dBm, PCS1900>24dBm

TIS: <W850/W900<-100dBm; W1900/W2100<-103dBm;

GSM850<-100dBm, GSM900<-100dBm; DCS1800/PCS1900<-102dBm

7.4 Product Layout among Terminal Products

The module layout among other terminal products should take full consideration of the electric magnetic compatibility. As the types of terminal products vary and their circuit layouts are different, when considering the module layout, we should reduce the electric magnetic interference from other devices upon the module. Taking 3G Internet-access laptop as an example, during the layout of laptops, make sure that the module is not adjacent to the switch power or the high-speed signal cable, and well protect the cabling of these interference sources. At the same time, keep the antenna and the coaxial cables of network cables and antenna far away from the interference sources. Keep MF210V2 away from the devices that have a large heat-radiating capacity such as CPU, hard disk and south bridge, to guarantee that heat can be radiated effectively.

7.5 Antenna Dimensions & Location

The dimensions of different terminal products are different, so they impose different requirements upon the performance of antenna. The dimensions and location of antennas are also different. Taking 3G Internet-access laptop as an example, it is recommended that the antenna dimensions be above 7mm*10mm*100mm, and the antenna be placed on the top of LCD.

7.6 Design of Rx Antenna

The design of Rx antenna is the same as that of the main antenna, only its efficiency index is allowed to decrease by 3dB. The separation degree between the main antenna and the Rx antenna should be greater than 12dB. The difference between Rx TIS and the TIS of main antenna should be within 6dbm.

7.7 Recommended Upgrade Methods

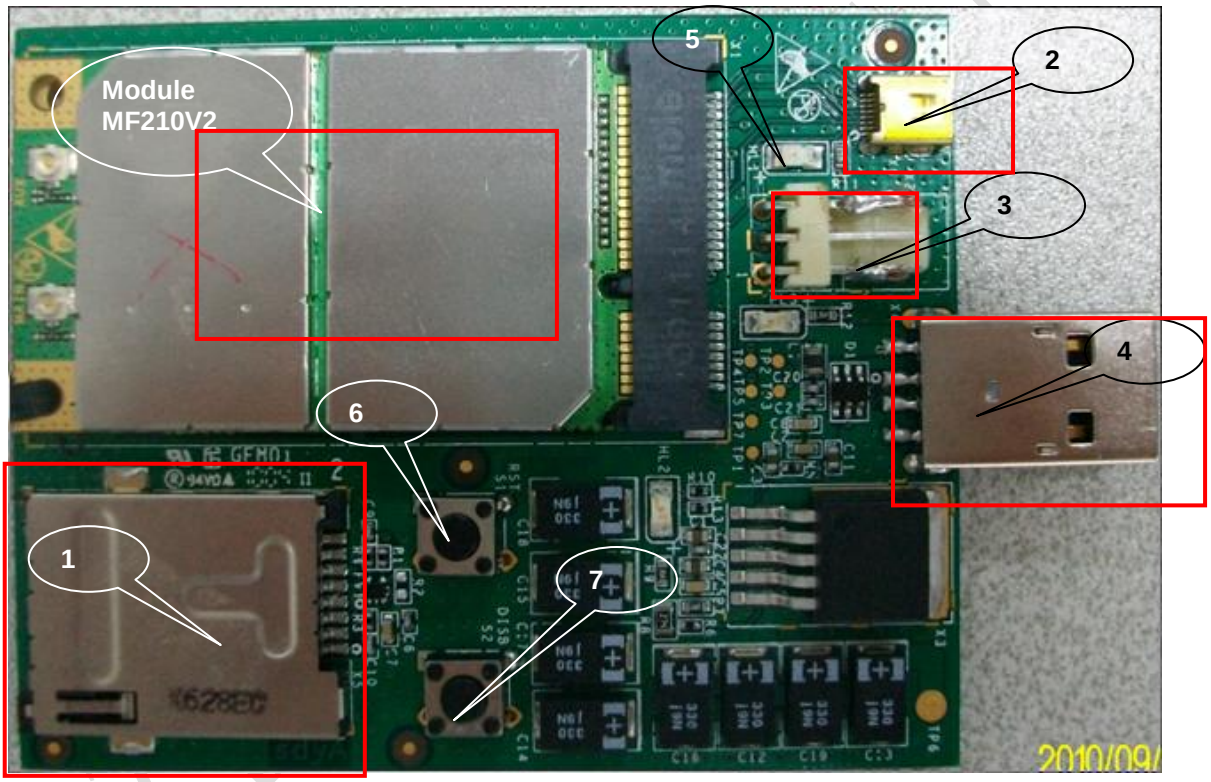
It's recommended to use the one-click software upgrade tool to upgrade through the USB port provided by ZTEWelink in the Windows system. If the customers want to upgrade the module in other operation systems, ZTEWelink provides the corresponding reliable tools too.

8 Debugging Environment & Methods

8.1 Debugging Board

Figure 8–1 shows the module debugging & installation method. The debugging board is mainly used to debug the basic functions of MF210V2 module, such as downloading the JTAG program, resetting the module, powering off and shutting down RF, LED indicator display, making a call or browsing web pages by inserting the USIM card into the computer UI. The USB interface supplies power to the debugging board, provides it to the module after LDO conversion, and directly supplies the 3.3V power to the module by the power socket on the board.

Figure 8–1 Debugging Board



Note: 1 – UIM card console; 2 –JTAG downloading interface; 3-3.3V DC power interface; 4 – USB interface; 5 – LED indicator; 6 - PON_RESET_N button (module resetting); 7 -W_DISABLE_N button (RF switch)

8.2 Interfaces on Debugging Board

8.2.1 JTAG Interface

The JTAG interface can be used to download and debug the firmware program.

8.2.2 USB Interface

The USB2.0 interface on the debugging board is connected to the PCI-E interface on MF210V2.

8.2.3 Power-supply Interface

The USB interface as illustrated in Figure 8–1 supplies power, provides the 3.3V power to the module after LDO conversion, and directly supplies the 3.3V power to the module by the power socket on the board.

8.2.4 USIM Card Console Interface

As shown in Figure 8–1, 1 the USIM card console is the 5PIN USIM card console on the conversion board, connecting to: power, ground, USIM_DATA, USIM_CMD and USIM_CLK. It supports the 1.8V/3V USIM card.

8.2.5 PON_RESET_N Button

This button corresponds to the PON_RESET_N PIN of the PCI-E interfaced. The user presses the button to reset the module.

8.2.6 W_DISABLE_N Button

This button corresponds to the W_DISABLE_N PIN of the PCI-E interface. The user presses this button to enable or disconnect RF, so as to perform the debugging of this PIN.

8.2.7 LED Indicator

The LED indicator on the debugging board is connected to the LED_WWAN_N interface of MF210V2. By controlling the indicator, the user can debug the function of this interface.